Radio, audio and associated systems Bipolar, MOS

BOOK IC01 1991

Philips Semiconductors

PHILIPS

RADIO, AUDIO AND ASSOCIATED SYSTEMS

BIPOLAR, MOS

Functional index

Functional index

Functional index

Functional index

Functional index

Functional index

Functional index

Functional index

Numerical index

Numerical index

Product status definition for type numbers with prefixes NE, PCA, PCB, PCD, SA, SAA, TDA, TEA and TSA

Ordering information for type numbers for type numbers with prefixes NE, PCA, PCB, PCD, PCD, SA, SAA, TDA, TEA and TSA

Type designation for type numbers with prefixes NE, PCA, PCB, PCD, SA, SAA, TDA, TEA and TSA

Rating systems

Handling MOS devices

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order

$250 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (– 55°C to + 125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5537N	LF398	LIN	Sample & Hold Amp

NE5537N

- Package Descriptions — See Table 2
- Device Number
- Device Family and Temperature Range Prefix—See Tables 3 & 4

LF398

- Description of Product Function

LIN

- Product Family: LIN Analog Products; MIL Military Products

Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to + 70°C
S	– 55° to + 125°C
NE	0° to + 70°C
SE	– 55° to + 125°C
SA	– 40° to + 85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

Pro electron type designation code for integrated circuits

TYPE DESIGNATION

Basic type number

This type designation applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick- film and hybrid integrated circuits.

A basic type number consists of three letters followed by a serial number.

FIRST AND SECOND LETTER

Digital family circuits

The first two letters identify the family (see note 1).

Solitary circuits

The first letter divides the solitary circuits into:

S : solitary digital circuits
T : analog circuits
U : mixed analog/digital circuits

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 2).

Microprocessors

The first two letters identify microprocessors and correlated circuits as follows:

MA: microcomputer central processing unit
MB: slice processor (see note 3)
MD: correlated memories
ME: other correlated circuits (interface, clock, peripheral controller, etc.)

Charge-transfer devices and switched capacitors.

The first two letters identify the following:

NH : hybrid circuits
NL : logic circuits
NM: memories
NS : analog signal processing, using switched capacitors
NT : analog signal processing, using change-transfer device
NX : imaging devices
NY : other correlated circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range. The letters A to G give information about the temperature:

A : temperature range not specified below (see note 4)
B : 0 to + 70 °C
C : −55 to +125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example : the range 0 to +75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

Version letter(s)

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack (2 leads)
G : for flat pack (4 leads)
H : for quadrature flat pack (QFP)
L : for chip on tape (foil)
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Pro electron type designation code for integrated circuits

TYPE DESIGNATION

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : cylindrical
D : dual-in-line (DIL)
E : power DIL (with external heatsink)
F : flat (leads on 2 sides)
G : flat (leads on 4 sides)
H : quadrature flat pack (QFP)
K : diamond (TO-3 family)
M : multiple-in-line (except dual-, triple-, quadruple-in-line)
Q : quadruple-in-line (QIL)
R : power QIL (with external heatsink)
S : single-in-line
T : triple-in-line
W : lead chip-carrier (LCC)
X : leadless chip-carrier (LLCC)
Y : pin grid array (PGA)

SECOND LETTER: Material

C : metal-ceramic
G : glass-ceramic (cerdip)
M : metal
P : plastic

To avoid confusion when the serial number ends with a letter, a hyphen is used preceding the suffix.

Examples (see note 5)

PCF1105WP : Digital IC, PC family, operational temperature range –40 to +85 °C, serial number 1105, plastic leaded chip-carrier.

GMB74LS00A-DC: Digital IC, GM family, operational temperature range 0 to +70 °C, company number 74LSS00A, ceramic DIL package.

TDA1000P : Analog circuit, no standard temperature range, serial number 1000, plastic DIL package.

SAC2000 : Solitary digital circuit, operational temperature range –55 to +125 °C.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).

2. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

3. By 'slice processor' is meant: a functional slice of microprocessor.

4. In the case of two same types with two different temperature ranges not specified below, one type should use the letter 'A' as the third letter and the other, the letter 'X'.

5. Some companies have been using version letters and/or two letter-suffix, which differ from the Pro Electron definitions. In case of confusion Pro Electron may be contacted.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and D.C. lines.

DEVICE DATA

Philips Components

Date of Issue	May 23, 1990
Status	Product Specification
Application Specific Product	

80C31/80C51/87C51

CMOS single-chip, 8-bit microcontroller

DESCRIPTION

The Philips 80C31/80C51/87C51 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC51 is functionally compatible with the NMOS 8031/8051 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

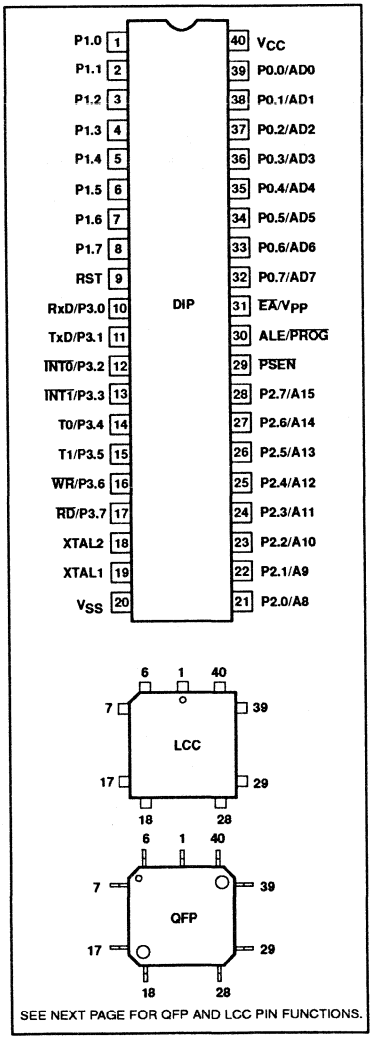
The 8XC51 contains a 4k x 8 ROM (80C51) EPROM (87C51), a 128 x 8 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

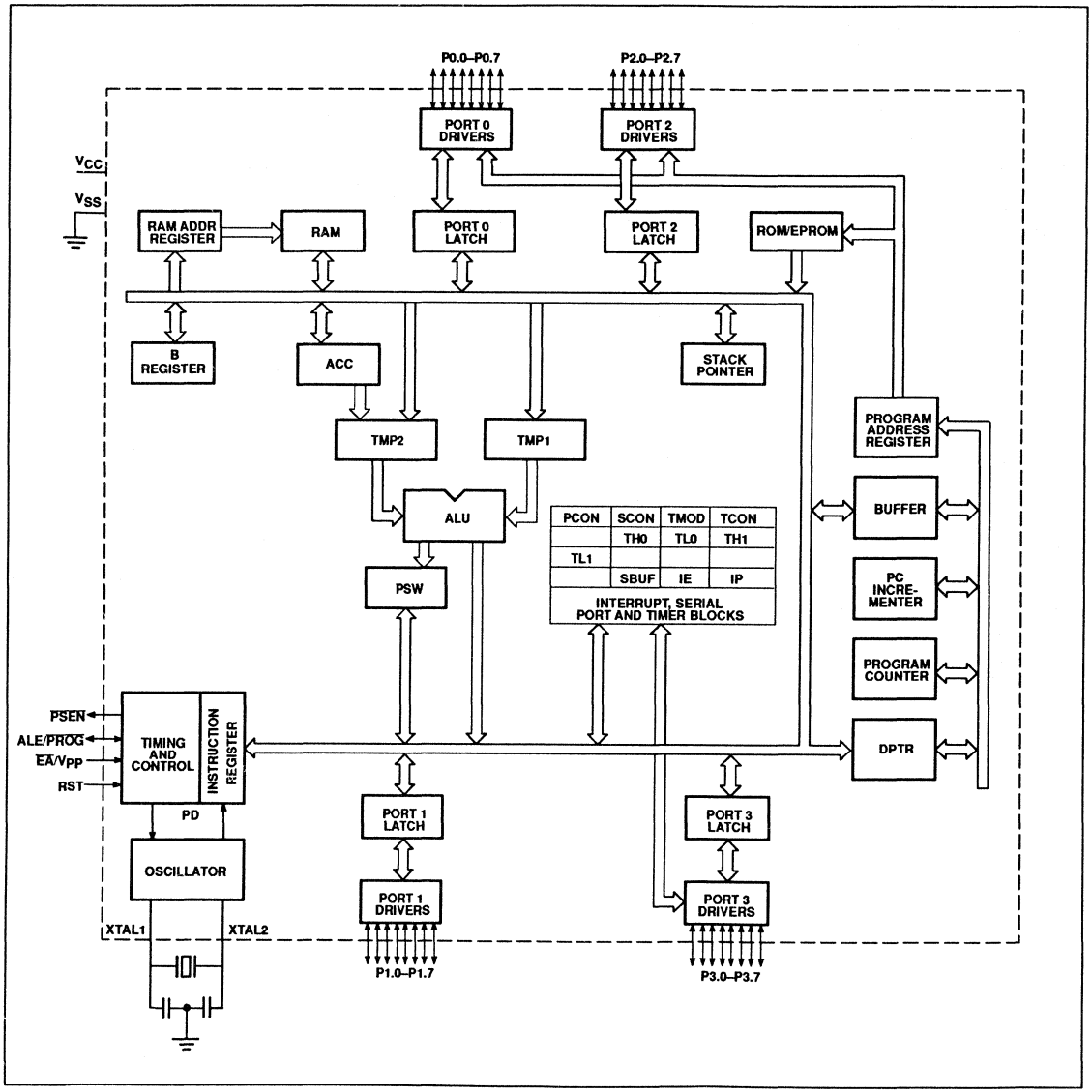
- 8031/8051 compatible
  - 4k x 8 ROM (80C51)
  - 4k x 8 EPROM (87C51)
  - ROMless (80C31)
  - 128 x 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Five speed ranges at V_{CC} = 5V
  - 12MHz
  - 16MHz
  - 20MHz
  - 24MHz
  - 30MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Document No.	
ECN No.	
Date of Issue	January 1990
Status	Preliminary Specification
Application Specific Product	

80C32/80C52/87C52
CMOS single-chip 8-bit microcontroller

DESCRIPTION

The Philips 80C32/80C52/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC52 is functionally compatible with the NMOS SCN-8032/8052 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

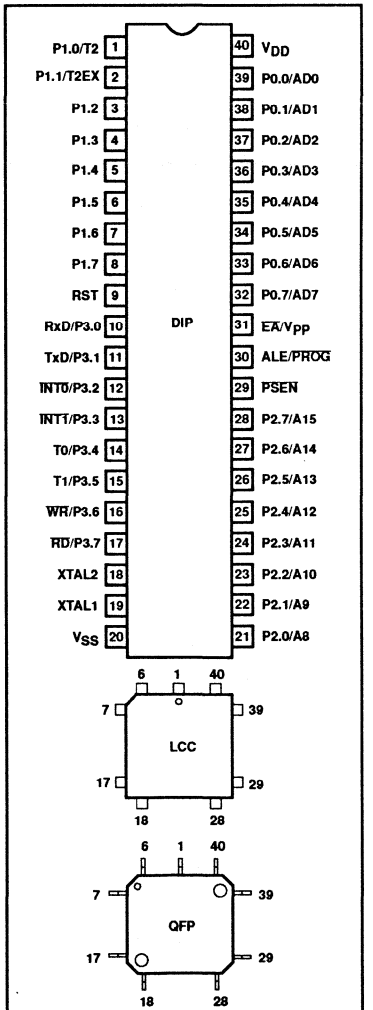
The 8XC52 contains an 8K x 8 ROM (80C52) EPROM (87C52), a 256 x 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 8XC52 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

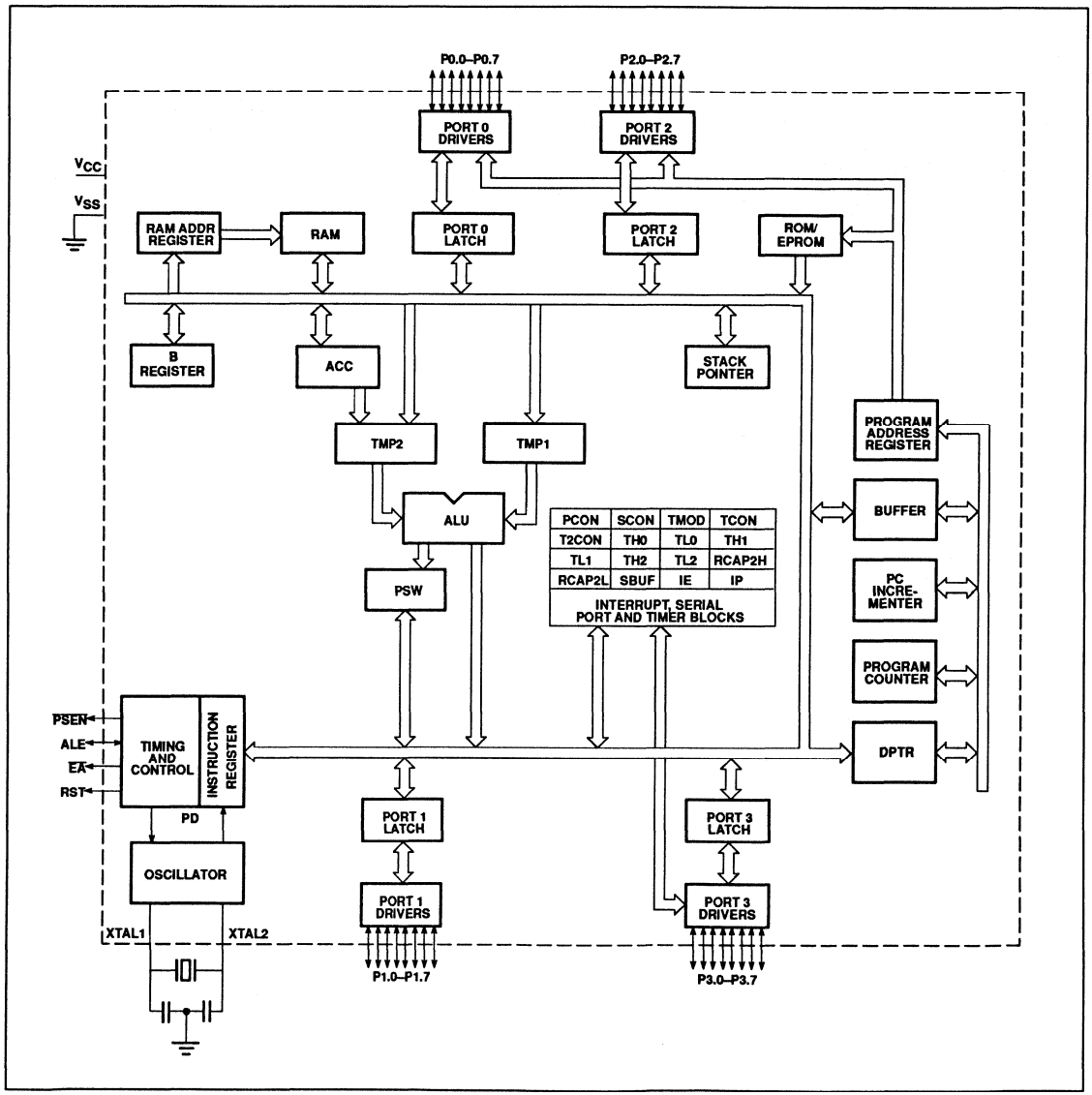
- 80C51 based architecture
- 8032/8052 compatible
  - 8k x 8 ROM (80C52)
  - 8k x 8 EPROM (87C52)
  - ROMless (80C32)
  - 256 x 8 RAM
  - Three 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Two speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 20MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC AND QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

80CL410/83CL410

Low voltage/low power single-chip 8-bit microcontroller

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.5V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

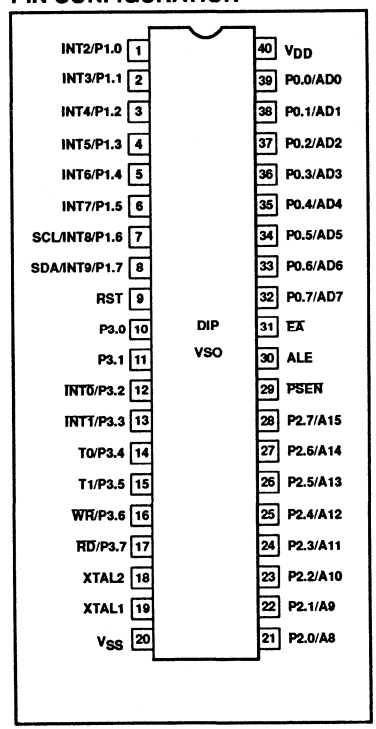
The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

FEATURES

- Supply voltage from 1.5 to 5.5V
- Operating frequency from 32kHz to 20MHz
- 80C51 based architecture
  - 4k x 8 ROM (64k external)
  - 128 x 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen source, two level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



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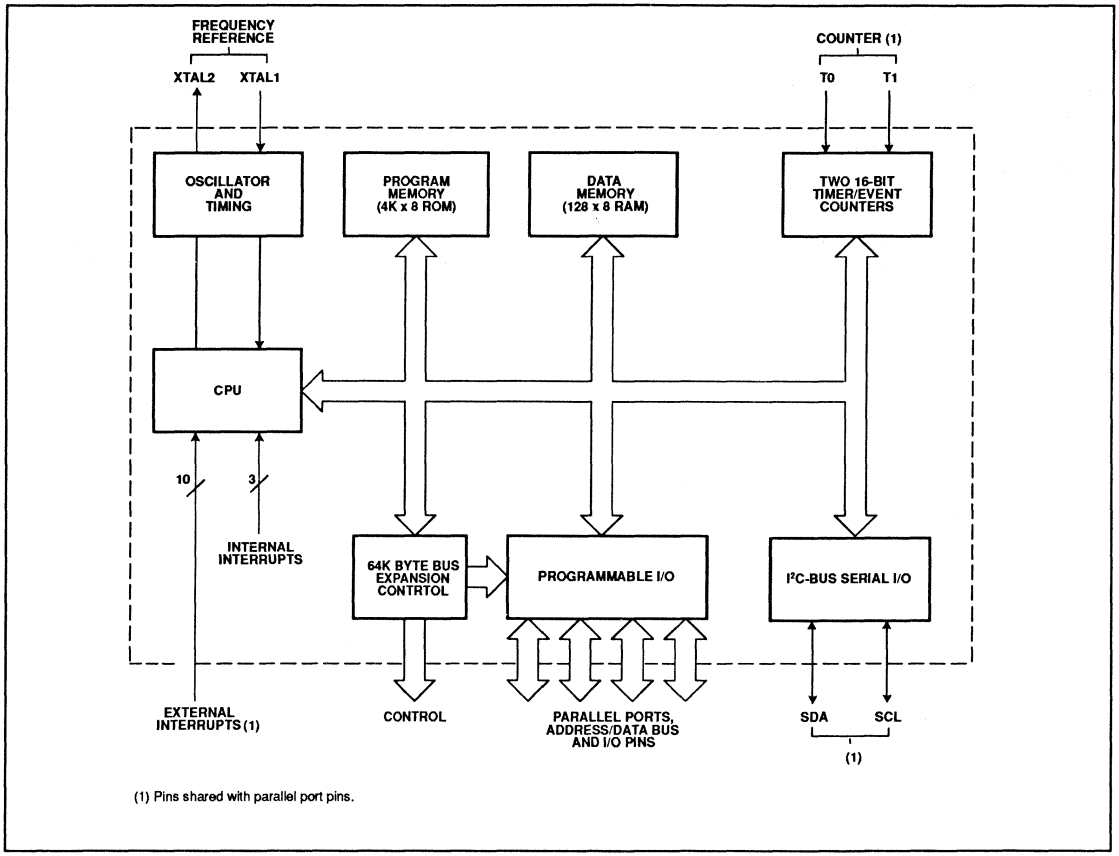


(1) Pins shared with parallel port pins.

Philips Components

Date of Issue	February 1, 1990
Status	Product Specification
Application Specific Product	

80C451/83C451/87C451

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The Philips 8XC451 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC451 is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines. The LCC version has a total of 68 pins. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 8XC451 includes a 4k X 8 ROM (83C451) EPROM (87C451), a 128 X 8 RAM, 56 (LCC) or 52 (DIP) I/O lines, two 16-bit timer/counters, a five source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or muti-processor communications, and on-chip oscillator and clock circuits. The 80C451 includes all of the 83C451 features except the on-board 4k X 8 ROM.

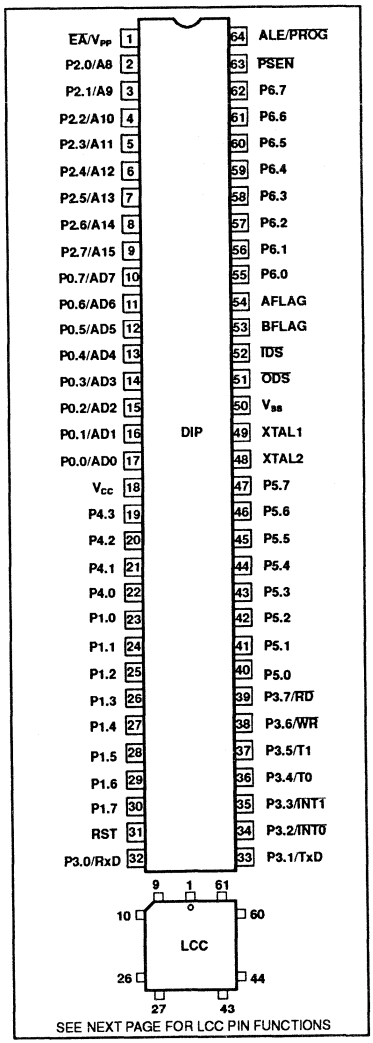
The 87C451 has 4k of EPROM on-chip as program memory and is otherwise identical to the 83C451.

The 8XC451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

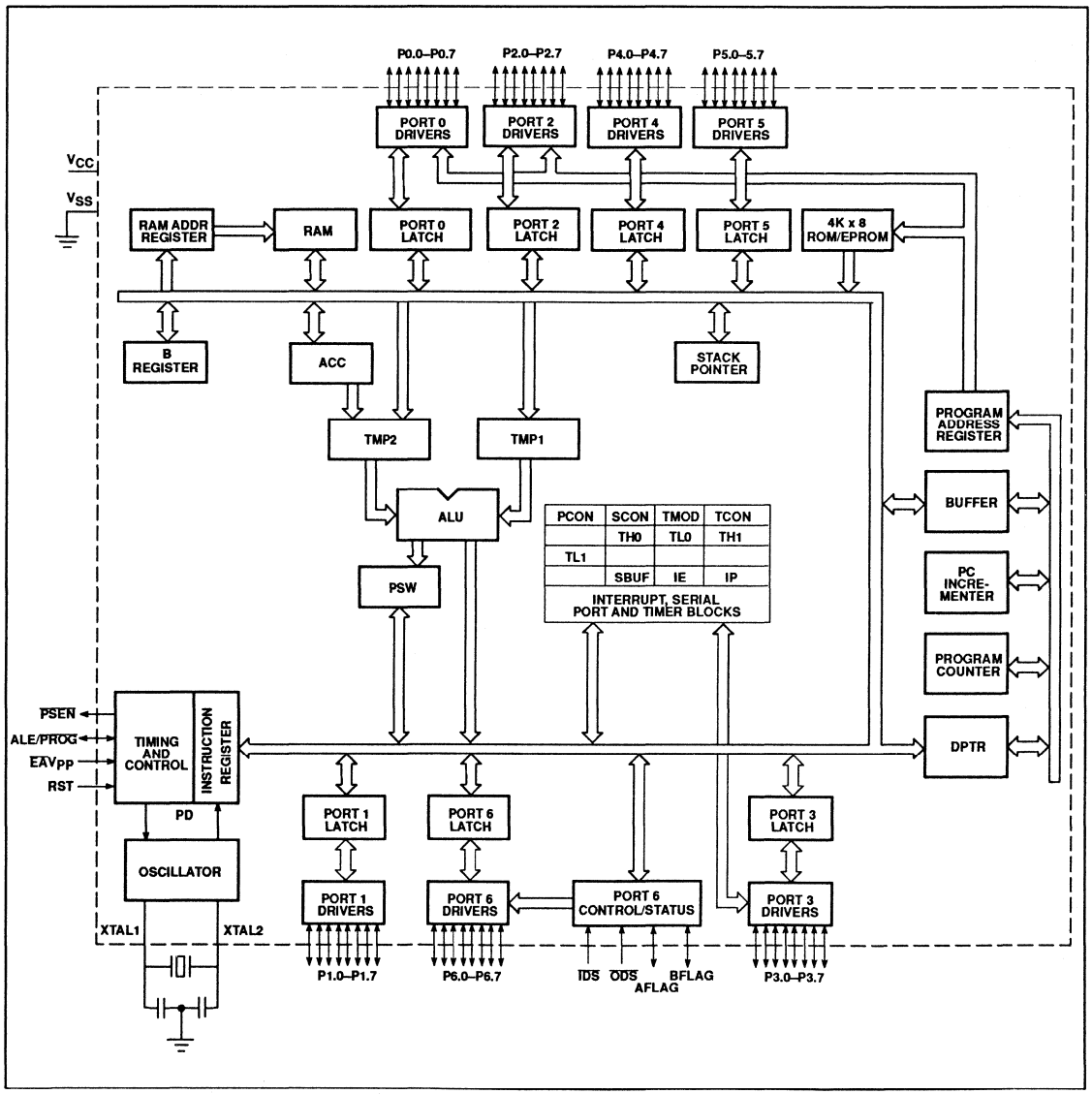
- 80C51 based architecture
- 68-pin LCC and 64-pin DIP packages:
  - Seven 8-bit I/O ports (LCC version)
  - Six 8-bit ports and one 4-bit port (DIP version)
- Port 6 features:
  - 8 data pins
  - 4 control pins
  - Direct MPU bus interface
  - Parallel printer interface
- On the microcontroller:
  - 4k X 8 ROM (83C451)
    4k X 8 EPROM (87C451)
    ROMless version (80C451)
  - 128 X 8 RAM
  - Two 16-bit counter/timers
  - Two external interrupts
- External memory addressing capability
  - 64k ROM and 64k RAM
- Low power consumption:
  - Normal operation: less than 24mA at 5V, 12MHz
  - Idle mode
  - Power-down mode

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC PIN FUNCTIONS

BLOCK DIAGRAM



Philips Components

Document No.	
ECN No.	
Date of Issue	February 1990
Status	Preliminary Specification
Application Specific Product	

80C528/83C528/87C528

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The 8XC528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroler family. The 8XC528 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

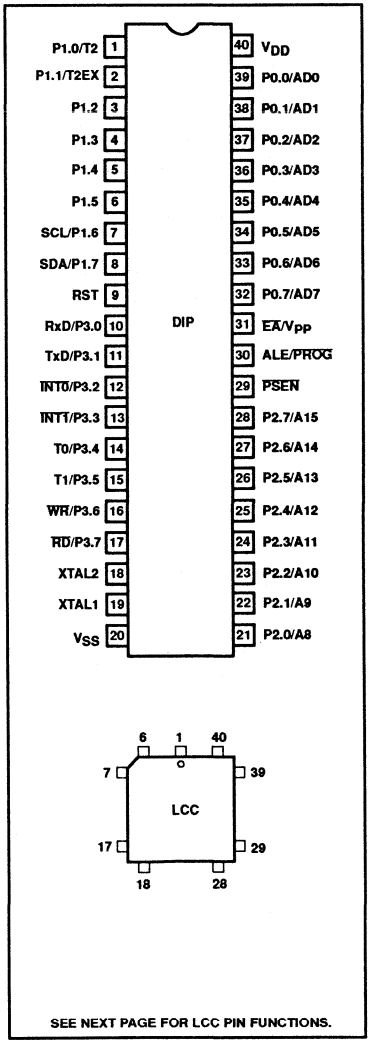
The 8XC528 contains a 32k x 8 ROM (83C528)/EPROM (87C528), a 512 x 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I^2C-bus), and on-chip oscillator and timing circuits.

In addition, the 8XC528 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

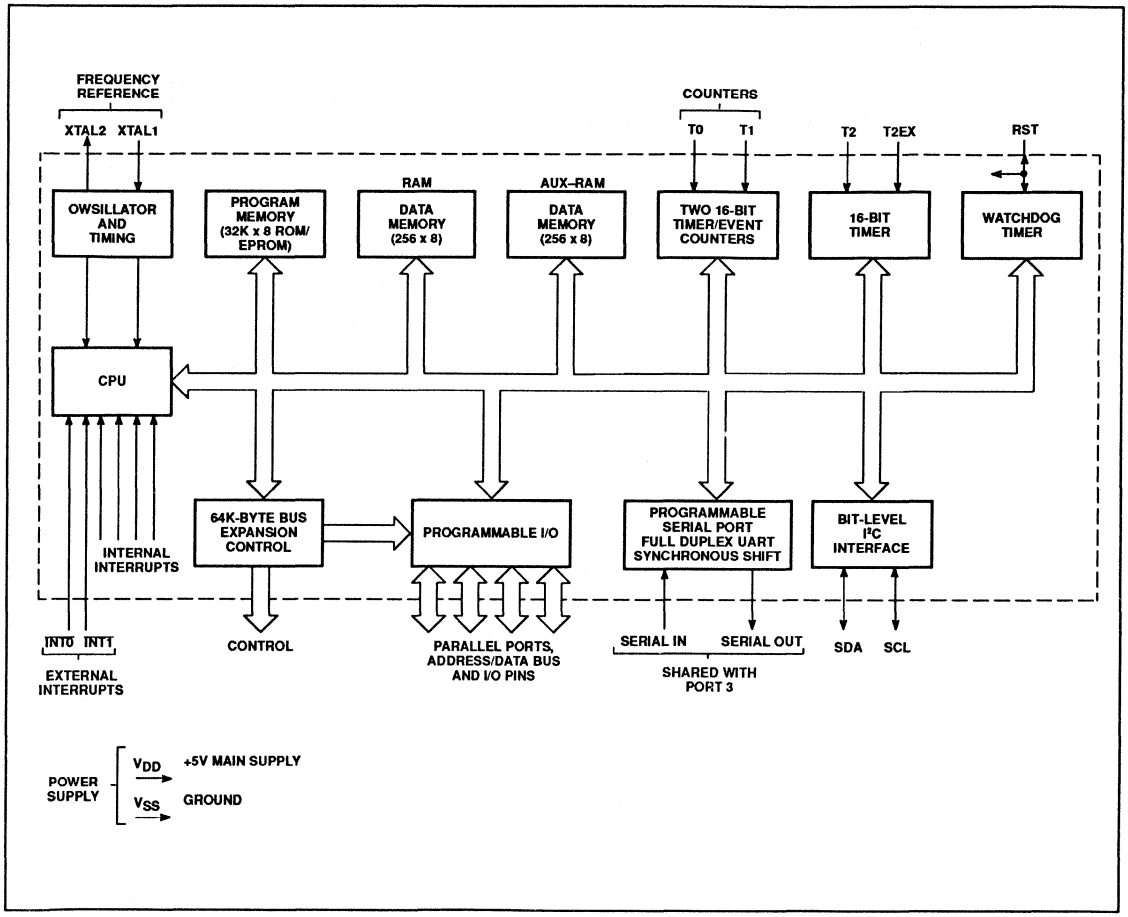
- 80C51 instruction set
  - 32k x 8 ROM (83C528)
  - 32k x 8 EPROM (87C528)
  - ROMless (80C528)
  - 512 x 8 RAM
  - Memory addressing capability – 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer
  - Full duplex UART
  - I^2C serial interface
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Three speed ranges at V_{DD} = 5V ±10%
  - 3.5 to 12MHz
  - 3.5 to 16MHz
  - 0.5 to 12MHz
- Extended temperature ranges
- OTP package available
- ROM/EPROM code protection

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Document No.	
ECN No.	
Date of Issue	August 1990
Status	Preliminary Specification
Application Specific Product	

80C550/83C550/87C550

CMOS single-chip 8-bit microcontroller with A/D and watchdog timer

DESCRIPTION

The Philips 8XC550 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. This Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity. The CMOS 8XC550 has the same instruction set as the 80C51.

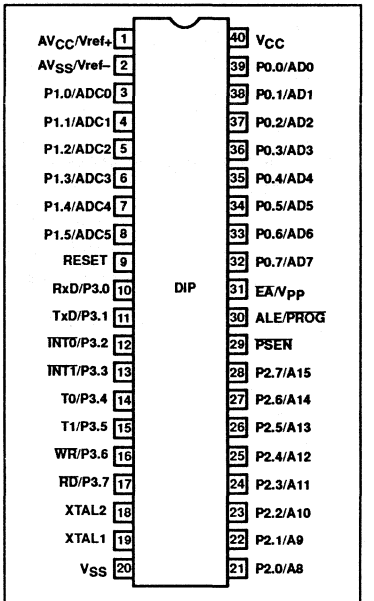
The 8XC550 contains a 4k x 8 EPROM (87C550)/ROM (83C550)/ROMless (80C550 has no program memory on-chip), a 128 x 8 RAM, 8 channels of 8-bit A/D, four 8-bit ports (port 1 is input only), a watchdog timer, two 16-bit counter/timers, a seven-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and an on-chip oscillator and clock circuits.

In addition, the 8XC550 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k x 8 EPROM (87C550)/ ROM (83C550)
  - 128 x 8 RAM
  - 8 channels of 8-bit A/D
  - Two 16-bit counter/timers
  - Watchdog timer
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Three speed ranges at V_{CC} = 5V ±10%
  - 3.5 to 12MHz
  - 3.5 to 16MHz
- Four package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION

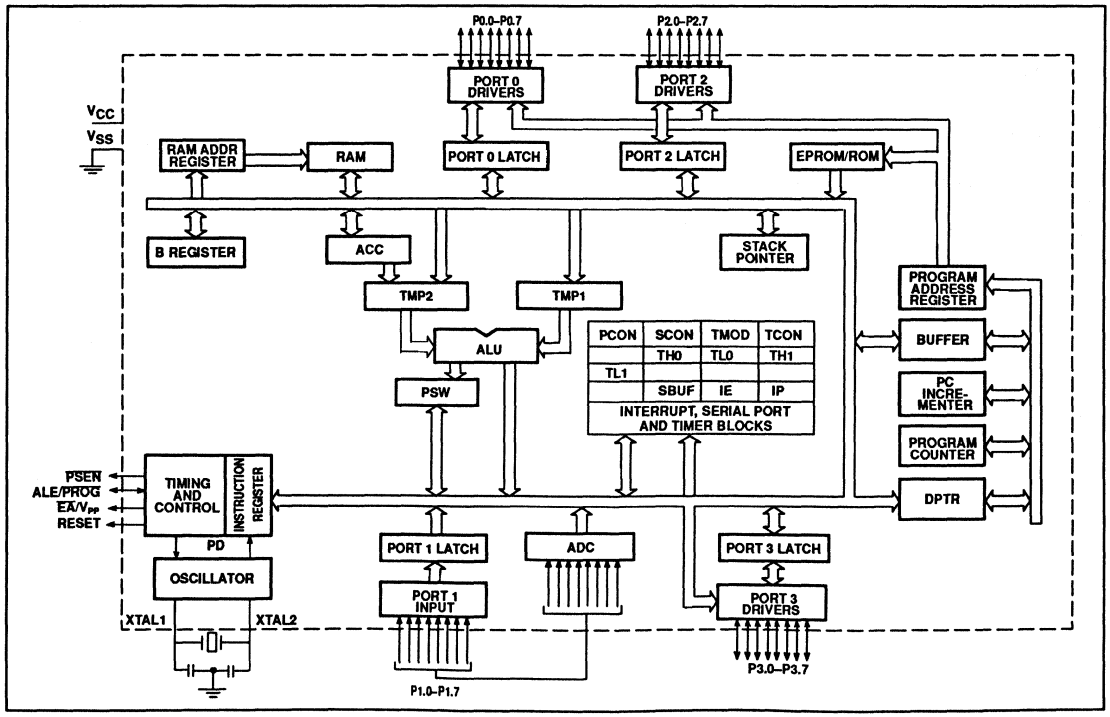


Pin	Function	Pin	Function	Pin	Function
1	AV_{CC}	16	P3.2/INT0	31	P2.6/A14
2	Vref+	17	P3.3/INT1	32	P2.7/A15
3	Vref–	18	P3.4/T0	33	PSEN
4	AV_{SS}	19	P3.5/T1	34	ALE/PROG
5	P1.0/ADC0	20	P3.6/WR	35	EA/V_{PP}
6	P1.1/ADC1	21	P3.7/RD	36	P0.7/AD7
7	P1.2/ADC2	22	XTAL2	37	P0.6/AD6
8	P1.3/ADC3	23	XTAL1	38	P0.5/AD5
9	P1.4/ADC4	24	V_{SS}	39	P0.4/AD4
10	P1.5/ADC5	25	P2.0/A8	40	P0.3/AD3
11	P1.6/ADC6	26	P2.1/A9	41	P0.2/AD2
12	P1.7/ADC7	27	P2.2/A10	42	P0.1/AD1
13	RESET	28	P2.3/A11	43	P0.0/AD0
14	P3.0/RxD	29	P2.4/A12	44	V_{CC}
15	P3.1/TxD	30	P2.5/A13		

PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE AND PACKAGE	FREQUENCY
P80C550BBF	P83C550BBF	P87C550BBF	0 to +70°C, ceramic DIP	3.5 to 12MHz
P80C550EBF	P83C550EBF	P87C550EBF	0 to +70°C, ceramic DIP	3.5 to 16MHz
P80C550BBK	P83C550BBK	P87C550BBK	0 to +70°C, ceramic LCC	3.5 to 12MHz
P80C550EBK	P83C550EBK	P87C550EBK	0 to +70°C, ceramic LCC	0.5 to 16MHz
P80C550BBP	P83C550BBP	P87C550BBP	0 to +70°C, plastic DIP	3.5 to 12MHz
P80C550EBP	P83C550EBP	P87C550EBP	0 to +70°C, plastic DIP	3.5 to 16MHz
P80C550BBA	P83C550BBA	P87C550BBA	0 to +70°C, plastic LCC	3.5 to 12MHz
P80C550EBA	P83C550EBA	P87C550EBA	0 to +70°C, plastic LCC	3.5 to 16MHz
P80C550BFP	P83C550BFP	P87C550BFP	–40 to +85°C, plastic DIP	3.5 to 12MHz
P80C550EFP	P83C550EFP	P87C550EFP	–40 to +85°C, plastic DIP	3.5 to 16MHz
P80C550BFA	P83C550BFA	P87C550BFA	–40 to +85°C, plastic LCC	3.5 to 12MHz
P80C550EFA	P83C550EFA	P87C550EFA	–40 to +85°C, plastic LCC	3.5 to 16MHz
P80C550BFF	P83C550BFF	P87C550BFF	–40 to +85°C, ceramic DIP	3.5 to 12MHz
P80C550EFF	P83C550EFF	P87C550EFF	–40 to +85°C, ceramic LCC	3.5 to 12MHz
P80C550BFK	P83C550BFK	P87C550BFK	–40 to +85°C, ceramic LCC	3.5 to 16MHz
P80C550EFK	P83C550EFK	P87C550EFK	–40 to +85°C, ceramic DIP	3.5 to 16MHz

BLOCK DIAGRAM



Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C552/83C552/87C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C552/83C552/87C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552 — 8k bytes mask programmable ROM
- 80C552 — ROMless version of the 83C552
- 87C552 — 8k bytes EPROM

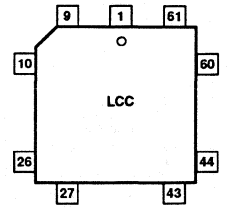
The 8XC552 contains a non-volatile 8k x 8 read-only program memory (83C552) EPROM (87C552), a volatile 256 x 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

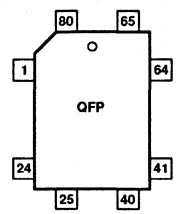
FEATURES

- 80C51 central processing unit
- 8k x 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 x 8 RAM, expandable externally to 64k bytes
- Capable of producing 8 synchronized, timed outputs
- A 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Two speed ranges:
  - 12MHz
  - 16MHz
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION

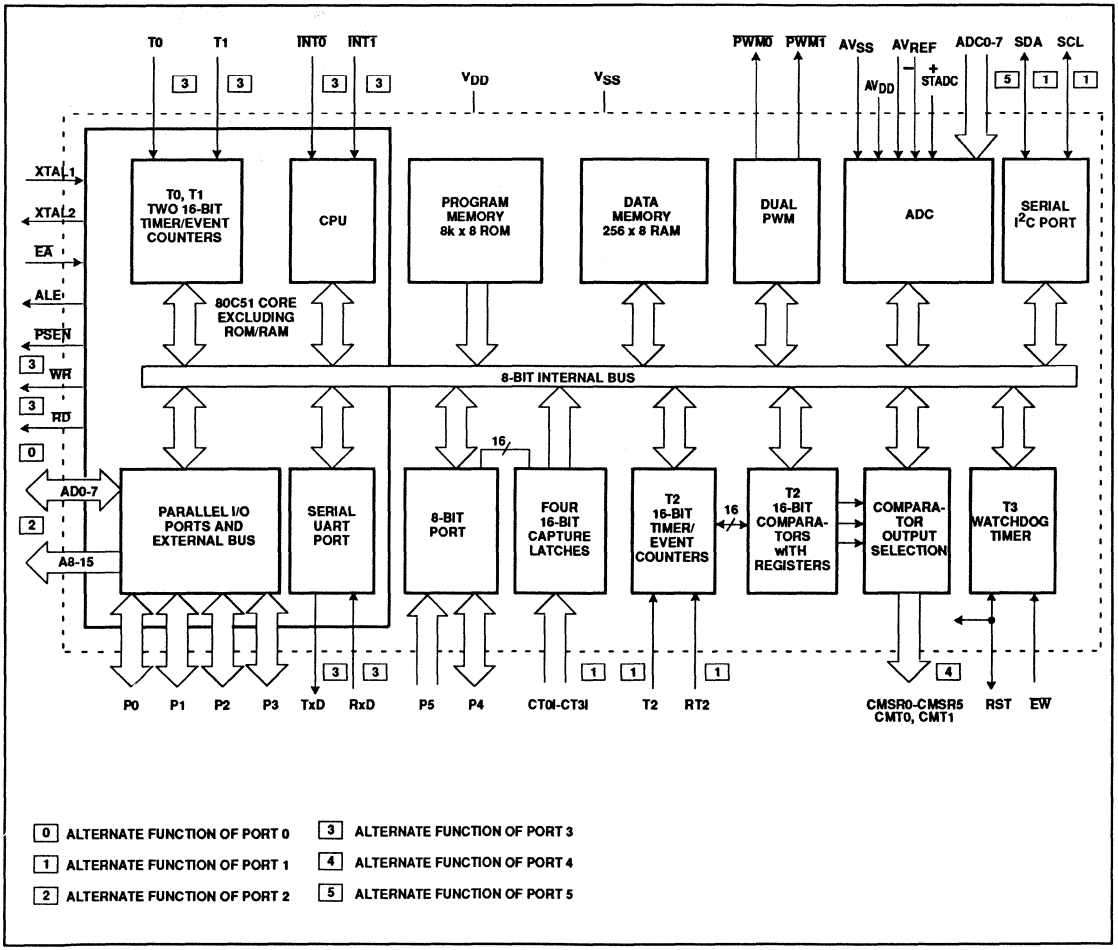


Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWMT}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	45	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE/$\overline{PROG}$
15	RST	49	$\overline{EA}/V_{PP}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref-
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



SEE PAGE 347 FOR QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C562/83C562

Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

The 8XC562 contains a non-volatile 256 x 8 read-only program memory, a volatile 256 X 8 read/write data memory (83C562) (the 80C562 is ROMless), a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

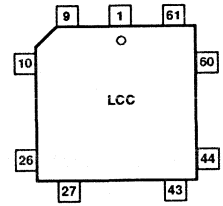
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

For emulation purposes, the 87C552 is recommended.

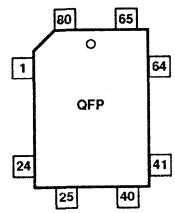
FEATURES

- 80C51 instruction set
- 8k x 8 ROM expandable externally to 64k bytes
- 256 x 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing 8 synchronized, timed outputs
- A 8-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

PIN CONFIGURATION

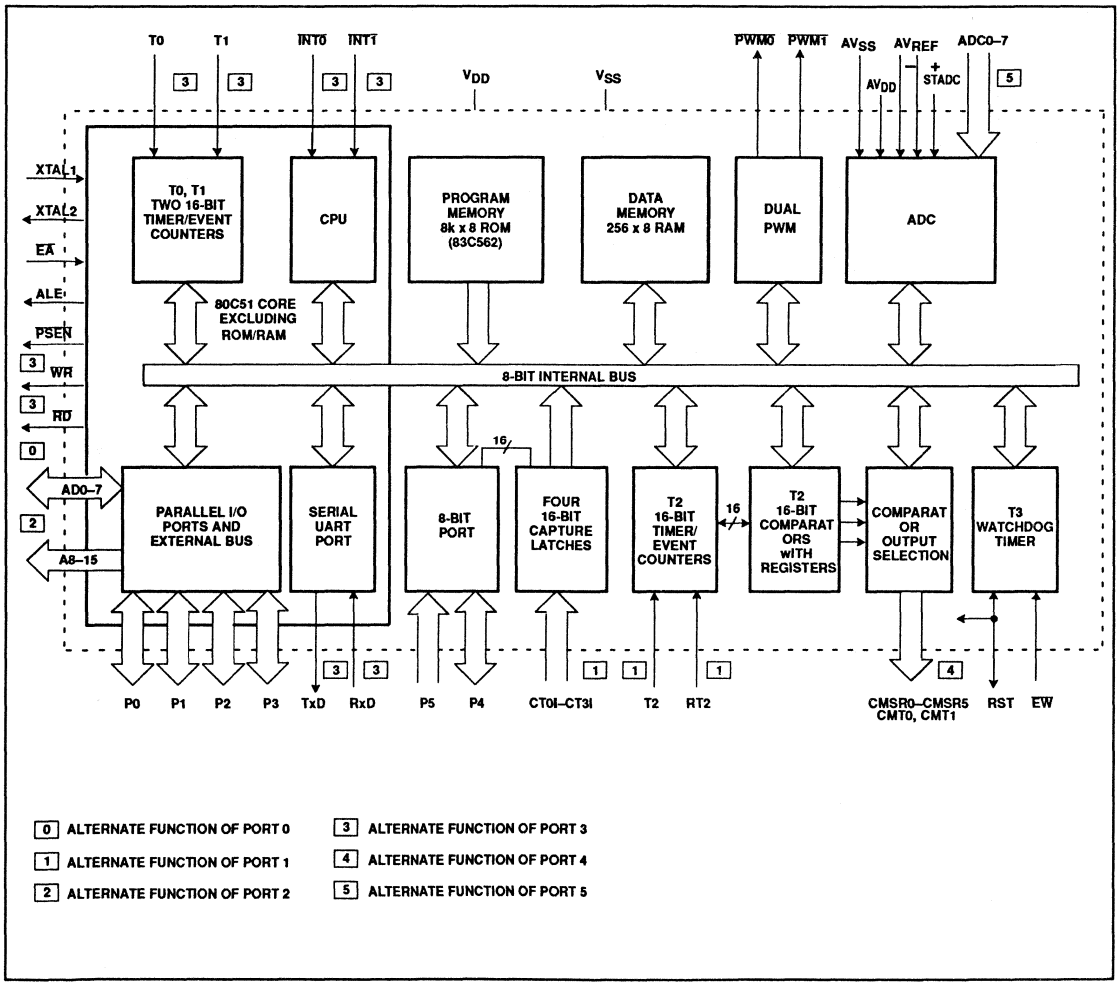


Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



SEE NEXT PAGE FOR QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

80C652/83C652/87C652

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The 80C652/83C652/87C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652/87C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 – 8k bytes mask programmable ROM

80C652 – ROMless version

87C652 – EPROM version

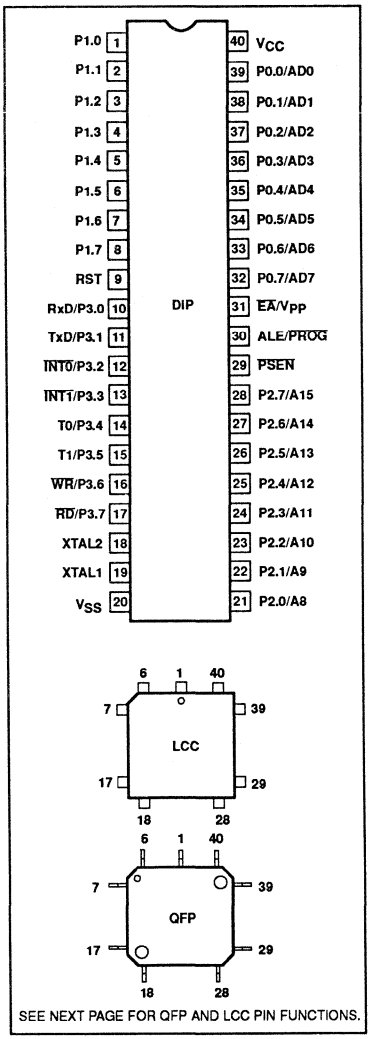
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k X 8 read-only program memory (83C652) EPROM (87C652), a volatile 256 X 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

FEATURES

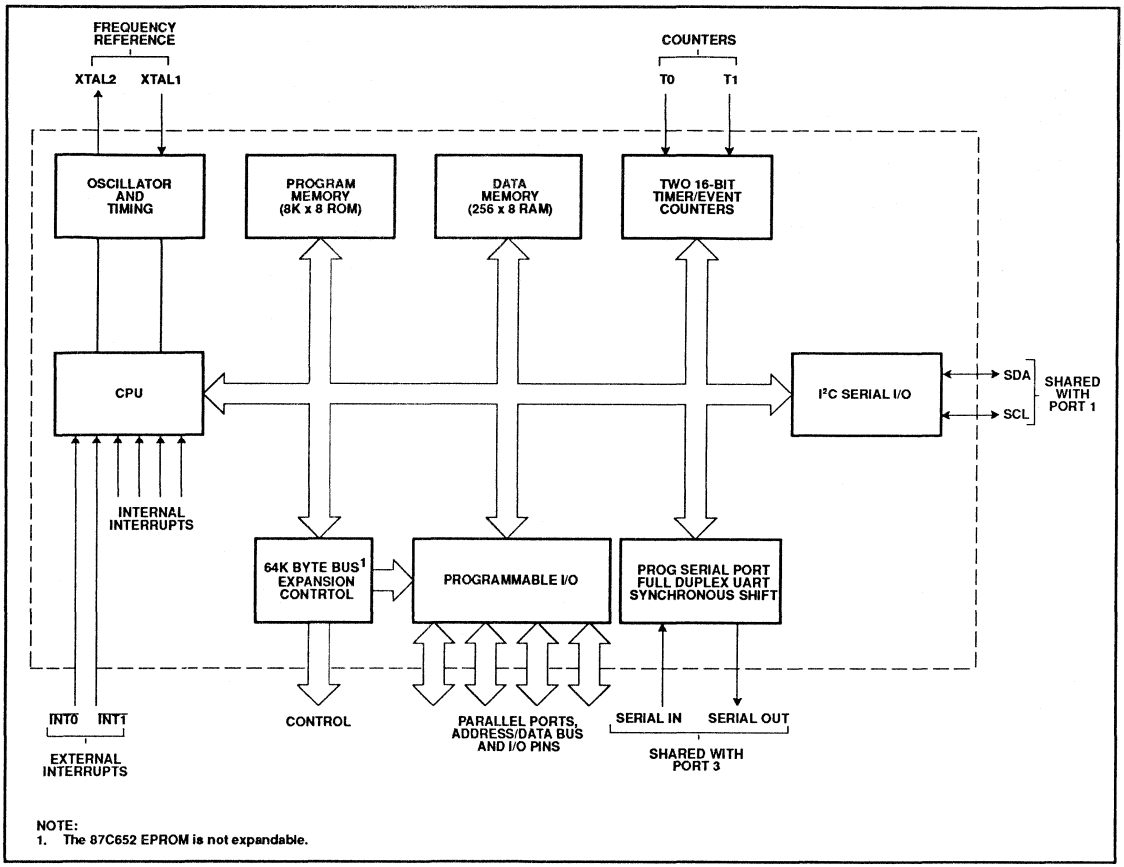
- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes (87C652 EPROM is not expandable)
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



NOTE:
1. The 87C652 EPROM is not expandable.

Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

83C654/87C654

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The 83C654/87C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C654/87C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654 – 16k bytes mask programmable ROM

87C654 – EPROM version

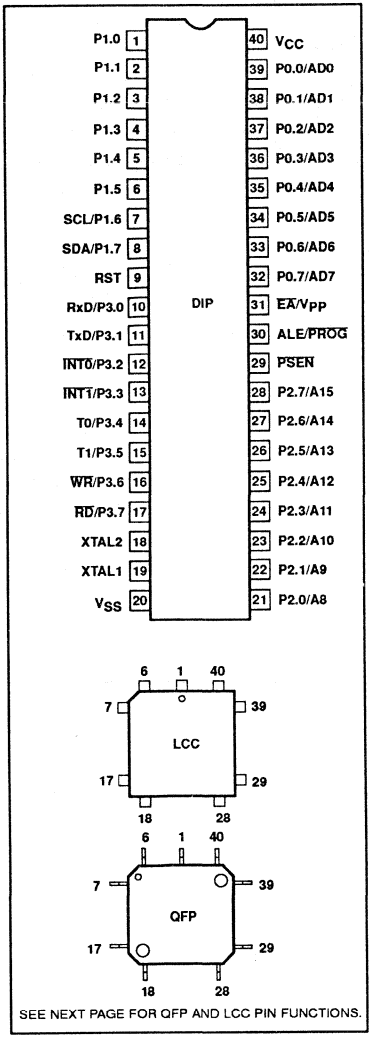
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC654 contains a non-volatile 16k X 8 read-only program memory (83C654) EPROM (87C654), a volatile 256 X 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

FEATURES

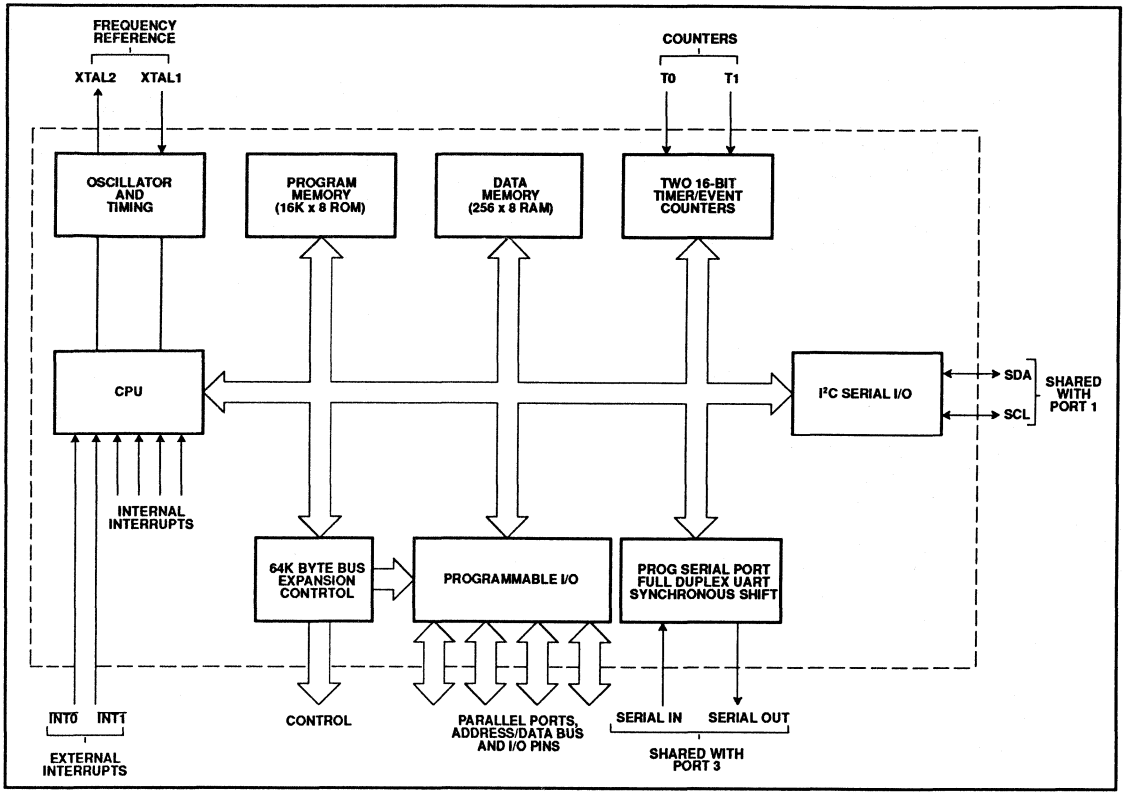
- 80C51 central processing unit
- 16k X 8 ROM expandable externally to 64k bytes
- 256 X 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Components

Date of Issue	June 15, 1990
Status	Product Specification
Application Specific Product	

83C751/87C751

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The Philips 83C751/87C751 offers the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC751 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

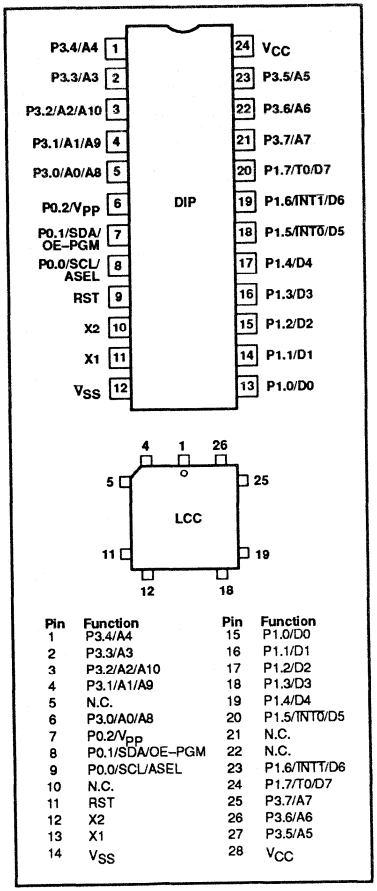
The 8XC751 contains a 2k x 8 ROM (83C751) EPROM (87C751), a 64 x 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, and an on-chip oscillator.

The on-board inter-integrated circuit (I^2C) bus interface allows the 8XC751 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

FEATURES

- 80C51 based architecture
- Inter-Integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 24-pin DIP (300 mil "skinny DIP")
  - 28-pin PLCC
- 87C751 available in erasable quartz lid or one-time programmable plastic packages
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k x 8 ROM (83C751)
  2k x 8 EPROM (87C751)
- 64 x 8 RAM
- 16-bit auto reloadable counter/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

PIN CONFIGURATION

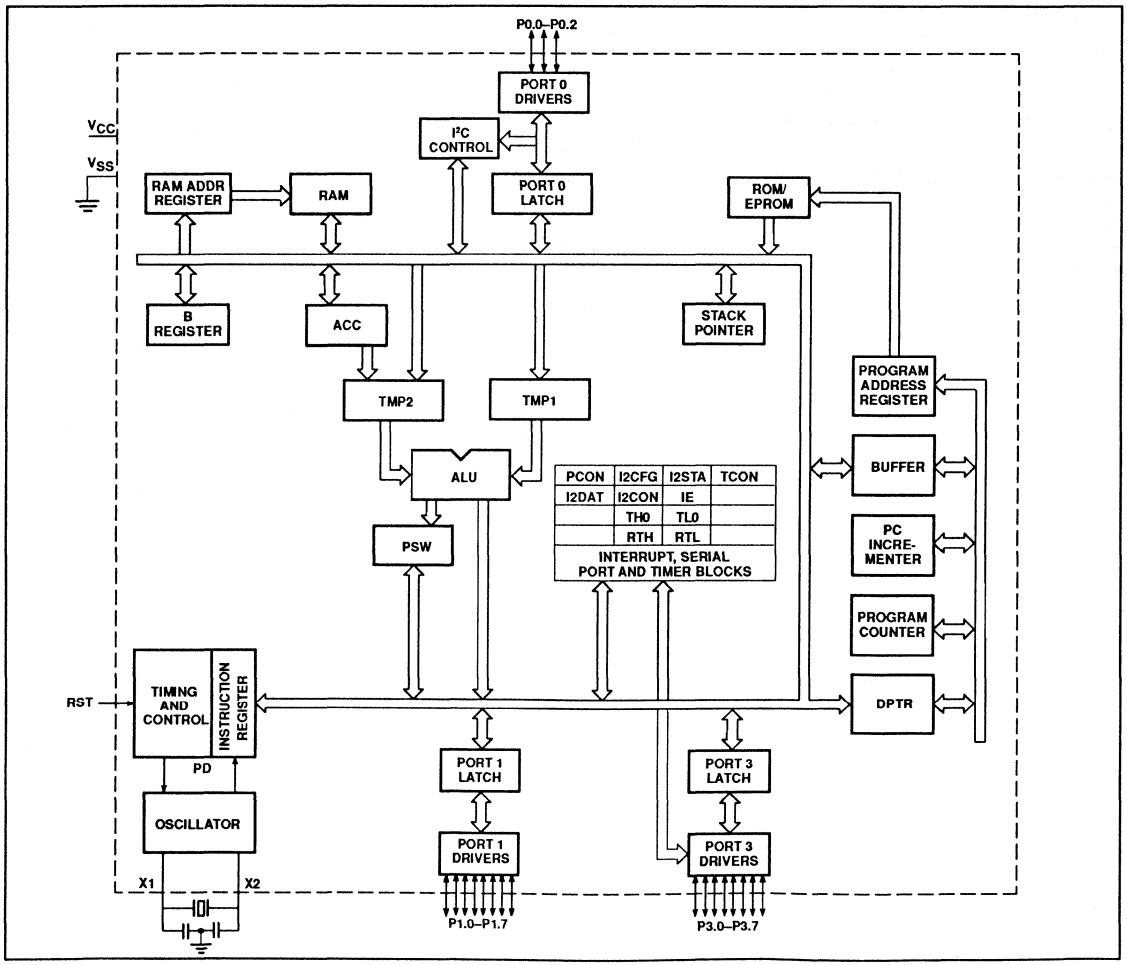


Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/V_{PP}	21	N.C.
8	P0.1/SDA/OE–PGM	22	N.C.
9	P0.0/SCL/ASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	V_{SS}	28	V_{CC}

PART NUMBER SELECTION

ROM	EPROM	SPEED	TEMPERATURE AND PACKAGE
	S87C751–1F24	3.5 to 12MHz	0 to +70°C, ceramic DIP
	S87C751–2F24	3.5 to 12MHz	–40 to +85°C, ceramic DIP
	S87C751–4F24	3.5 to 16MHz	0 to +70°C, ceramic DIP
	S87C751–5F24	3.5 to 16MHz	–40 to +85°C, ceramic DIP
S83C751–1N24	S87C751–1N24	3.5 to 12MHz	0 to +70°C, plastic DIP
S83C751–2N24	S87C751–2N24	3.5 to 12MHz	–40 to +85°C, plastic DIP
S83C751–4N24	S87C751–4N24	3.5 to 16MHz	0 to +70°C, plastic DIP
S83C751–5N24	S87C751–5N24	3.5 to 16MHz	–40 to +85°C, plastic DIP
S83C751–1A28	S87C751–1A28	3.5 to 12MHz	0 to +70°C, plastic LCC
S83C751–2A28	S87C751–2A28	3.5 to 12MHz	–40 to +85°C, plastic LCC
S83C751–4A28	S87C751–4A28	3.5 to 16MHz	0 to +70°C, plastic LCC
S83C751–5A28	S87C751–5A28	3.5 to 16MHz	–40 to +85°C, plastic LCC

BLOCK DIAGRAM



Philips Components

Date of Issue	June 15, 1990
Status	Product Specification
Application Specific Product	

83C752/87C752

CMOS single-chip 8-bit microcontroller with A/D, PWM

DESCRIPTION

The Philips 83C752/87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

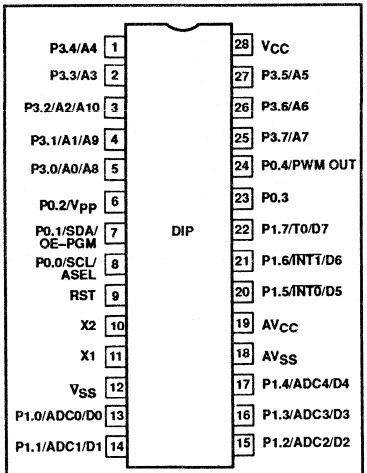
The 8XC752 contains a 2k x 8 ROM (83C752) EPROM (87C752), a 64 x 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

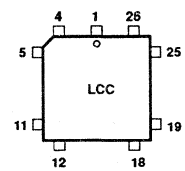
The onboard inter-integrated circuit (I^2C) bus interface allows the 8XC752 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

FEATURES

- Available in erasable quartz lid or One-Time Programmable plastic packages
- 80C51 based architecture
- Inter-integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 28-pin DIP
  - 28-pin PLCC
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k x 8 ROM (83C752) EPROM (87C752)
- 64 x 8 RAM
- 16-bit auto reloadable counter/timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

PIN CONFIGURATION



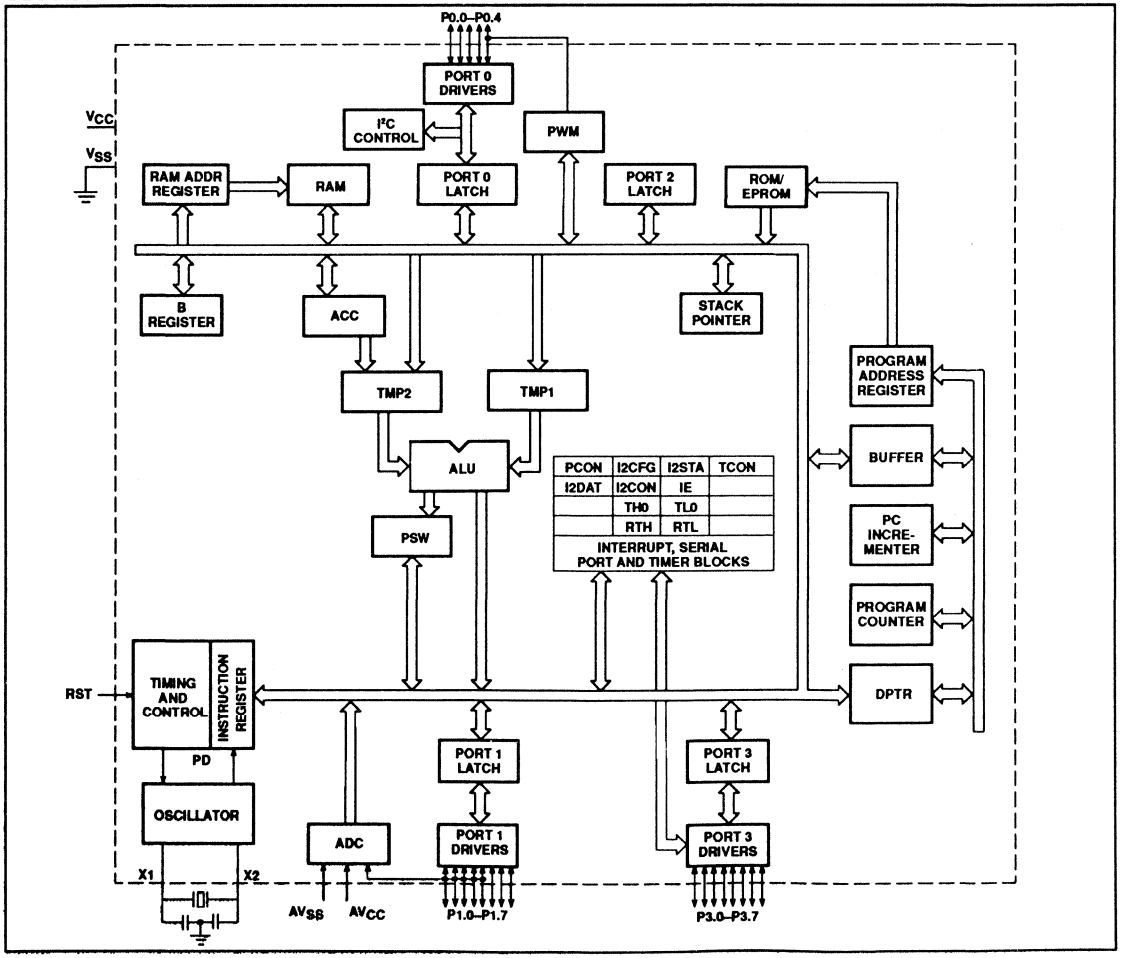


Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV_{SS}
5	P3.0/A0/A8	19	AV_{CC}
6	$P0.2/V_{PP}$	20	P1.5/INT0/D5
7	P0.1/SDA/OE–PGM	21	P1.6/INT1/D6
8	P0.0/SCL/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V_{SS}	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V_{CC}

PART NUMBER SELECTION

ROM	EPROM	SPEED	TEMPERATURE AND PACKAGE
	87C752–1F28	3.5 to 12MHz	0 to +70°C, ceramic DIP
	87C752–2F28	3.5 to 12MHz	–40 to +85°C, ceramic DIP
	87C752–4F28	3.5 to 16MHz	0 to +70°C, ceramic DIP
	87C752–5F28	3.5 to 16MHz	–40 to +85°C, ceramic DIP
83C752–1N28	87C752–1N28	3.5 to 12MHz	0 to +70°C, plastic DIP
83C752–2N28	87C752–2N28	3.5 to 12MHz	–40 to +85°C, plastic DIP
83C752–4N28	87C752–4N28	3.5 to 16MHz	0 to +70°C, plastic DIP
83C752–5N28	87C752–5N28	3.5 to 16MHz	–40 to +85°C, plastic DIP
83C752–1A28	87C752–1A28	3.5 to 12MHz	0 to +70°C, plastic LCC
83C752–2A28	87C752–2A28	3.5 to 12MHz	–40 to +85°C, plastic LCC
83C752–4A28	87C752–4A28	3.5 to 16MHz	0 to +70°C, plastic LCC
83C752–5A28	87C752–5A28	3.5 to 16MHz	–40 to +85°C, plastic LCC
83C752–6A28	87C752–6A28	3.5 to 12MHz	–55 to +125°C, plastic LCC
83C752–6F28	87C752–6F28	3.5 to 12MHz	–55 to +125°C, ceramic DIP
83C752–6N28	87C752–6N28	3.5 to 12MHz	–55 to +125°C, plastic DIP

BLOCK DIAGRAM



Philips Components

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C851/83C851

CMOS single-chip 8-bit microcontroller with on-chip EEPROM

DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

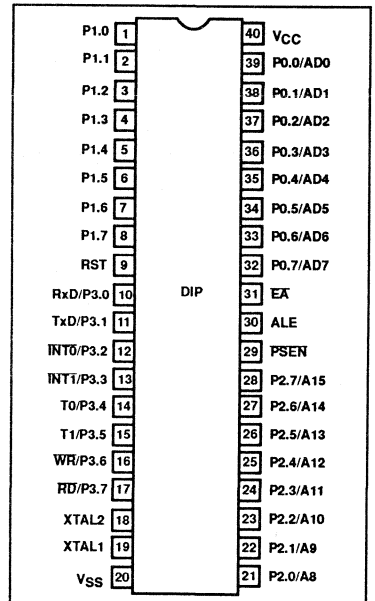
The 80C851/83C851 contains a 4k x 8 ROM with mask-programmable ROM code protection, a 128 x 8 RAM, 256 x 8 EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k x 8 ROM
  - 128 x 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile 256 x 8-bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 10,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 12MHz
- Two temperature ranges
- Three package styles

PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	NC	15	INT1/P3.3	30	P2.6/A14
2	P1.0	16	T0/P3.4	31	P2.7/A15
3	P1.1	17	T1/P3.5	32	PSEN
4	P1.2	18	WR/P3.6	33	ALE
5	P1.3	19	RD/P3.7	34	NC
6	P1.4	20	XTAL2	35	EA
7	P1.5	21	XTAL1	36	P0.7/AD7
8	P1.6	22	V_{SS}	37	P0.6/AD6
9	P1.7	23	NC	38	P0.5/AD5
10	RST	24	P2.0/A8	39	P0.4/AD4
11	RxD/P3.0	25	P2.1/A9	40	P0.3/AD3
12	NC	26	P2.2/A10	41	P0.2/AD2
13	TxD/P3.1	27	P2.3/A11	42	P0.1/AD1
14	INT0/P3.2	28	P2.4/A12	43	P0.0/AD0
		29	P2.5/A13	44	V_{CC}

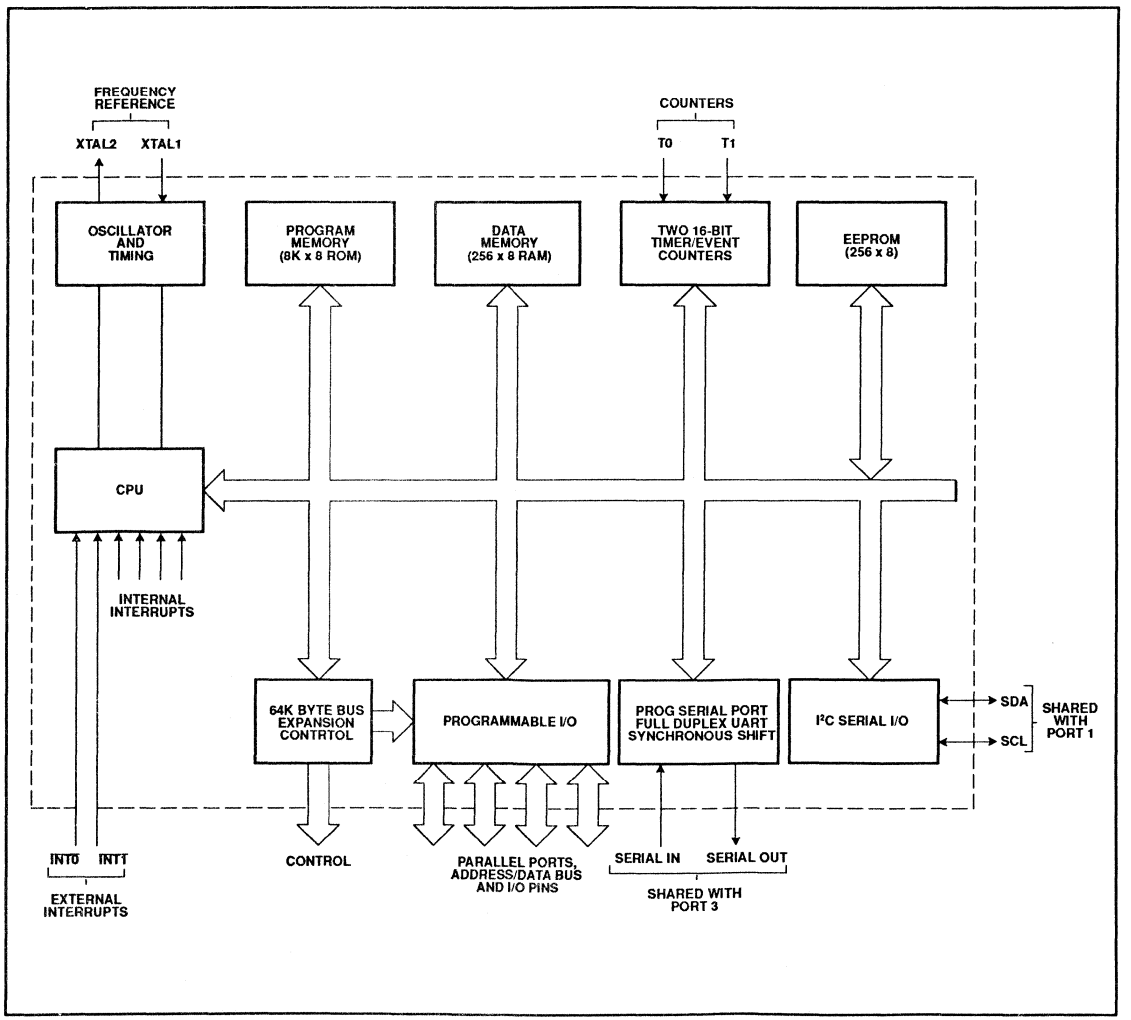
CMOS single-chip EEPROM 8-bit microcontroller

80C851/83C851

PART NUMBER SELECTION

PHILIPS		PHILIPS COMPONENTS-SIGNETICS		TEMPERATURE AND PACKAGE	FREQUENCY (MHz)
ROMless Version	ROM Version	ROMless Version	ROM Version		
PCB80C851P	PCB83C851P	S80C851-1N40	S83C851-1N40	0 to +70°C plastic DIP	1.2 to 12
PCB80C851WP	PCB83C851WP	S80C851-1A44	S83C851-1A44	0 to +70°C plastic LCC	1.2 to 12
PCB80C851H	PCB83C851H	S80C851-1B44	S83C851-1B44	0 to +70°C plastic QFP	1.2 to 12
PCF80C851P	PCF83C851P	S80C851-2N40	S83C851-2N40	–40 to +85°C plastic DIP	1.2 to 12
PCF80C851WP	PCF83C851WP	S80C851-2A44	S83C851-2A44	–40 to +85°C plastic LCC	1.2 to 12
PCF80C851H	PCF83C851H	S80C851-2B44	S83C851-2B44	–40 to +85°C plastic QFP	1.2 to 12

BLOCK DIAGRAM



NE570/571/SA571
Compandor

Product Specification

Linear Products

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|avg}{R_1}$$

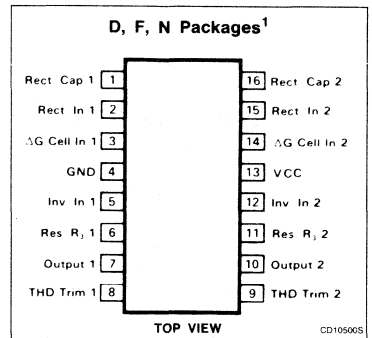
FEATURES

- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

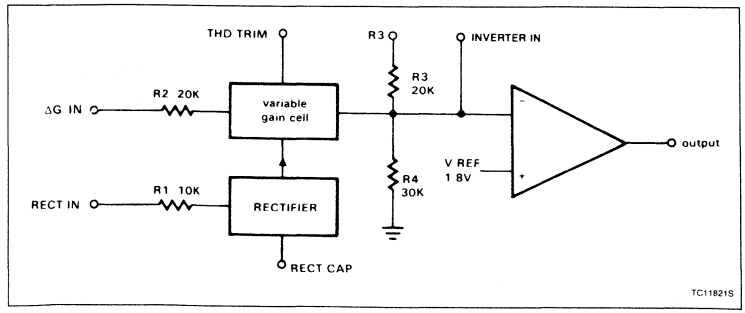


NOTE:
1. SOL - Released in Large SO Package Only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	-40°C to +85°C	SA571F
16-Pin Plastic DIP	-40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz − 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals [$V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = −30dBm, V_1 = 0dB		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final};\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

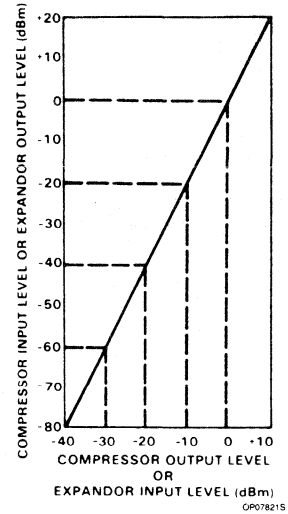
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ± 20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

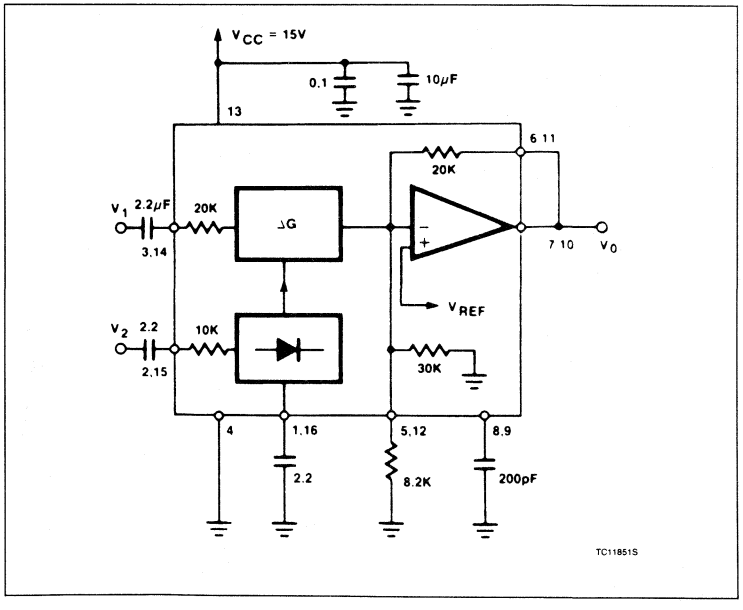
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

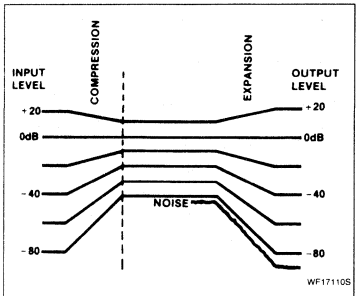


Figure 1. Restricted Dynamic Range Channel

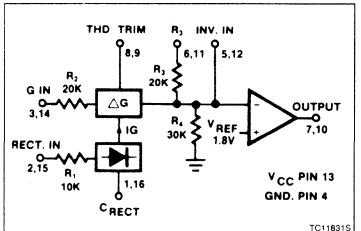


Figure 2. Chip Block Diagram (1 of 2 Channels)

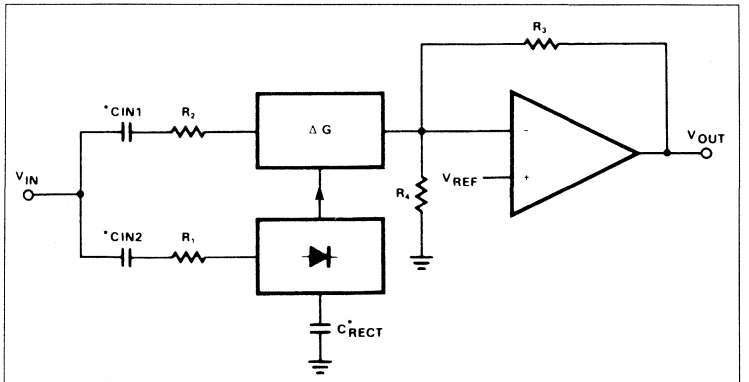
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k}\right) 1.8V$$



NOTES:

$$GAIN = \frac{2\ R_3\ V_{IN}\ (avg.)}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

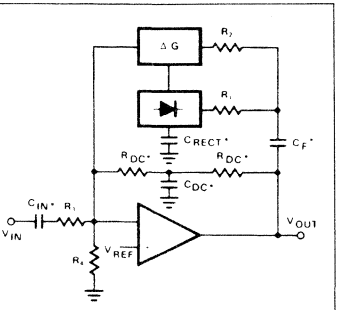
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4} V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k} \right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\ (avg)} \right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4. Basic Compressor

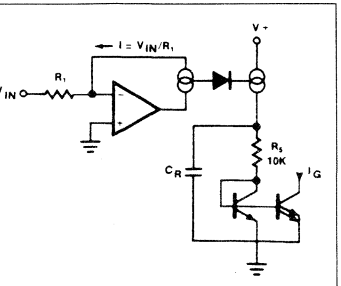
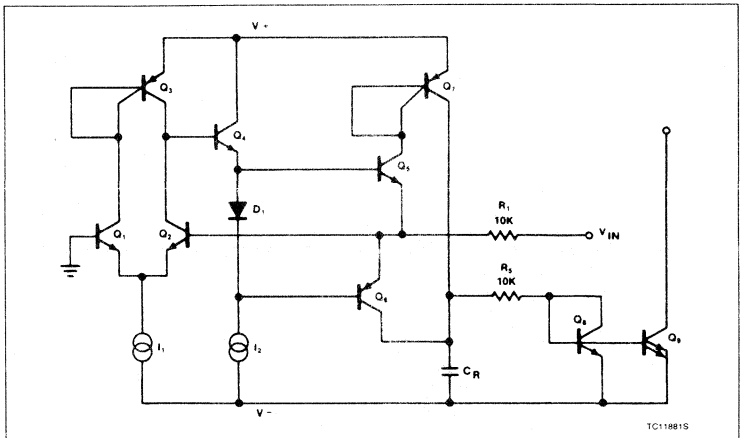


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2 \frac{V_{IN}\ avg}{R1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

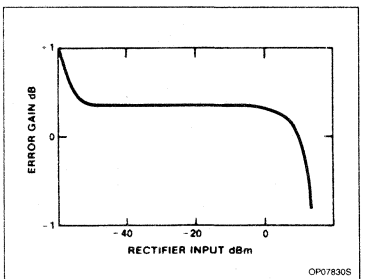


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

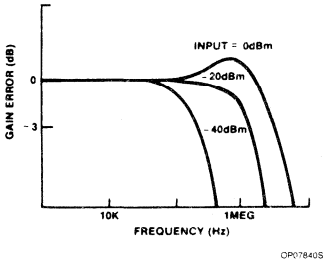


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} (= V_{IN}/R_2) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

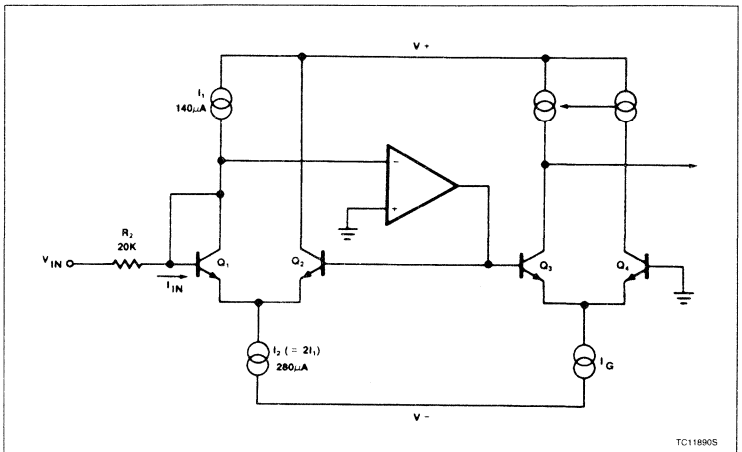
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

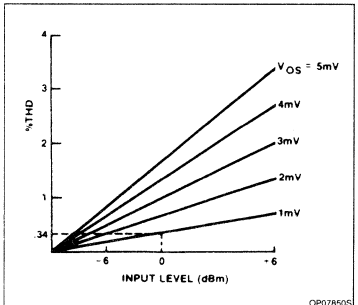


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

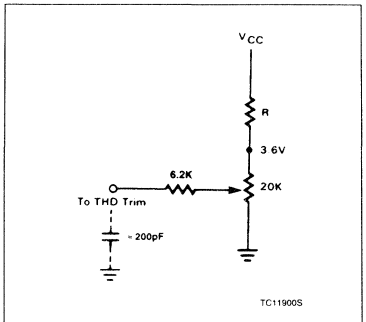


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

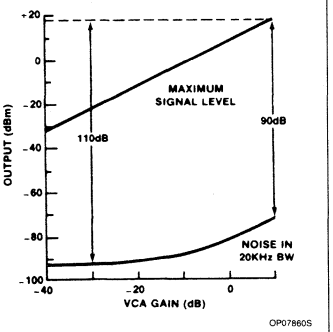


Figure 12. Dynamic Range of NE570

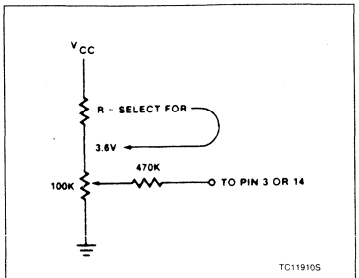


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

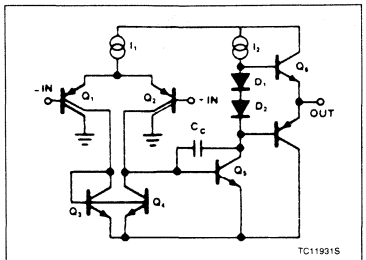


Figure 14. Operational Amplifier

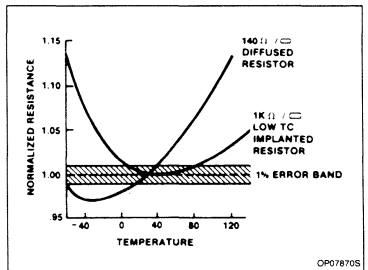


Figure 15. Resistance vs Temperature

NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

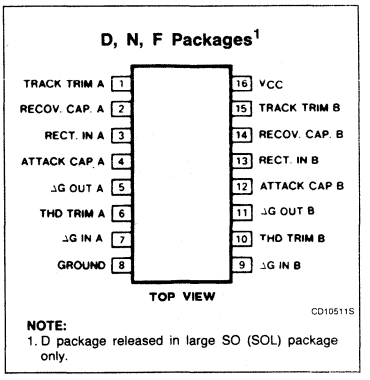
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

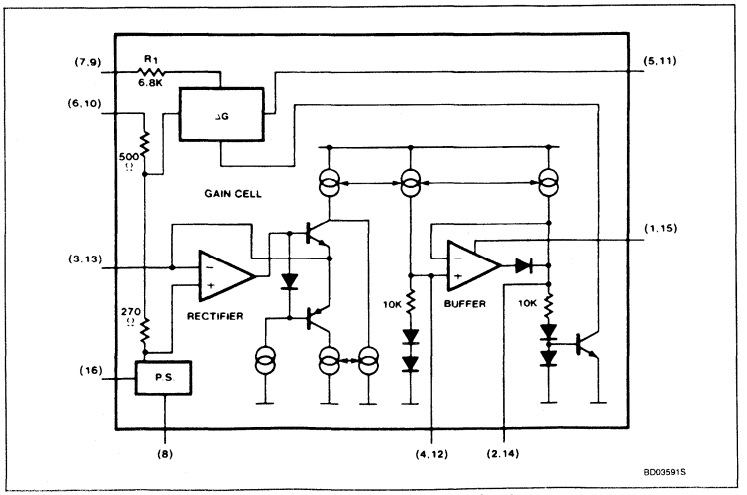
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

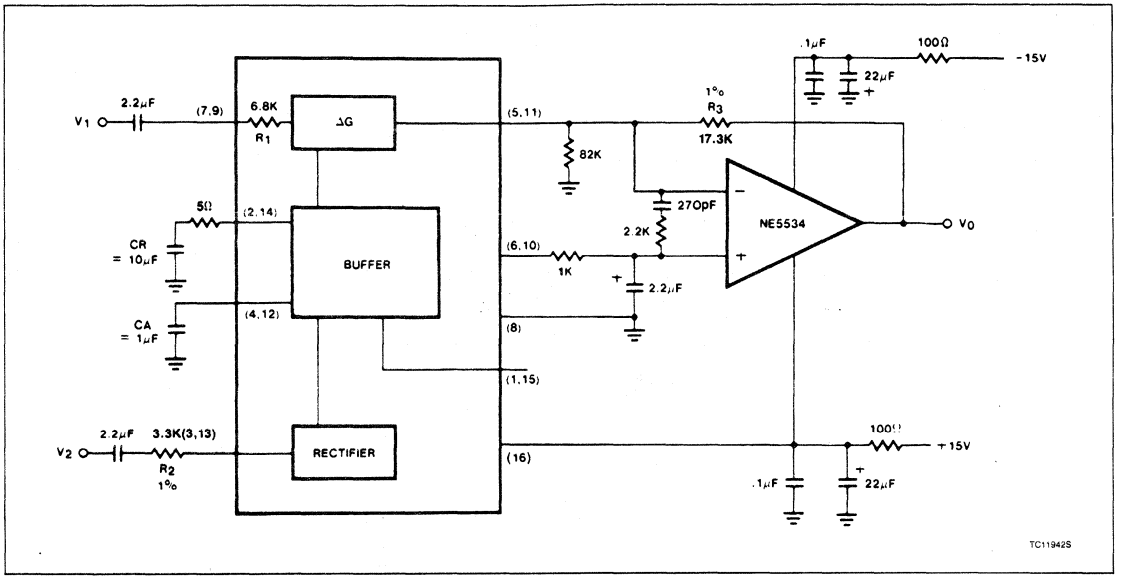
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 −40 to +85	 °C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 − 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)]dB − V_2dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = −30dB V_1 = 0dB		 ±0.2 ±0.5	 −1.5 +0.8		 ±0.2 ±0.5	 −2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\triangle V_{BE_{Q3-Q4}} = \triangle_{BE_{Q1-Q2}}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

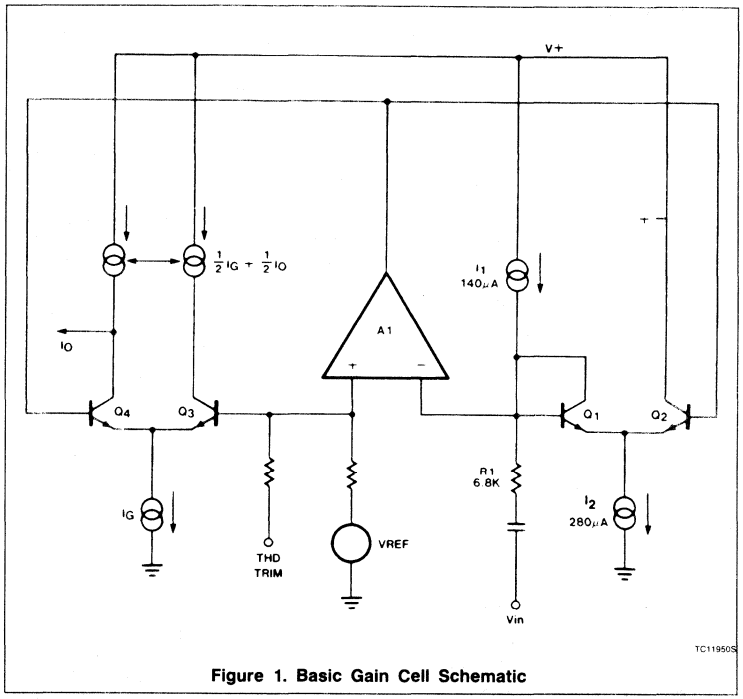


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

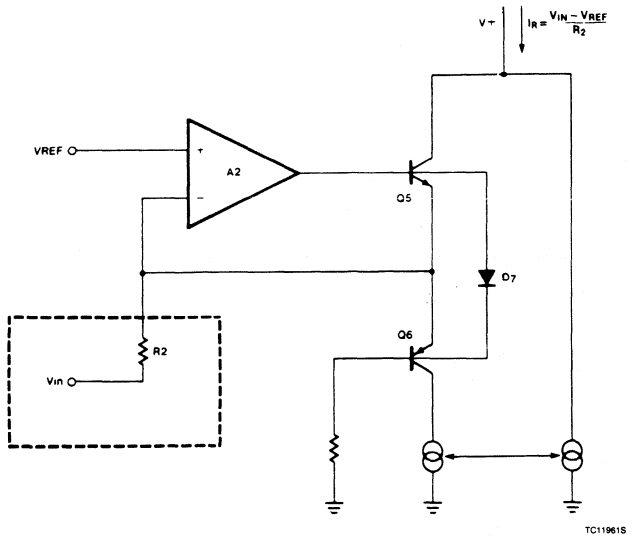


Figure 2. Simplified Rectifier Schematic

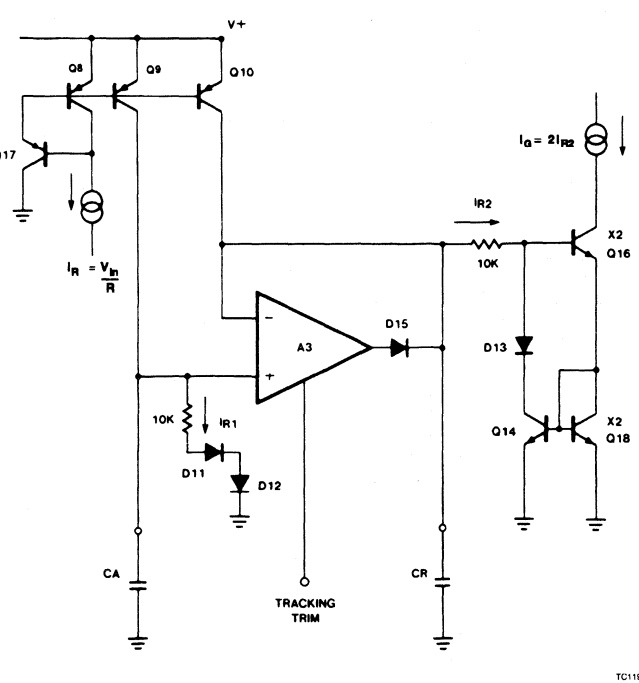


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR · R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

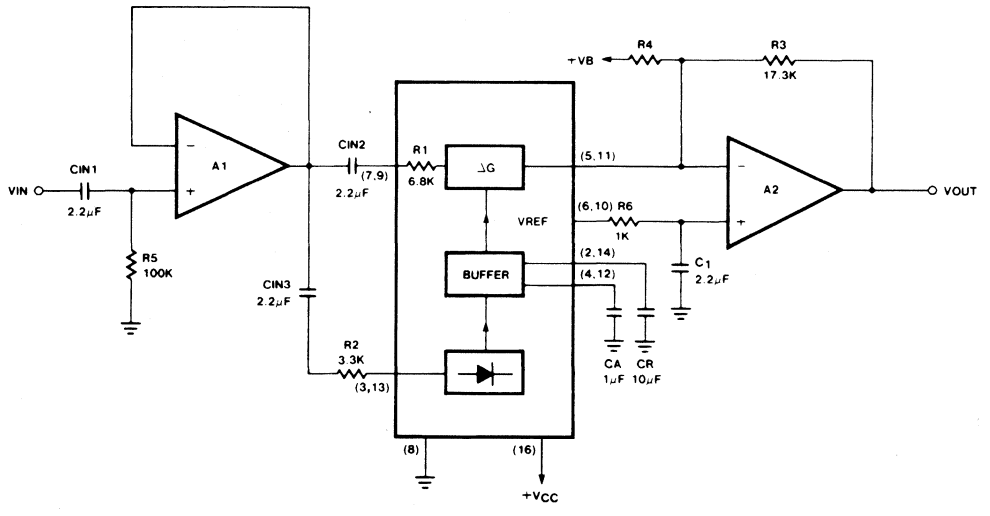


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right)$$

$$- V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

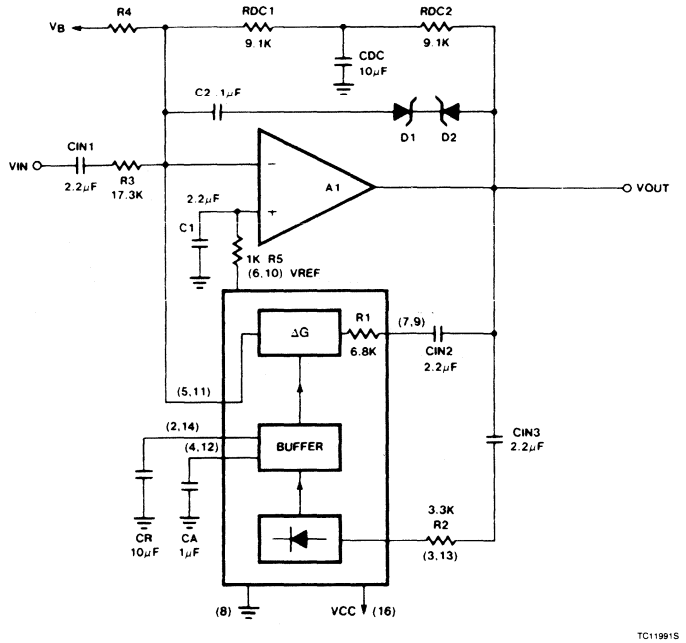


Figure 5. Basic Compressor Schematic

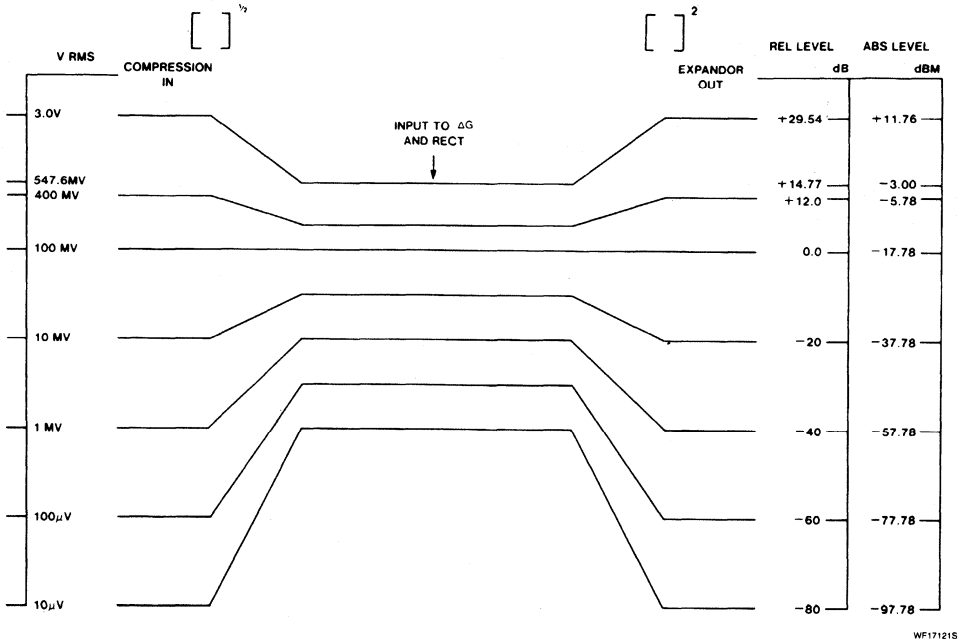


Figure 6. NE572 System Level

Low power compandor

NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

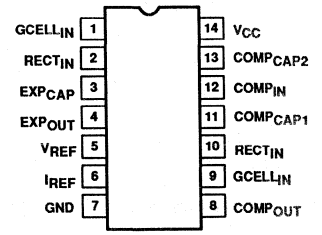
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION

D and N Packages



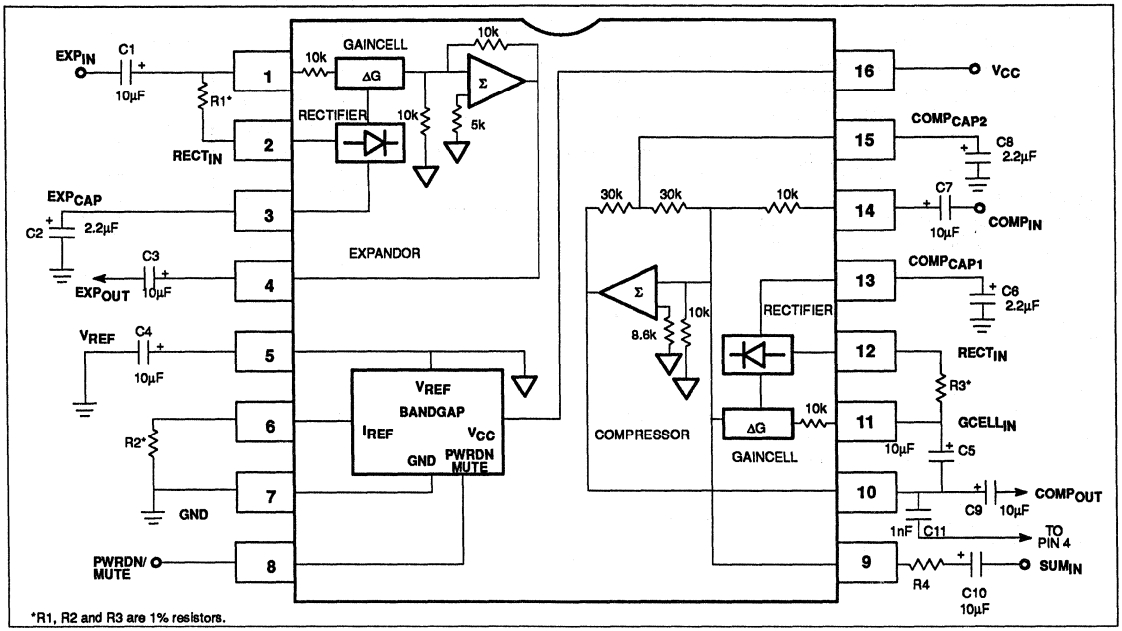
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE576N
14-Pin Plastic SO	0 to +70°C	NE576D
14-Pin Plastic DIP	–40 to +85°C	SA576N
14-Pin Plastic SO	–40 to +85°C	SA576D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

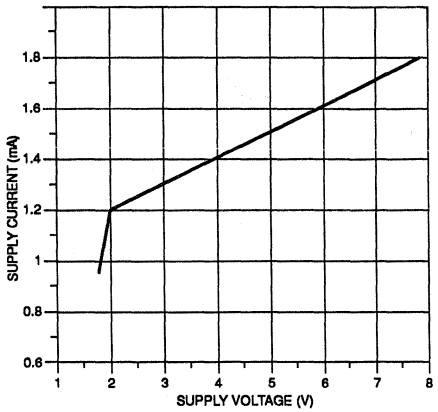
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA576			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

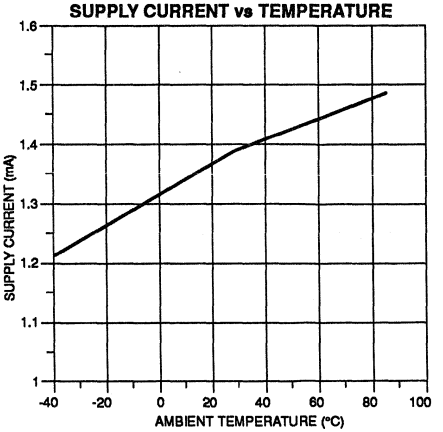
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz

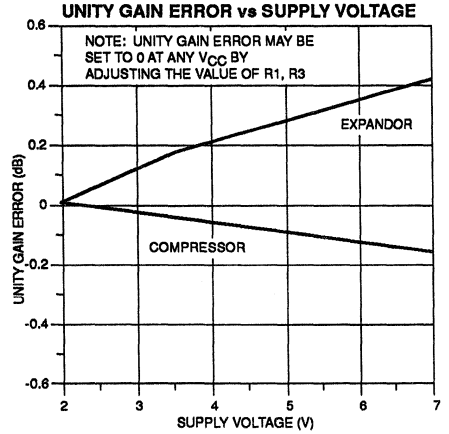
SUPPLY CURRENT vs SUPPLY VOLTAGE



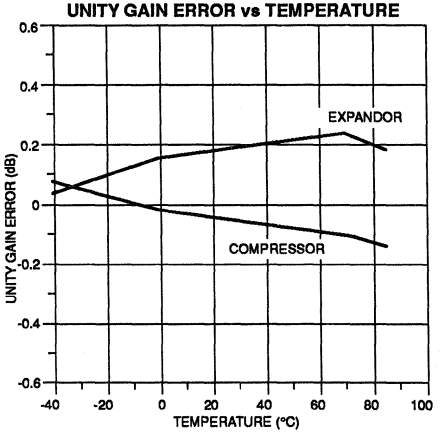
SUPPLY CURRENT vs TEMPERATURE



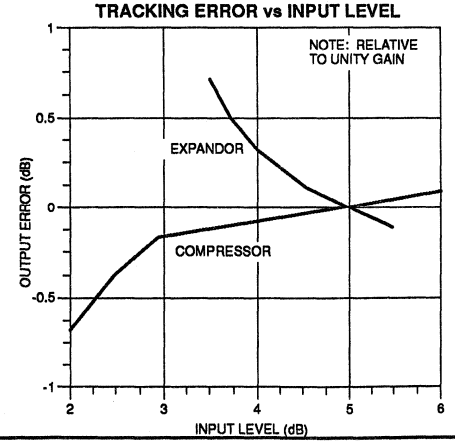
UNITY GAIN ERROR vs SUPPLY VOLTAGE



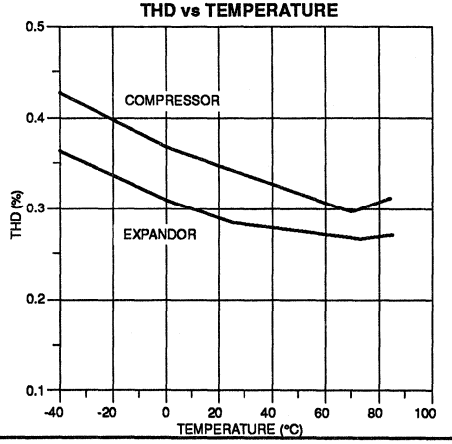
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



NE5240
Dolby Digital Audio Decoder

Preliminary Specification

DESCRIPTION

The NE5240 is a two channel decoder for the Dolby Digital Audio System. *The IC includes input latches to separate two channels of audio and control data, a precision internal voltage reference, and digital/analog signal processing circuitry for each channel. The IC design is implemented in a bipolar process to achieve low noise, low distortion, and wide dynamic range.

NOTE:

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and applications information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

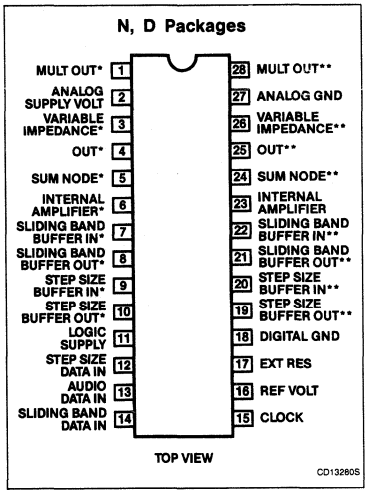
FEATURES

- **Wide dynamic range — 85dB**
- **Low distortion 0.05% @ 1kHz, −10dB**
- **TTL and CMOS compatible logic inputs**
- **Audio bandwidth — 30Hz to 15kHz**

APPLICATIONS

- **High quality digital transmission of audio data**
- **Satellite reception**
- **Cable TV**
- **Microwave distribution systems**

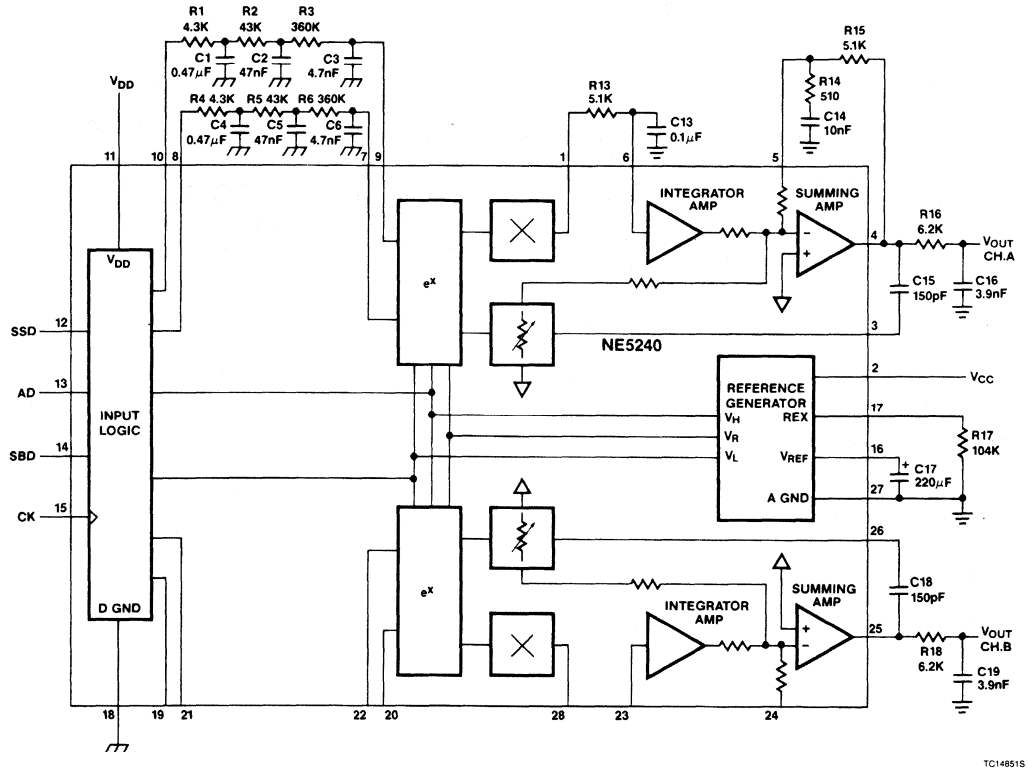
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin SO	0 to +70°C	NE5240D
28-Pin Plastic DIP	0 to +70°C	NE5240N

BLOCK DIAGRAM



NOTE:
One channel of the application shown with external components.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Analog supply voltage	+15	V
V_{DD}	Logic supply voltage	+7	V
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

All specifications are at $T_A = 25°C$, $V_{CC} = 12V$, $V_{DD} = 5V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Analog voltage supply range		10	12	14	V
V_{DD}	Logic voltage supply range		4.5	5	5.5	V
I_{CC}	Supply current	$V_{CC} = 12V$	10	24	35	mA
I_{DD}	Supply current	$V_{DD} = 5V$	5	12	18	mA
V_{IH}	Input voltage high		2		5	V
V_{IL}	Input voltage low		0		0.8	V
I_{IL}	Input current low	$V_{DD} = 4.5V$		10	100	μA
I_{IH}	Input current high			1	100	μA
t_S	Setup time		150			ns
t_H	Hold time		150			ns
I_B	Input buffers, Pins 7, 9, 20, 22	$V_{IN} = 2.0V$			100	nA
R_L	Summing amp output load		5			kΩ
V_{OS}	Output offset voltage			0.1	0.6	V
V_{OS}	Output offset change	10%-SBD-70%		±5	±20	mV
V_{REF}	Reference voltage		5.5	$0.5V_{CC}$	6.5	V

AC ELECTRICAL CHARACTERISTICS

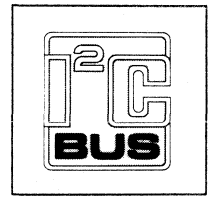
SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			Min	Typ	Max	
V_O	Full-Scale output, 0dB	f = 100Hz		1.8		V_{RMS}
	Absolute output level	f = 1kHz, SSD = 40%	93	118	150	mV_{RMS}
	Channel balance	f = 1kHz, 20%-SSD-70%	−1.5		1.5	dB
	Step-Size linearity	f = 1kHz, 20%-SSD-70%	−1.5		1.5	dB
	Step-Size linearity	f = 100Hz, SSD = 90%	−2.5		1.0	dB
f_R	Frequency response	f = 2kHz, SBD = 10%	−1.0		1.0	dB
f_R	Frequency response	f = 5kHz, SBD = 20%	−1.0		1.0	dB
f_R	Frequency response	f = 7kHz, SBD = 30%	−1.0		1.0	dB
f_R	Frequency response	f = 8kHz, SBD = 40%	−1.0		1.0	dB
f_R	Frequency response	f = 10kHz, SBD = 50%	−1.0		1.0	dB
f_R	Frequency response (all WRT 100Hz)	f = 12kHz, SBD = 60% f = 14kHz, SBD = 70%	−1.0 −1.5		1.0 1.5	dB dB
S/N	Dynamic range	SSD = 70%, CCIR/ARM	80	85		dB
THD	Harmonic distortion	f = 1kHz, −3dB		0.1	0.5	%
THD	Harmonic distortion Channel separation	f = 1kHz, −10dB f = 1kHz, 0dB	 60	0.05 75	0.2	% dB
PSRR	Power supply rejection ratio[1]	f = 1kHz		60		dB

NOTES:
1. PSRR depends on value of capacitor on Pin 16.
2. The duty cycle of SSD and SBD control data is 10%, unless otherwise noted.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	December 1990

PC.8582 Family
256 x 8-BIT CMOS EEPROMS with I²C-BUS interface
FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK



GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient.

Chip select is accomplished by the three address inputs, which also allows up to eight devices to be connected to the I²C-bus.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, and PCF8581
- Mini-pack package for SMD technology.

QUICK SELECTION GUIDE

TYPE	PCF8582A	PCA8582B	PCF8582C	PCD8582D	PCF8582E
extended temperature range	•	•	•	–	•
extended voltage supply range	–	–	•	•	–
no external RC required	–	–	•	•	•
single bit error correction for extended number of erase/write cycles	–	•	•	•	•

256 x 8-BIT CMOS EEPROMS with I²C-BUS interface

PC.8582 Family

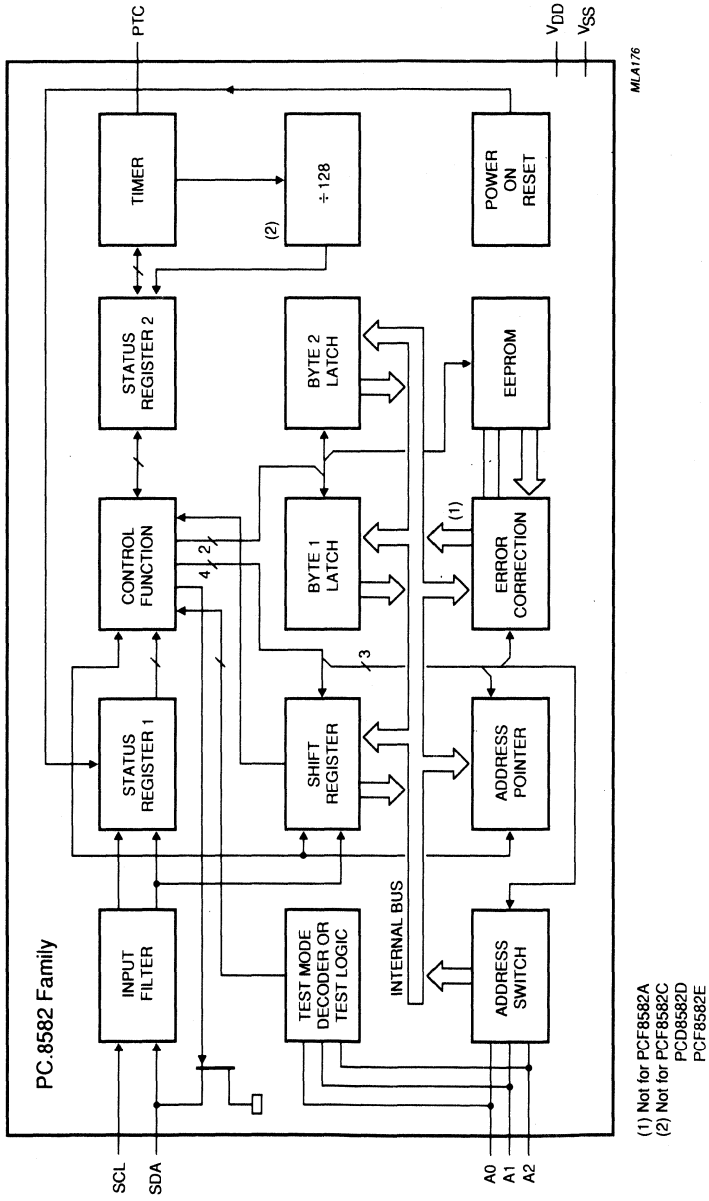


Fig.1 Block diagram.

(1) Not for PCF8582A.

(2) Not for PCF8582C, PCD8582D or PCF8582E.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:

- The PCB80C49 with resident mask programmed 2 K x 8 ROM, 128 x 8 RAM.
- The PCB80C39 without resident program memory for use with external EPROM/ROM, 128 x 8 RAM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O, and to test individual individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.
An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power down mode is provided.
For further detailed information see the 8048 family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption
- Available with extended temperature ranges: (PCB version) 0 to + 70 °C
  (PCF version) −40 to + 85 °C
  (PCA version) −40 to + 110 °C
- Frequency range: 1 to 15 MHz for all temperature ranges

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB/F/A80C39/C49P: 40-lead DIL; plastic (SOT129).
PCB/F/A80C39/C49WP: 44-lead PLCC; plastic leaded chip carrier (SOT187AA).

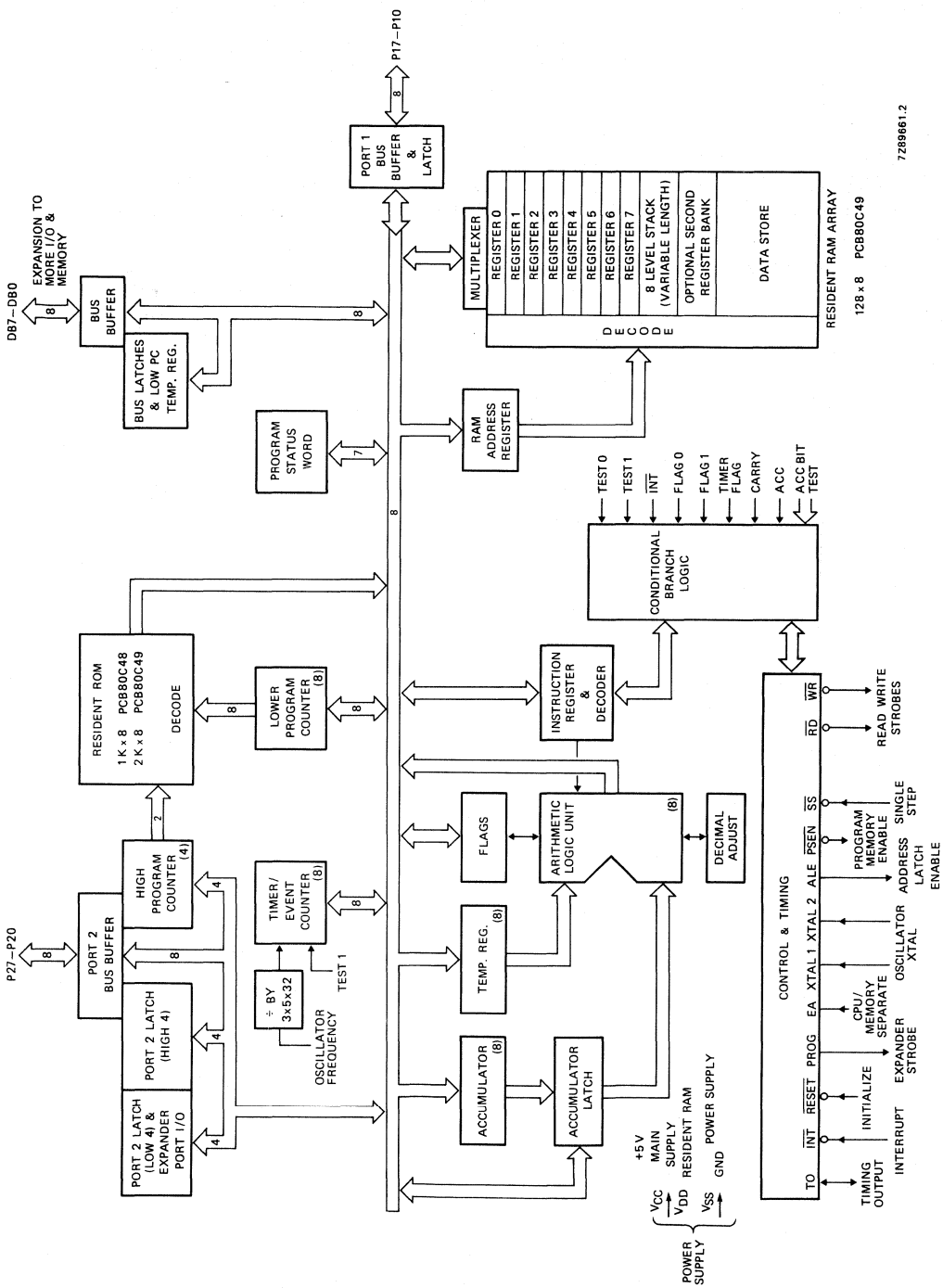


Fig. 1 Block diagram.

I²C-BUS CONTROLLER

GENERAL DESCRIPTION

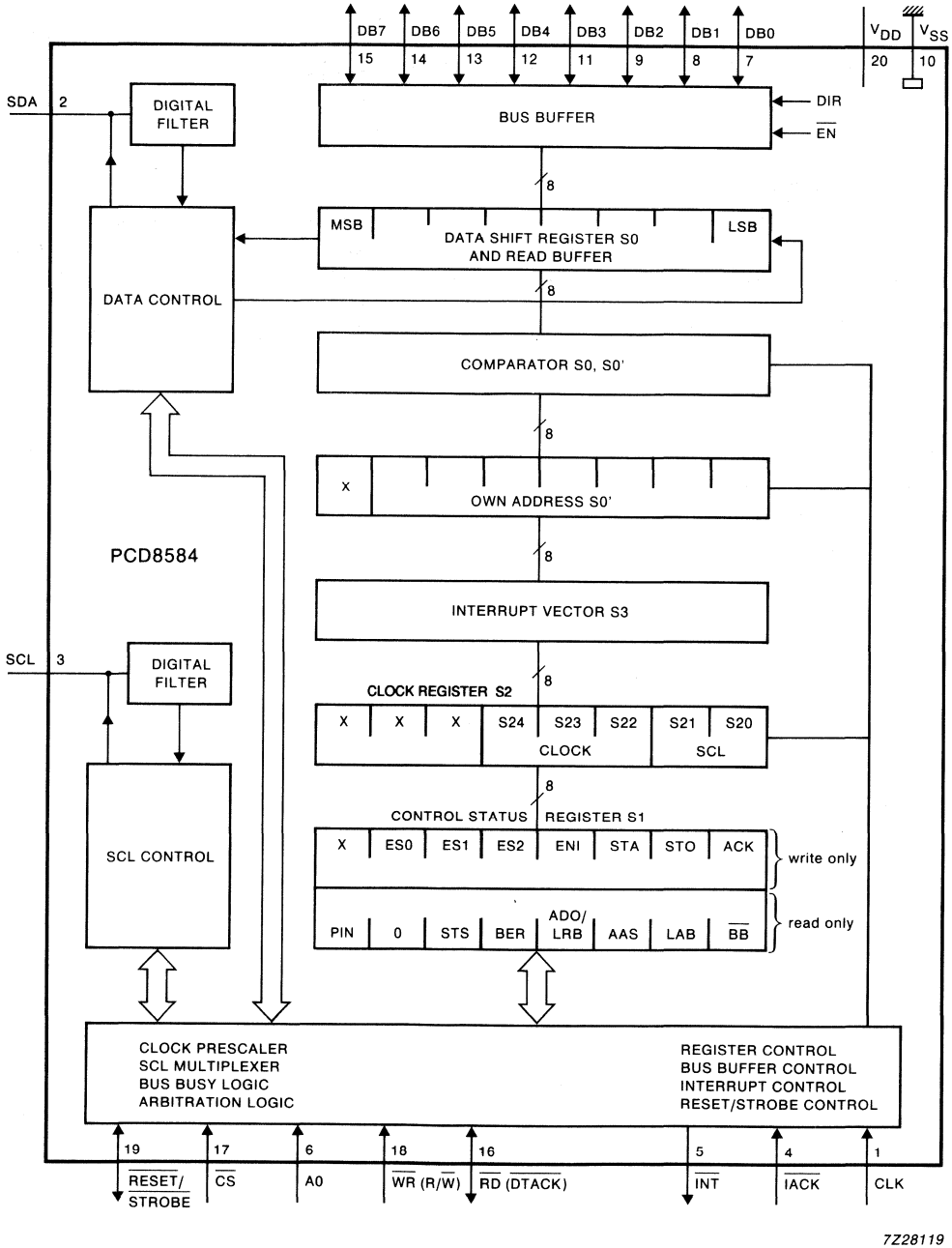
The PCD8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/processors and the serial I²C-bus. The PCD8584 provides both master and slave functions. Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequencing, protocol, arbitration and timing. The PCD8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

Features

- Parallel-bus/I²C-bus protocol converter
- Compatible with most parallel-bus processors including MAB8049, MAB8051, SCN68000 and Z80
- Automatic selection of bus interface
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range −20 to + 70 °C

PACKAGE OUTLINES

PCD8584P: 20-lead DIL; plastic (SOT146).
PCD8584T: 20-lead mini-pack; plastic (SO20; SOT163A).



7Z28119

Where:

( ) indicate the SCN68000 pin name designations.
X = don't care.

Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: −40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see 84CXXX family specification

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

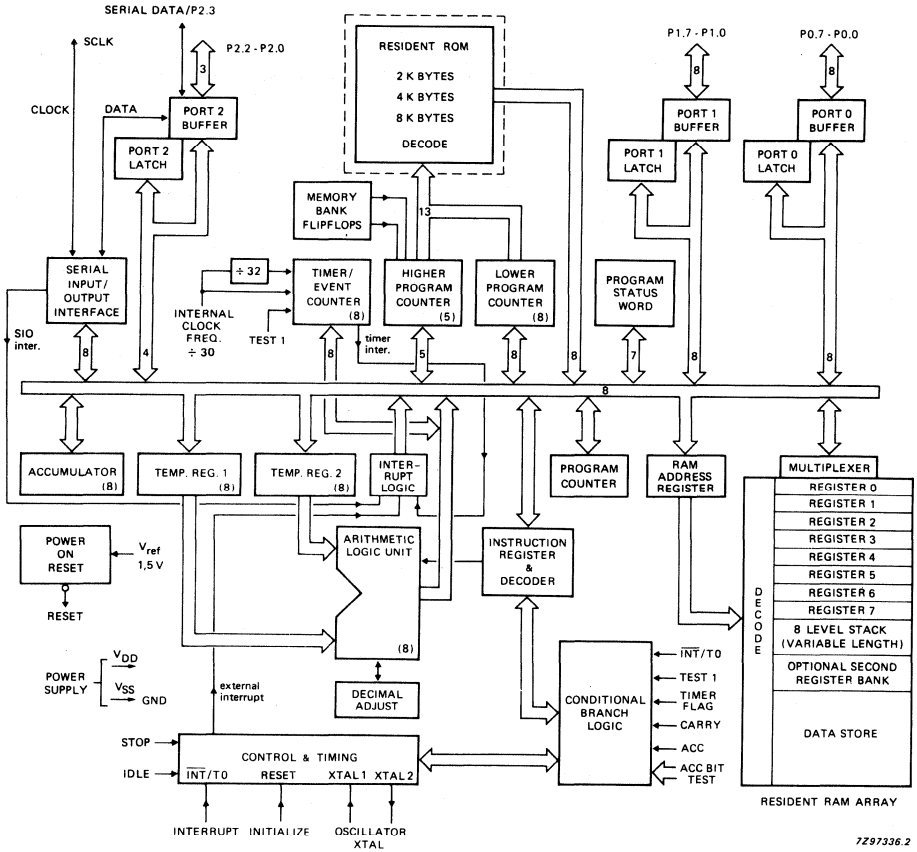


Fig. 1 Block diagram.

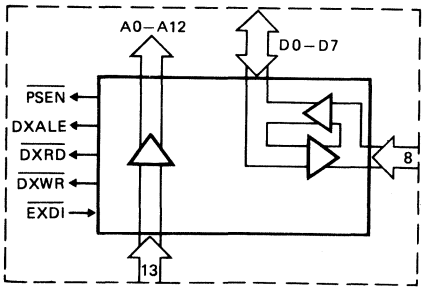
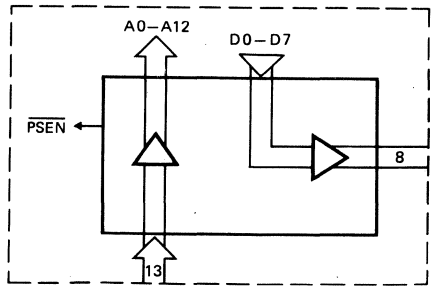


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.



7Z20149.1

Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C12, PCF84C22 and PCF84C42 microcontrollers. Each device has 13 quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C12 – 64 x 8 RAM, 1 K x 8 ROM
- PCF84C22 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C42 – 64 x 8 RAM, 4 K x 8 ROM

These efficient microcontrollers also perform well as arithmetic processors. The instruction set is similar to that of the MAB8048. They have bit handling abilities and facilities for both binary and BCD arithmetic.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K, 2 K or 4 K x 8 ROM
- 64 x 8 RAM
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level, vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 V to 5.5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: –40 to + 85 °C

PACKAGE OUTLINES

PCF84C12/22/42P: 20-lead DIL; plastic (SOT146).
PCF84C12/22/42T: 20-lead mini-pack; plastic (SO20, SOT163A).

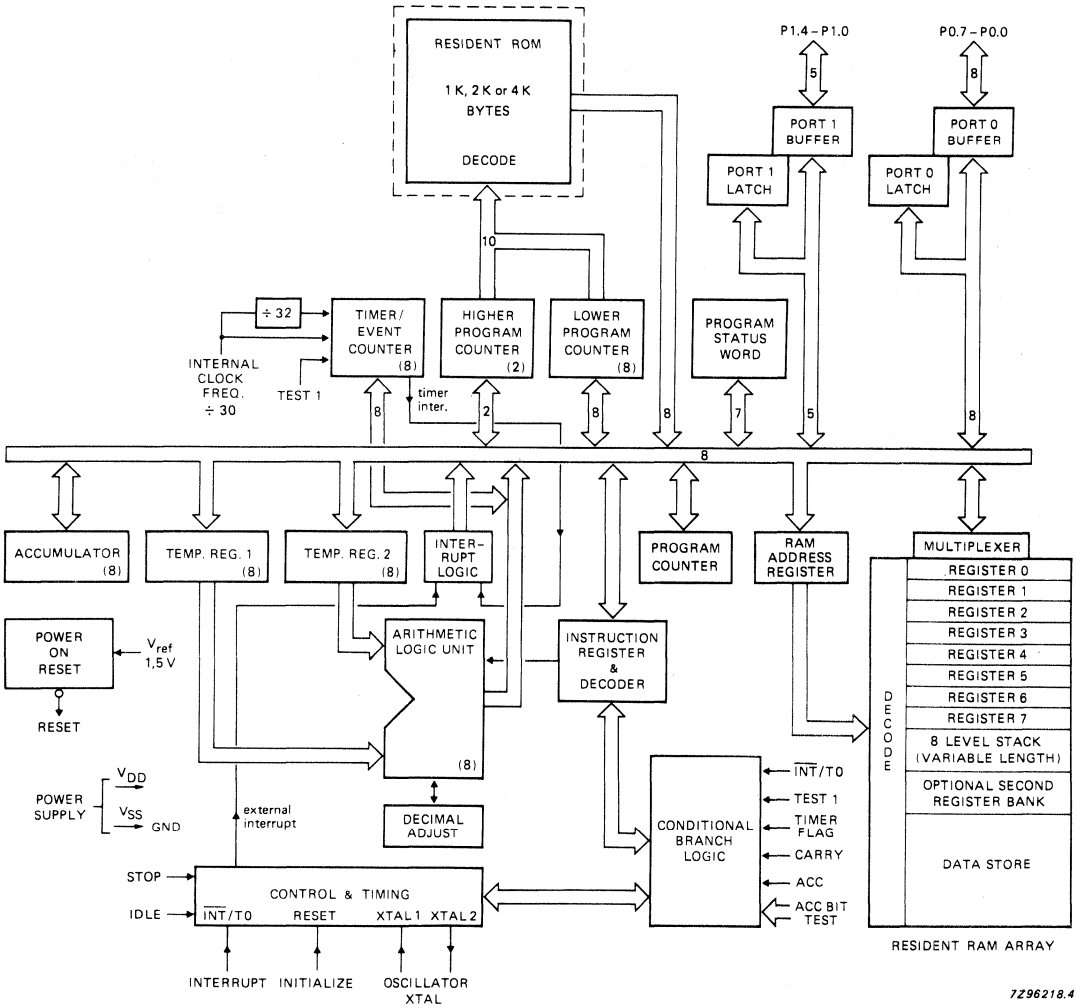


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the 84CXXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer
  (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158A).

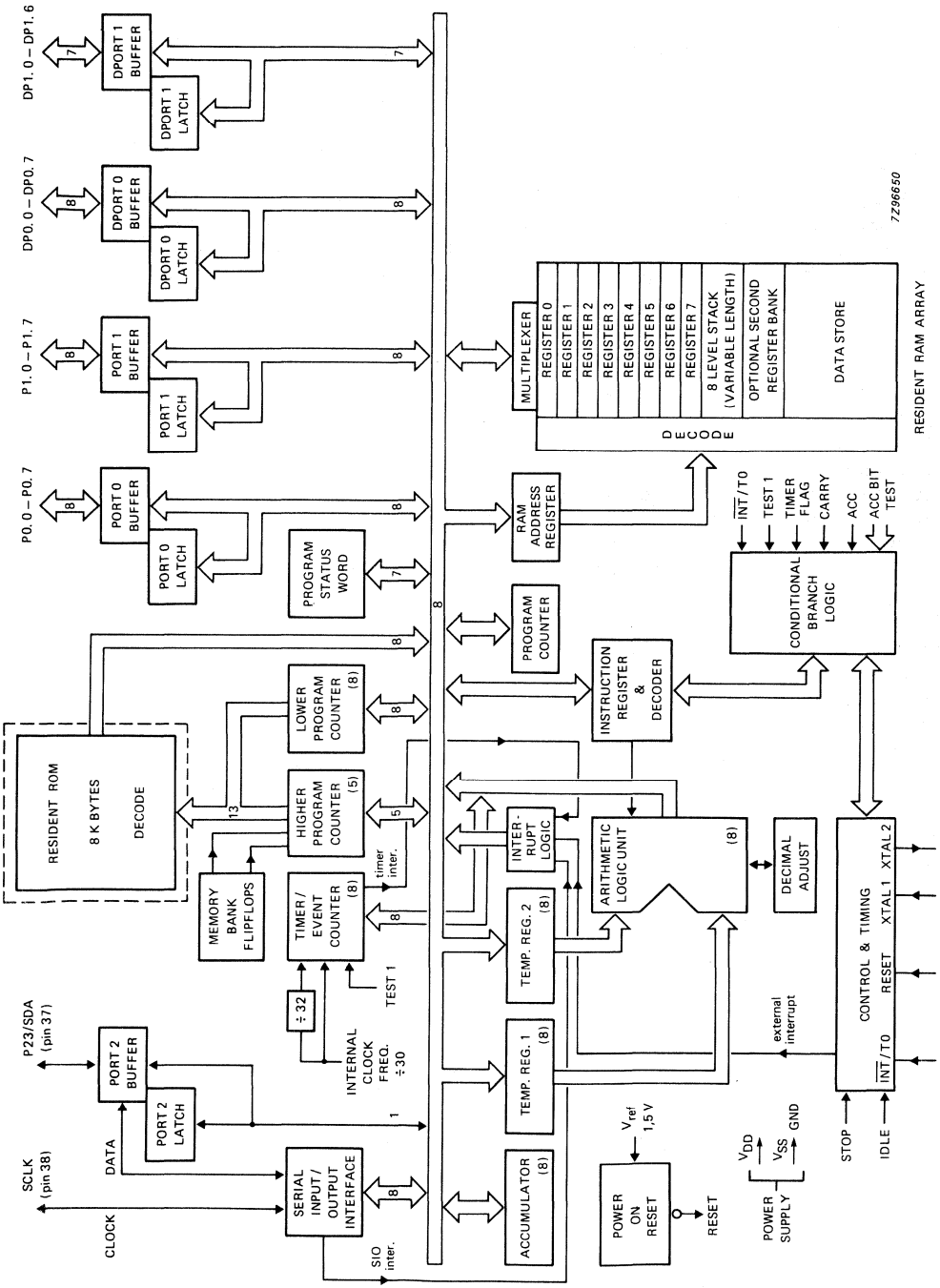


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The PCF84C230 is a single-chip 8-bit microcontroller manufactured in CMOS technology, and is a member of the 84CXXX family. For detailed information see the 84CXXX family specification.

The PCF84C230 provides 12 general purpose quasi-bidirectional I/O port lines, a line that is directly testable (T1), one external interrupt line, and an LCD driver for up to 64 graphic elements. The IC is mask-programmable and is designed for control in small systems with LCD displays.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL package
- 2 K ROM bytes
- 64 RAM bytes
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 12 quasi-bidirectional I/O port lines
- Configuration of I/O lines can be individually selected by mask (pull-up, open drain, push-pull)
- LCD drive circuit with 16 segment drivers and selectable backplane drive configuration: static or 2/3/4 multiplex, to drive up to 64 graphic elements
- LCD possible during STOP mode
- Single-level vectored interrupts: external and timer/event counter
- Power-on reset and low voltage detector
- Single supply voltage from 2.5 V to 5.5 V
- STOP and IDLE modes
- Clock frequency 100 kHz to 10 MHz
- Operating ambient temperature range: −40 to + 85 °C

PACKAGE OUTLINES

40-lead DIL; plastic (SOT129).
40-lead mini-pack; plastic (VS040; SOT158A).

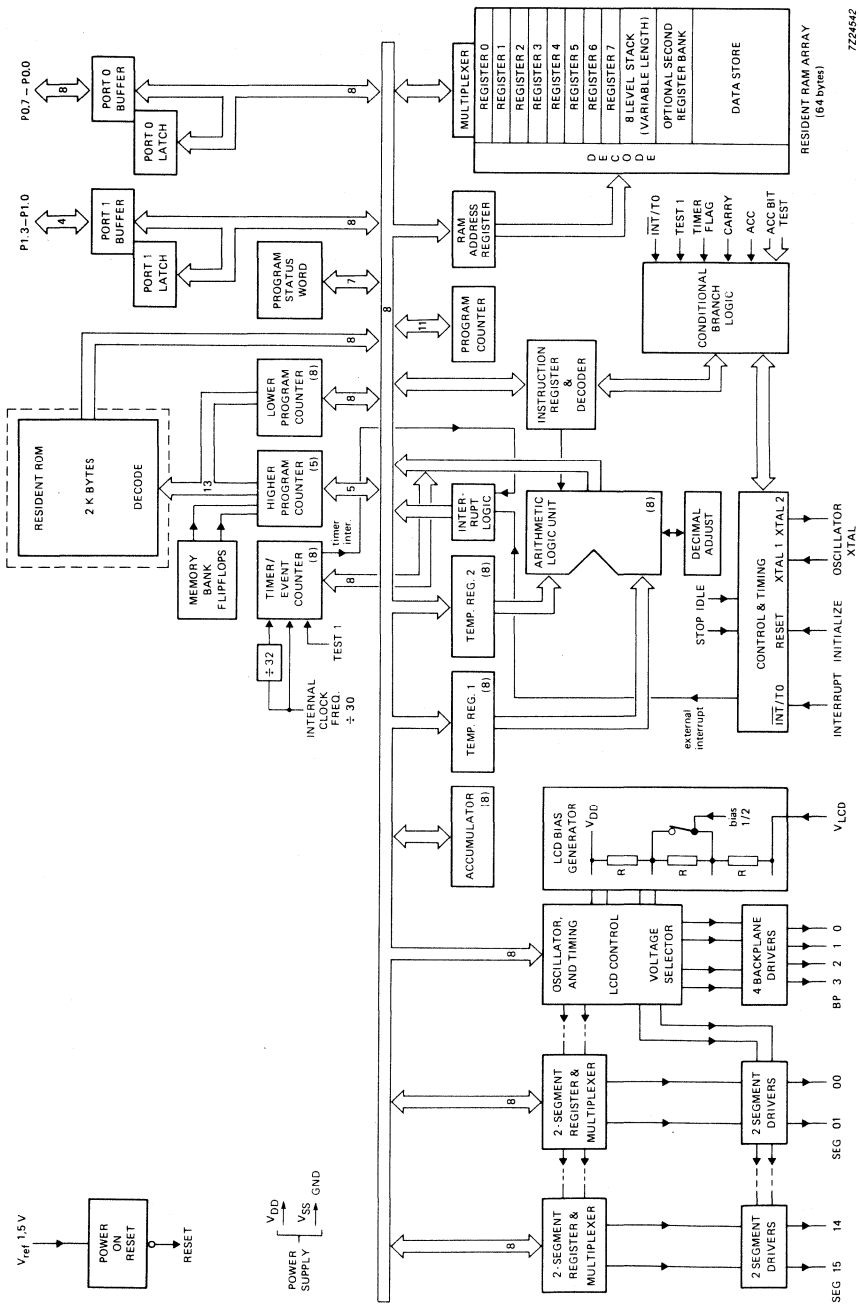


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the 84CXXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the 84CXXX family specification.

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

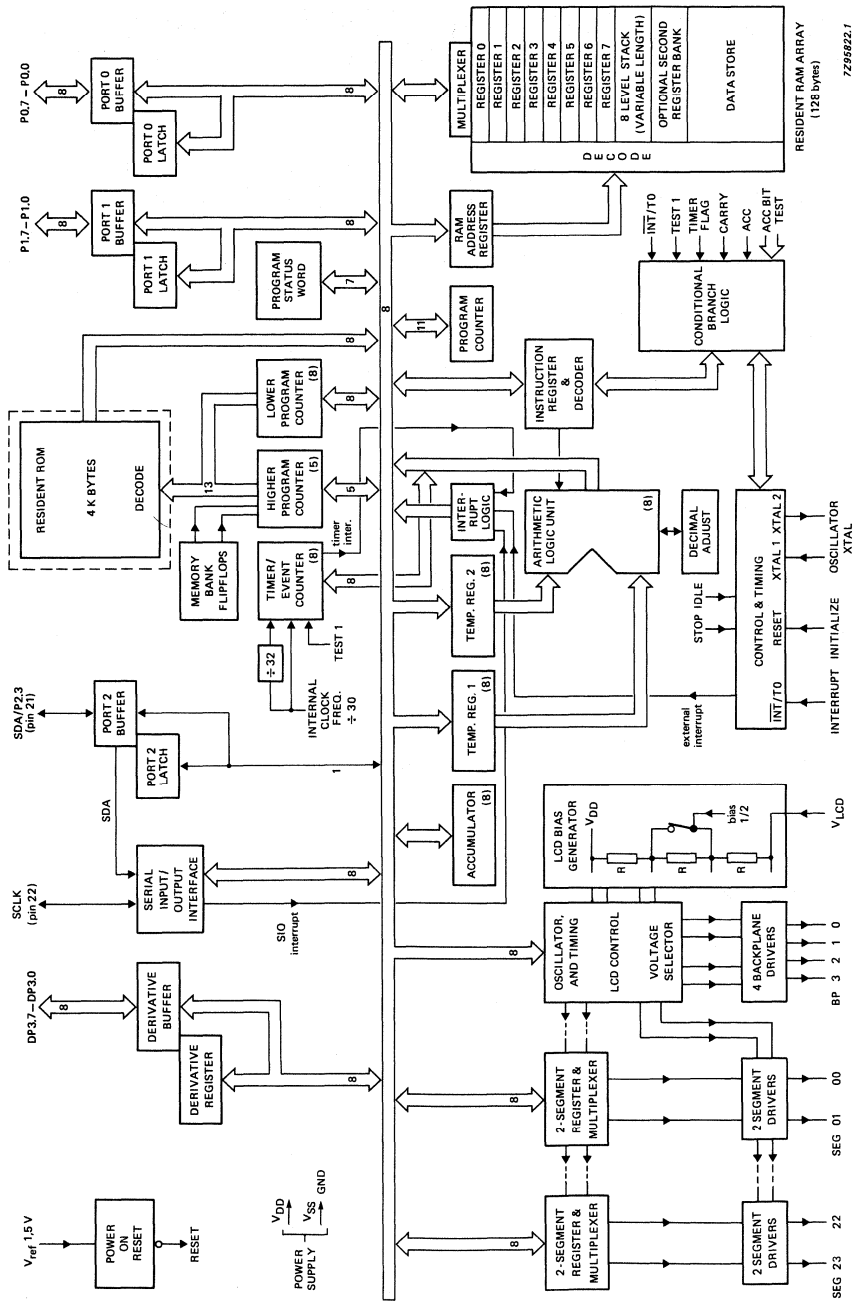


Fig. 1 Block diagram; PCF84C430.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVERS, DERIVATIVE PORT, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C633A is a microcontroller with 20 on-chip liquid crystal display (LCD) outputs. These can be configured for one to four backplanes and 19 to 16 segment lines, yielding a maximum of 64 display elements. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C633A includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding real-time applications.

IMPORTANT

This data sheet details the specific properties of the PCF84C633A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 56-lead package
- 6 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB 8048) all of 1 or 2 cycles
- 28 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupts; external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- 20 LCD output configurable for one to four backplanes and 19 to 16 segment lines
- Drive for up to 64 display elements
- Display memory bank switching in static and duplex drive modes
- 19 of the LCD outputs may serve as additional low-drive logic outputs with optional level-shift
- Stop and idle modes
- Logic supply V_{DD}; 2.5 V to 5.5 V
- Independent LCD supply V_{DDLC}; 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to 85 °C
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF84C633AT: 56-lead mini-pack; plastic (VSO56; SOT190)

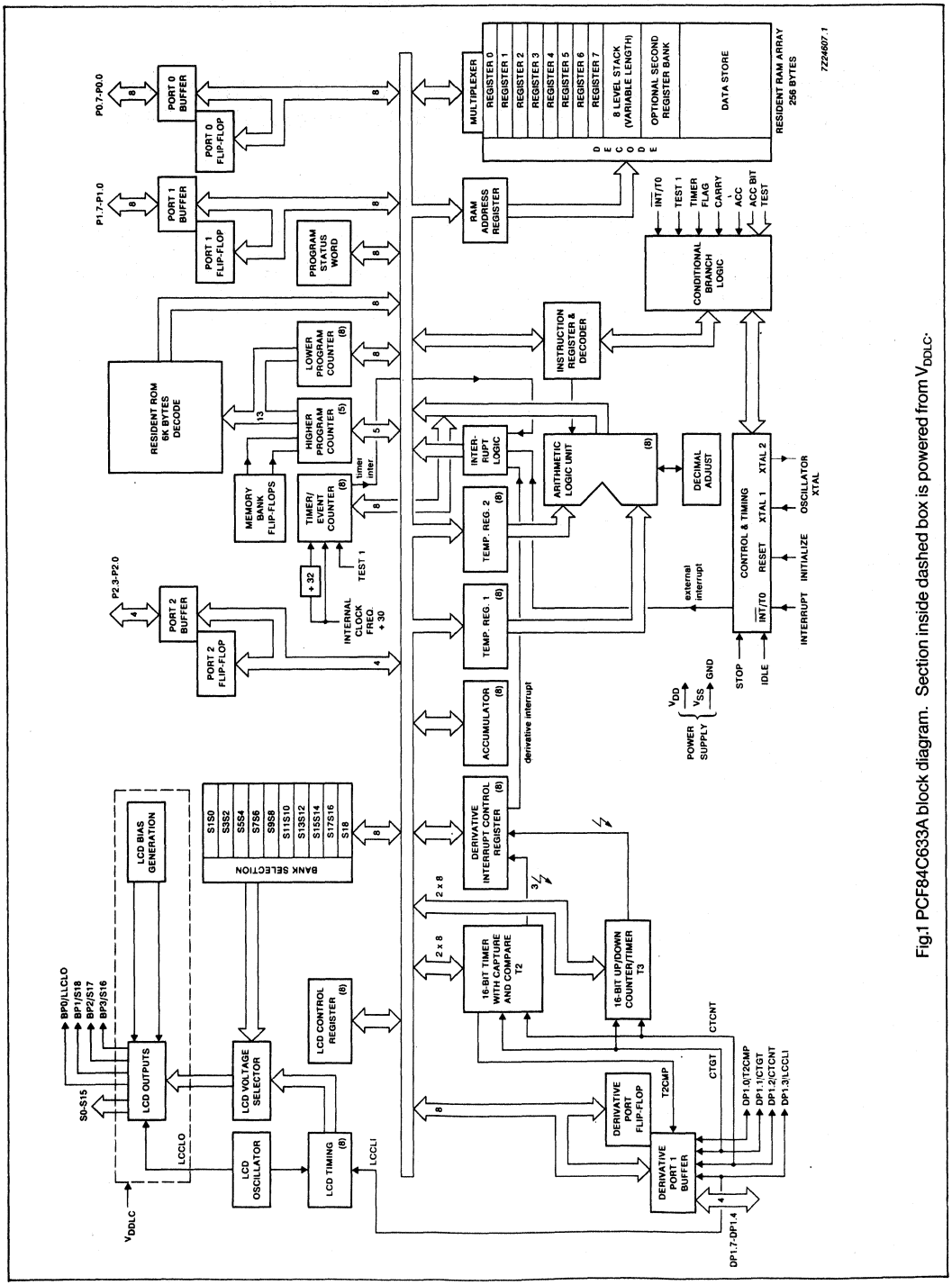


Fig.1 PCF84C633A block diagram. Section inside dashed box is powered from V_{DDLC}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH DERIVATIVE PORTS, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C853A is a microcontroller with 33 quasi-bidirectional I/O port lines. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C853 includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding realtime applications.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead package
- 8 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 33 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupt: external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- Stop and Idle modes
- Supply range V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to + 85 °C
- Manufactured in silicon gate CMOS process

IMPORTANT

This data sheet details the specific properties of the PCF84C853A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

PACKAGE OUTLINES

PCF84C853AP: 40-lead DIL; plastic (SOT129)
PCF84C853AT: 40-lead mini-pack; plastic (VSO40; SOT158A)

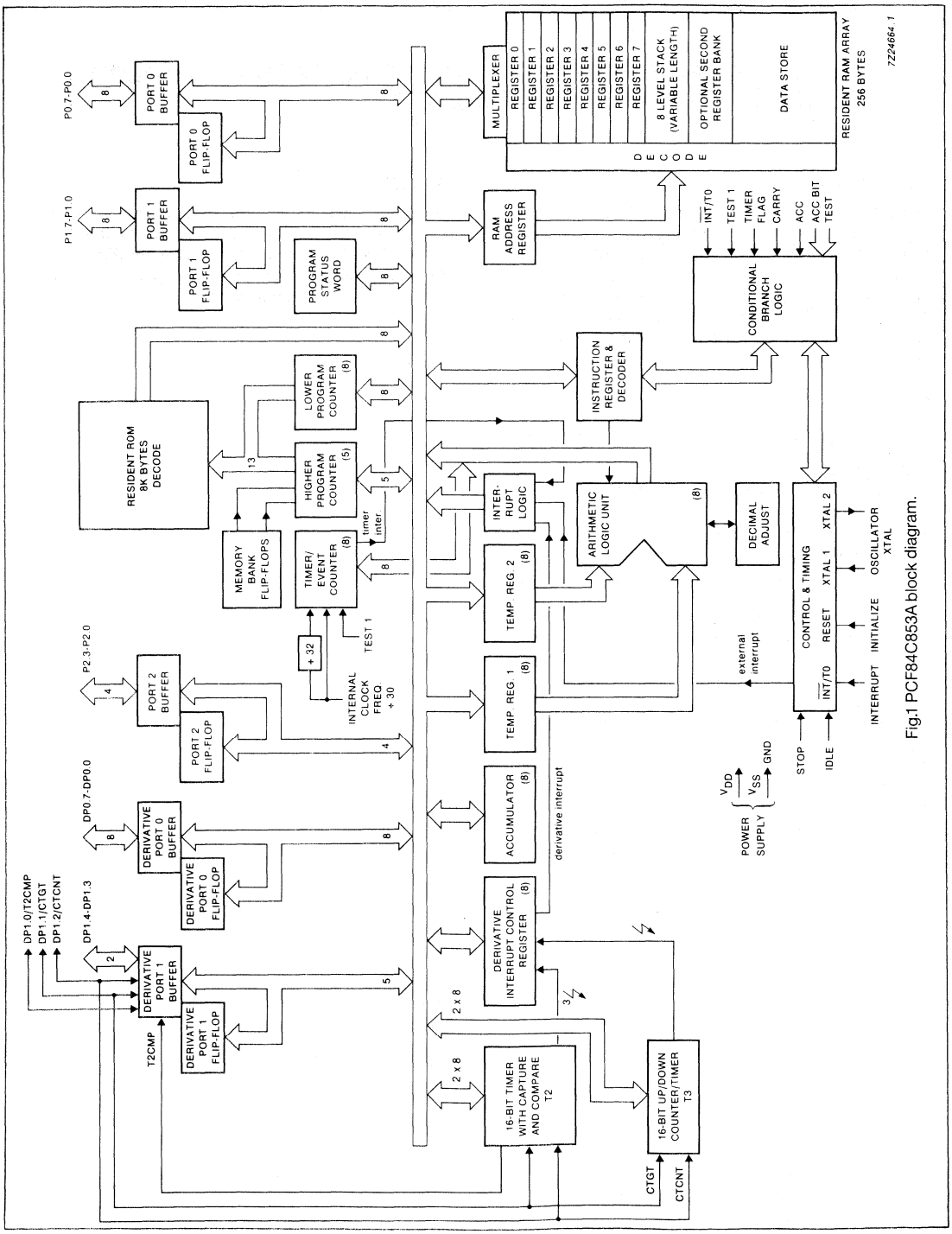


Fig.1 PCF84C853A block diagram.

POWER FAILURE DETECTOR AND RESET GENERATOR

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output $\overline{POWF}$ is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power failure

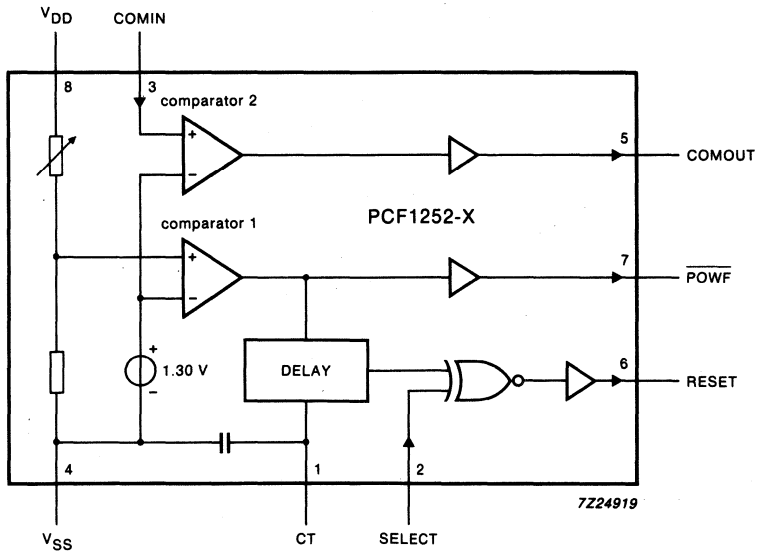


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

INFRARED REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

GENERAL DESCRIPTION

The PCF1254 is intended for remote control systems. The circuit can be used to transmit an individual code to a receiver by infrared radiation. The code is stored in an EEPROM which is programmed with 5 V by the equipment manufacturer. Application in identification and security systems are also possible.

Features

- 22 bits of EEPROM code with automatic 2-bit preamble
- Two operating modes: single or repetitive transmission
- Supply voltage range 2.5 V to 6.5 V
- High output current drive (typ. 50 mA at 5 V)
- Operating ambient temperature range −40 to + 85 °C

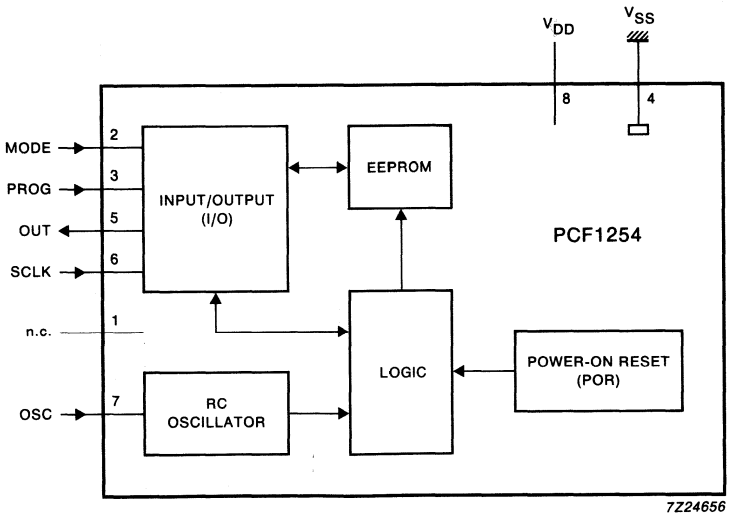


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1254P: 8-lead DIL; plastic (SOT97).
PCF1254T: 8-lead mini-pack; plastic (SO8; SOT96A).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_c) when in pointer or thermometer mode.

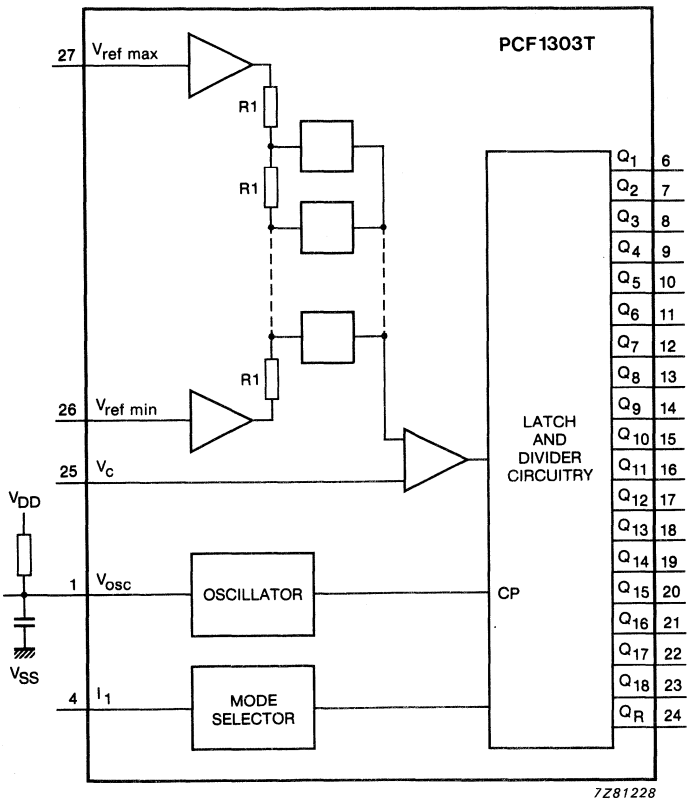


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

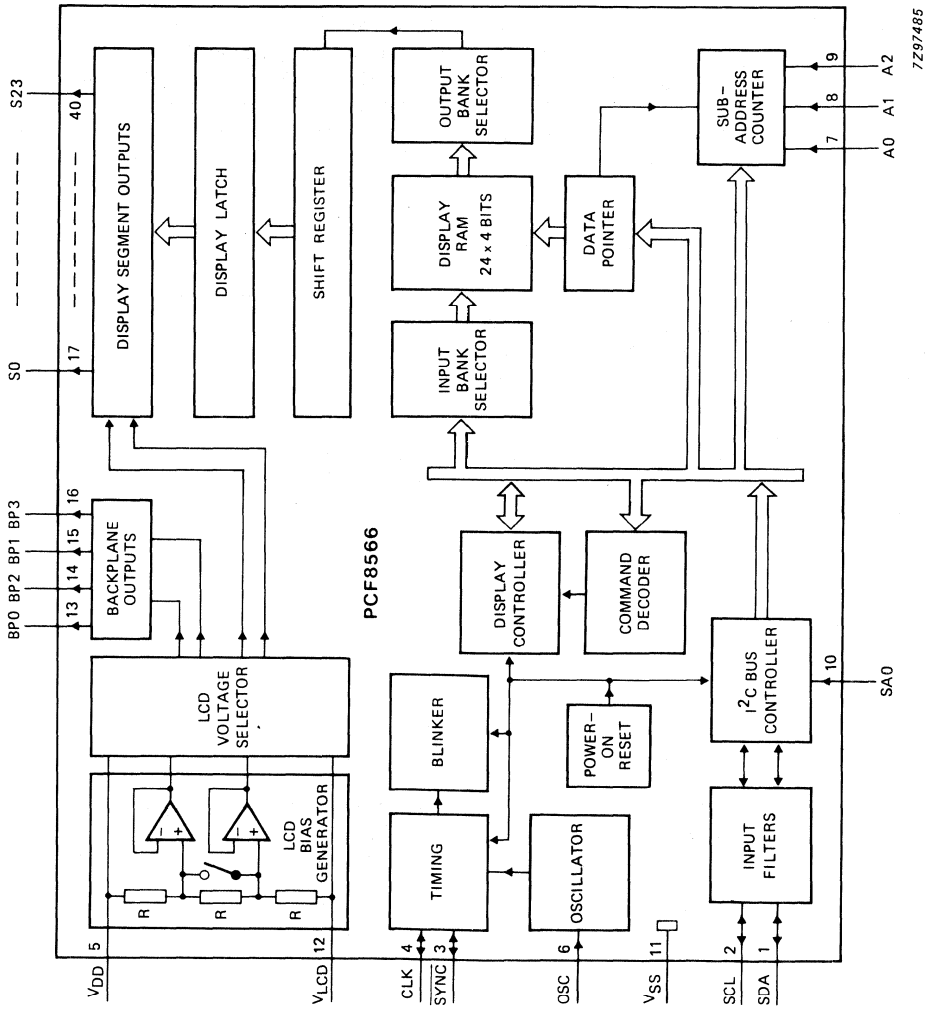


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD DIRECT MODE DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8567C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing and hardware subaddressing..

Features

- Direct drive mode with up to 32 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display

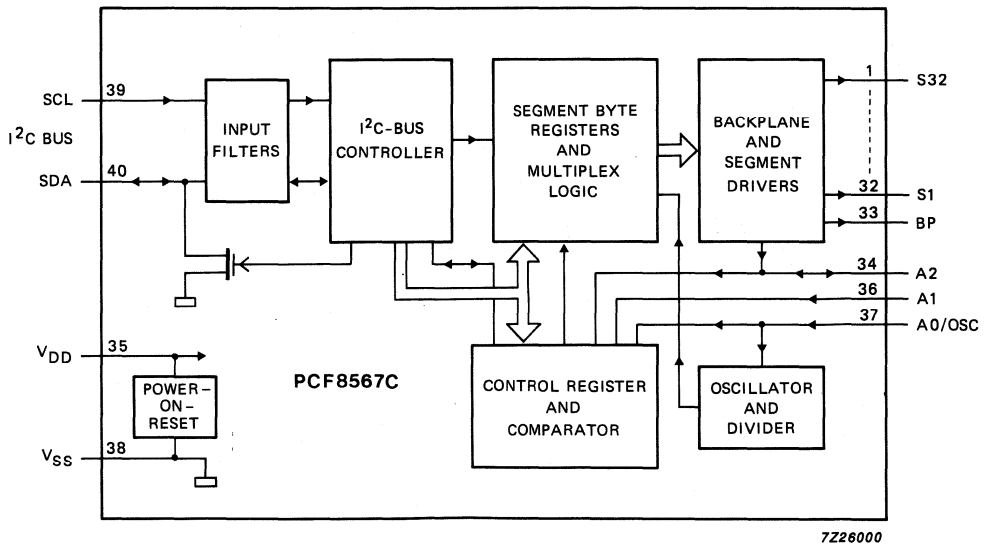


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8567CP: 40-lead DIL; plastic (SOT129).
PCF8567CT: 40-lead mini-pack; plastic (VSO40; SOT158A).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

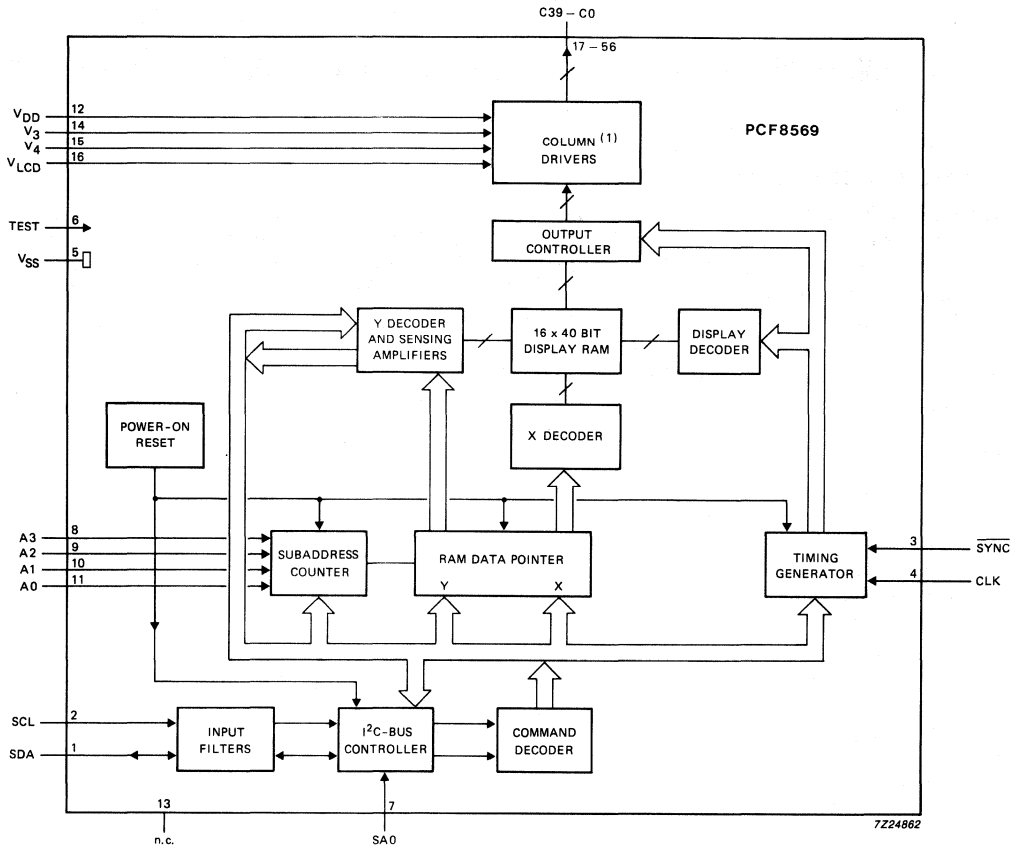
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

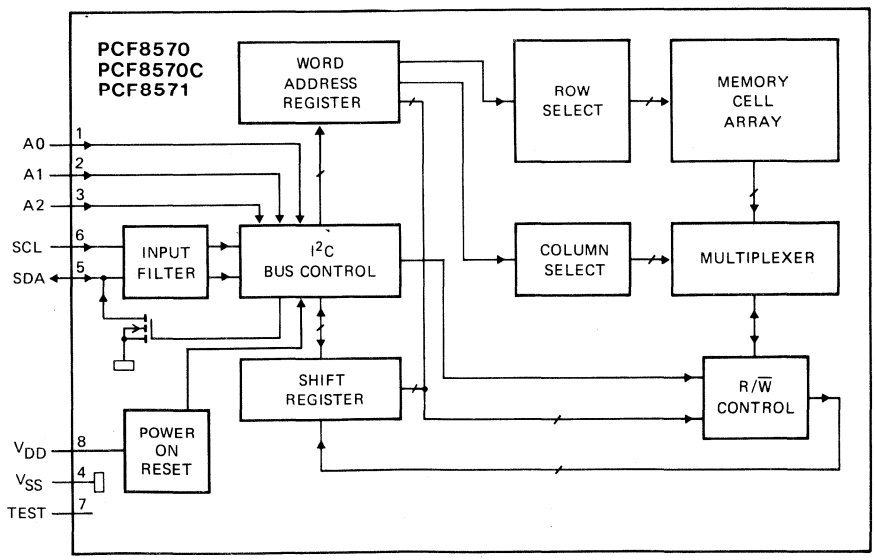


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

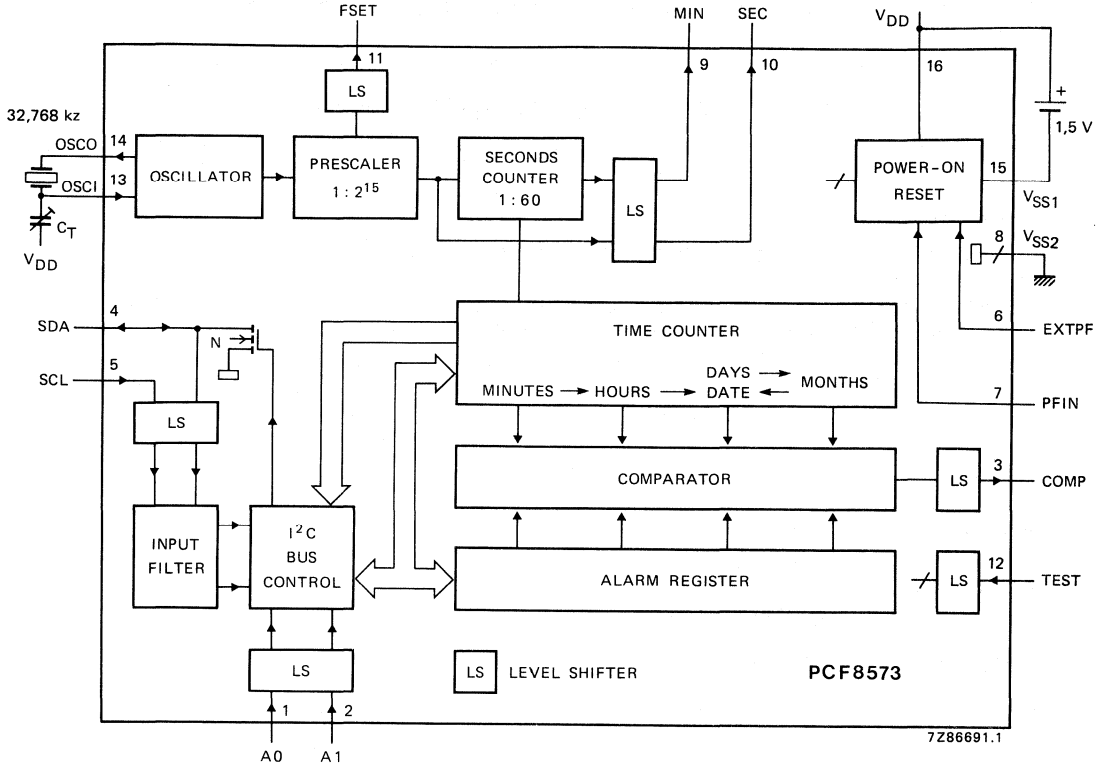


Fig.1 Block diagram.

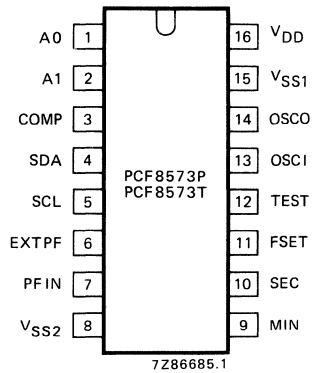


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C-bus)
5	SCL	serial clock line (I^2C-bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

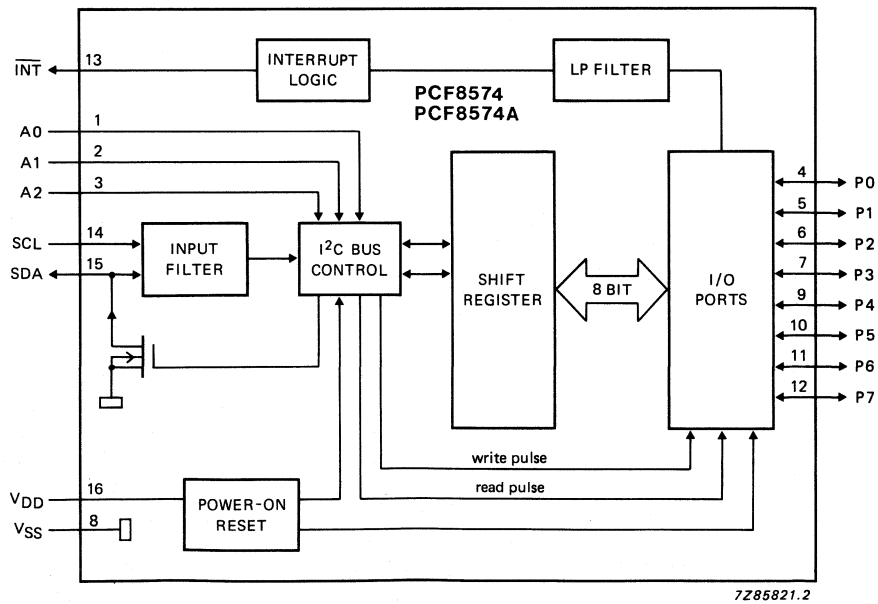


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

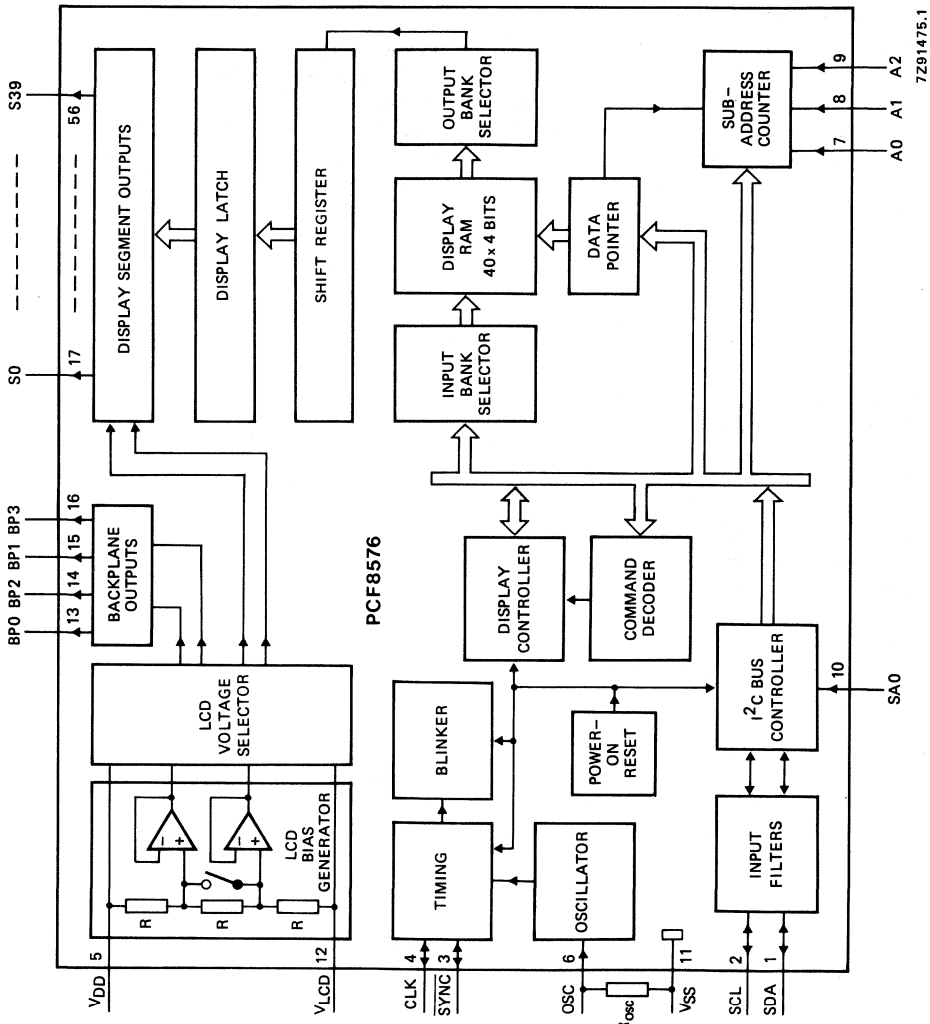


Fig.1 Block diagram; VSO56; SOT190.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

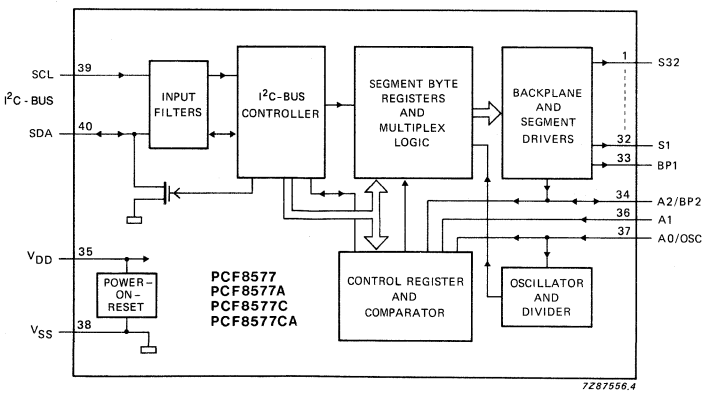


Fig.1 Block diagram.

PAKCAGE OUTLINES

PCF8577P, PCF8577AP PCF8577CP, PCF8577CAP	40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	in blister tape.
PCF8577U/5 PCF8577CU/5	wafer unsawn.
PCF8577U/10 PCF8577CU/10	chip on film-frame-carrier (FFC).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

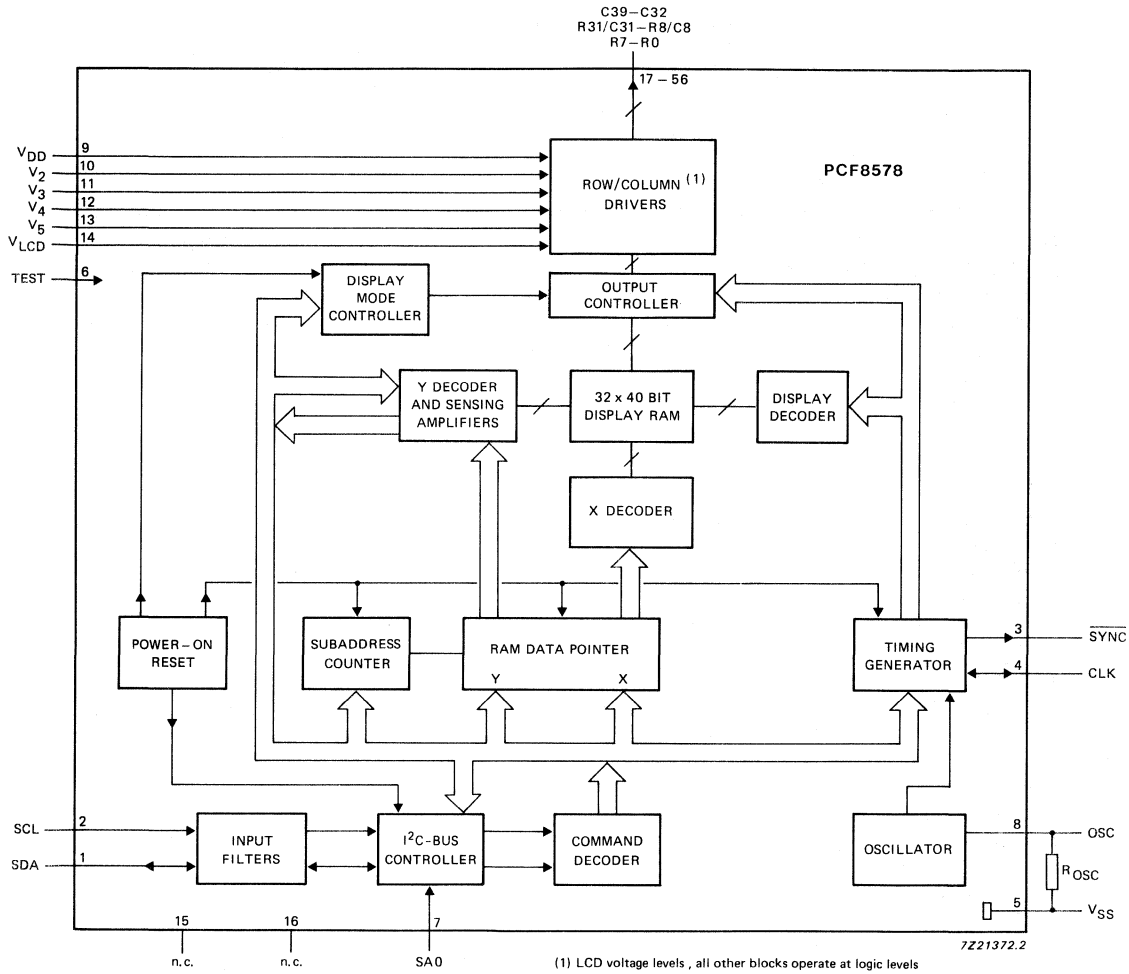


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

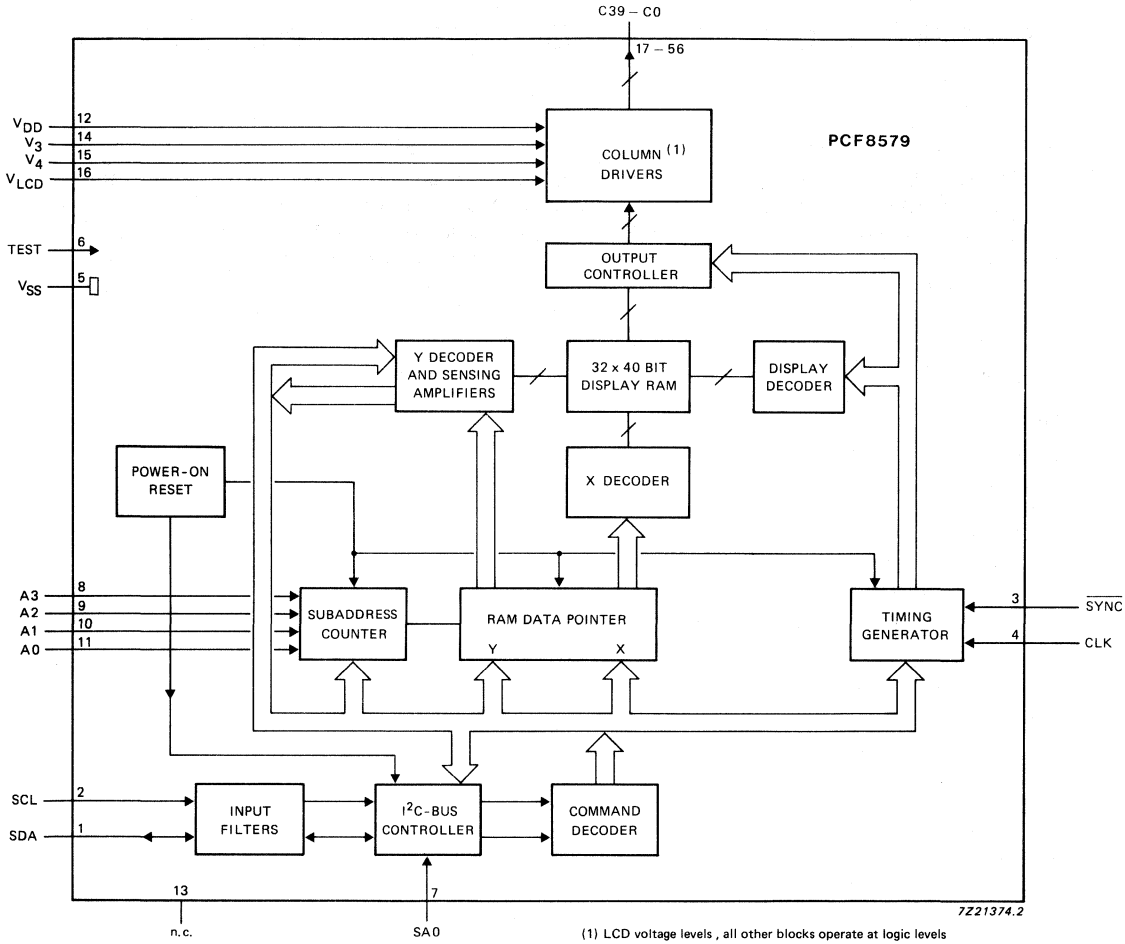


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

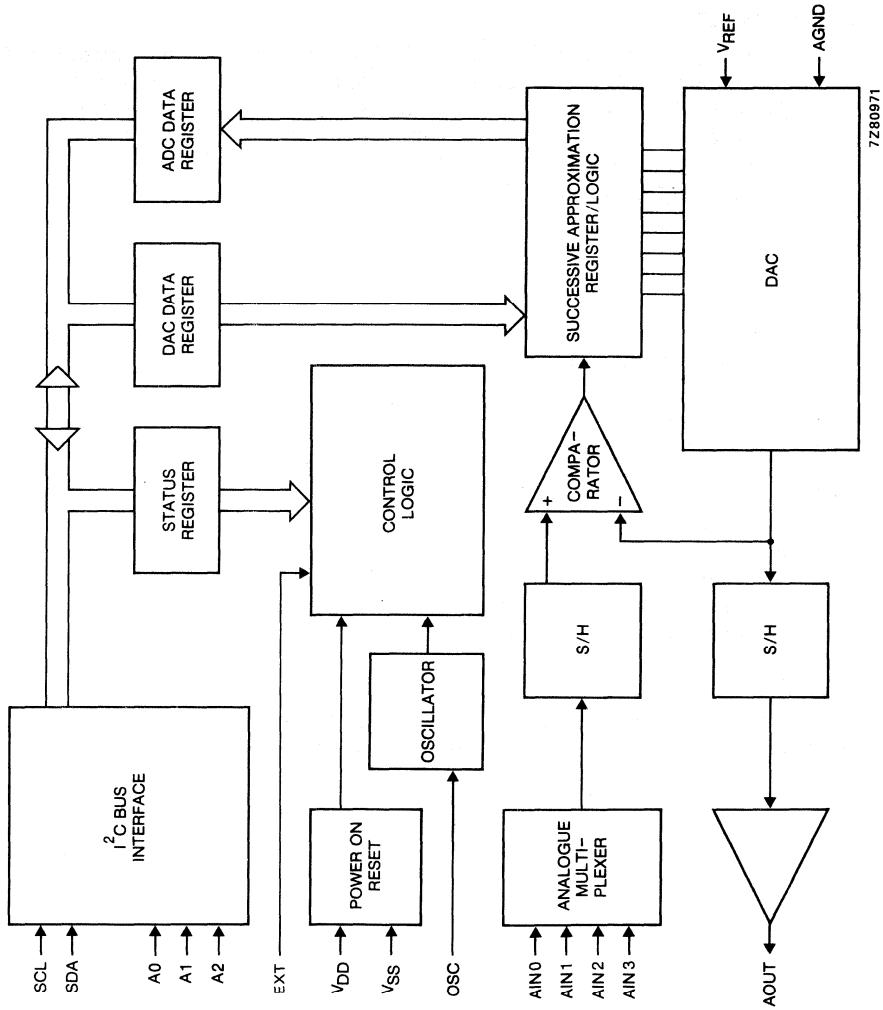


Fig. 1 Block diagram.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102H).

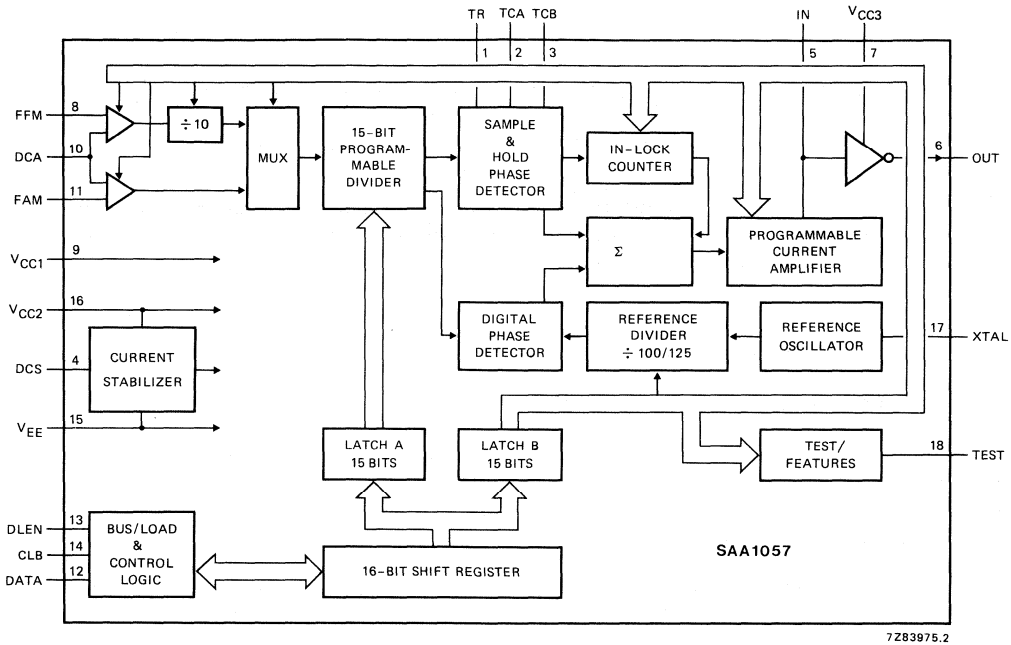


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

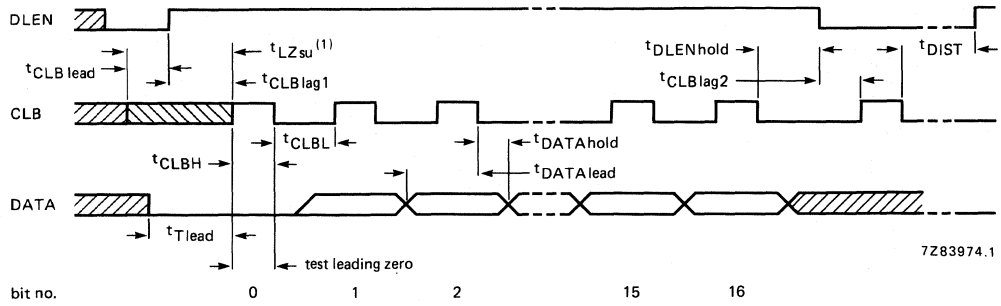


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I²C bus is used for other devices on the same data and clock lines.

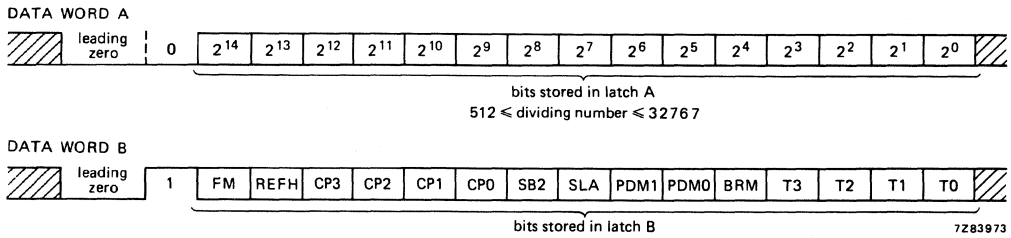


Fig. 3 Bit organization of data words A and B.

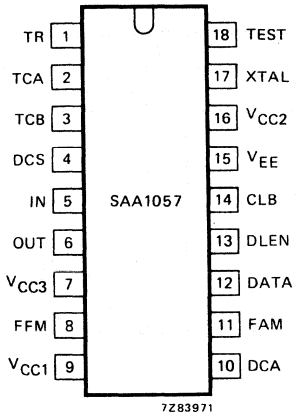


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	V_i (rms)	30	–	500	mV	
Input voltage at FFM	V_i (rms)	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device
Busy time						or
asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2} −0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	µs	REFH = '1'
	t_{dis}	–	–	6,25	µs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

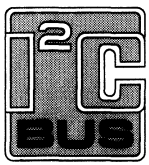
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

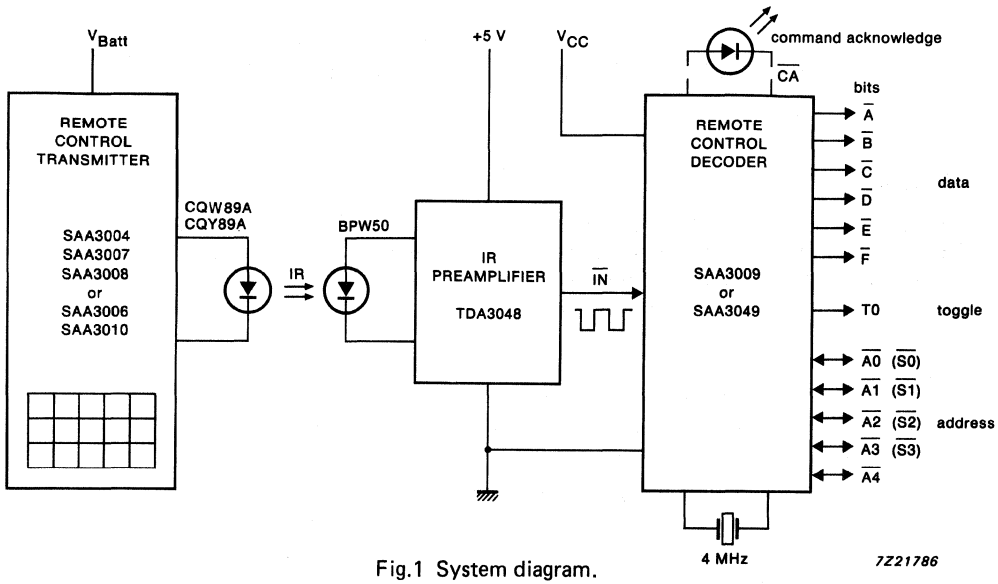


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004 V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)

SAA3007 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3008 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3006 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

SAA3010 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	$V_{CC}+0.8$	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	–	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	–	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation				
SAA3009	P_{tot}	–	1	W
SAA3049	P_{tot}	–	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+ 70	°C
SAA3049	T_{amb}	−40	+ 85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+ 150	°C
SAA3049	T_{stg}	−65	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = −40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	−0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	−0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	$I_{OH} = -50\ \mu A$	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 10$ mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 5$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	$V_{CC} = 5$ V ± 10%; $V_{OL} = 0.4$ V	I_{OL}	1.6	3.0	–	mA

DEVELOPMENT DATA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 or SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

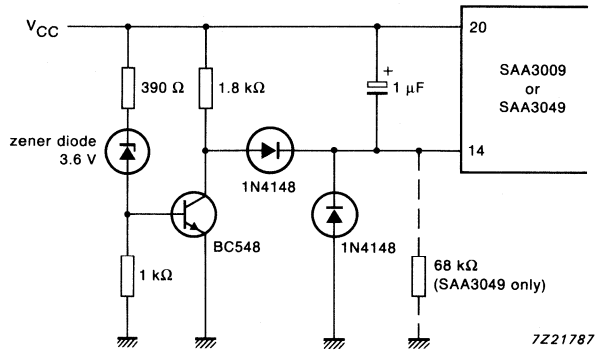


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

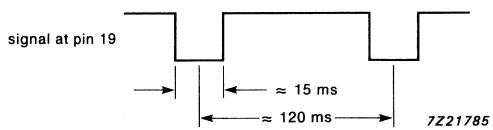
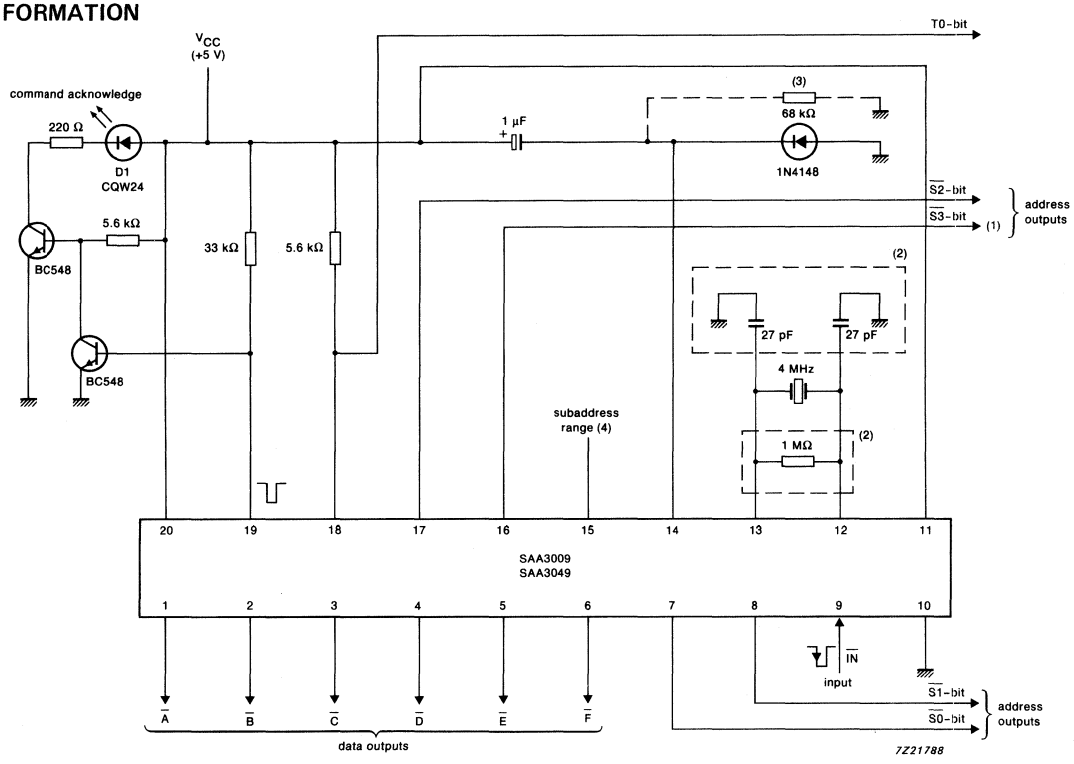


Fig.3 Output diagram of command acknowledge.

APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

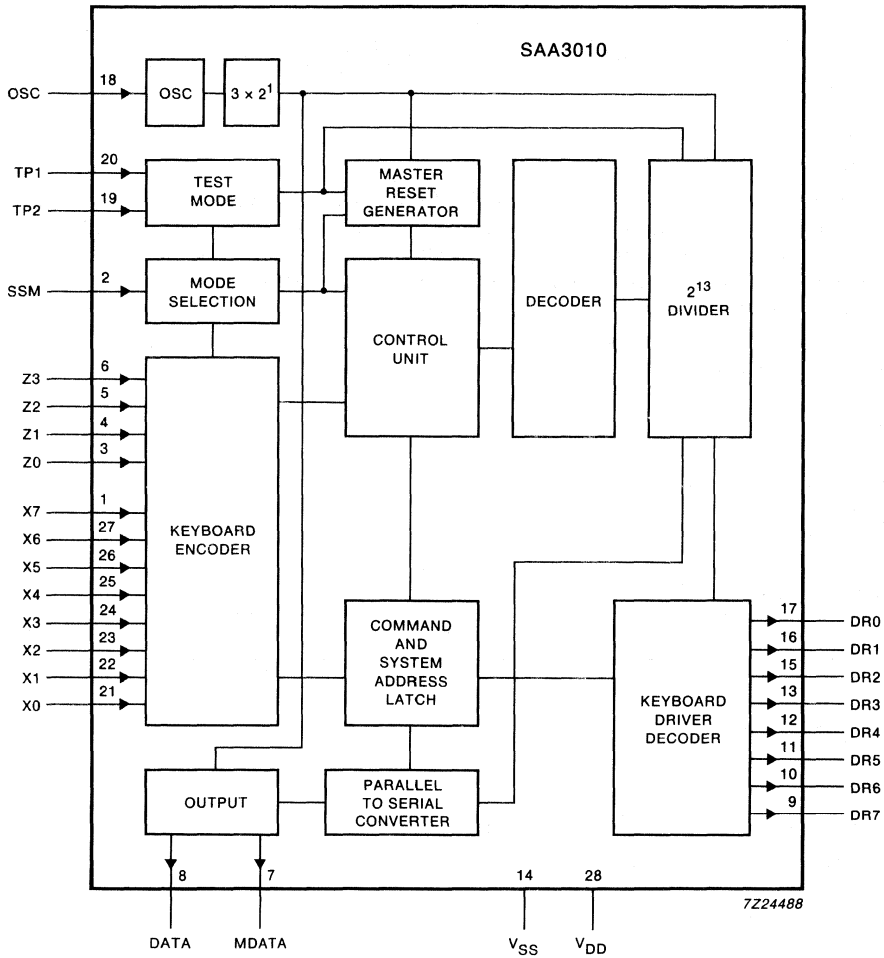


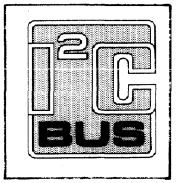
Fig.1 Block diagram.

Philips Components

Data sheet	
status	Product specification
date of issue	September 1990

SAA3028

Infrared remote control transcoder (RC-5)



FEATURES

- Converts RC-5 biphase coded signals into binary equivalents
- Two data inputs
- Rejects all codes not in RC-5 format
- I²C output interface capability
- Power-off facility
- Power-on-reset for defined start-up

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available for RC-5 coded signals. The input used is that at which an active code is first detected. Coded signals not in RC-5 format are rejected. Data input and output is by serial transfer, the output interface being compatible for I²C-bus operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		4.5	5.5	V
I_{DD}	supply current (quiescent)	V_{DD} = 5.5 V; T_{amb} = 25 °C	-	200	µA
T_{amb}	operating temperature range		−25	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3028P	16	16	plastic	SOT38D
SAA3028T	16	16	mini-pack	SO16L; SOT162A

Infrared remote control transcoder (RC-5) SAA3028

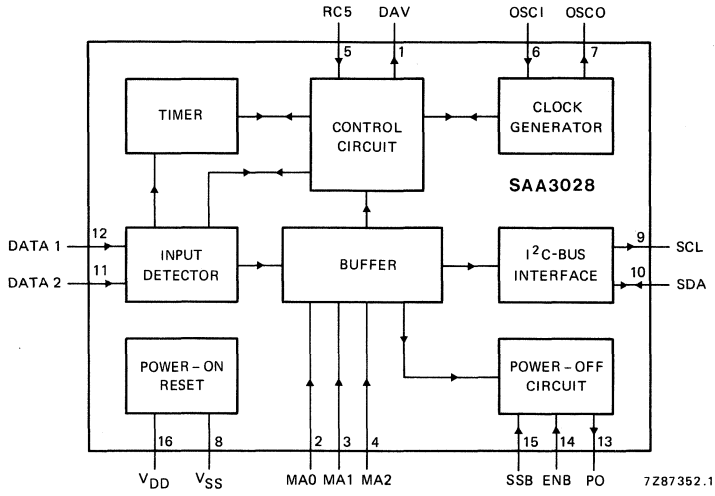


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DAV	1	data valid output with open drain n-channel transistor
MA0	2	master address input 0
MA1	3	master address input 1
MA2	4	master address input 2
RC5	5	data 2 input select
OSCI	6	oscillator input
OSCO	7	oscillator output
V_{SS}	8	negative supply (ground)
SCL	9	I^2C bus serial clock line
SDA	10	I^2C bus serial data line
DATA 2	11	data 2 input
DATA 1	12	data 1 input
PO	13	power-off signal output with open drain n-channel transistor
ENB	14	enable input
SSB	15	set standby input
V_{DD}	16	positive supply (+5 V)

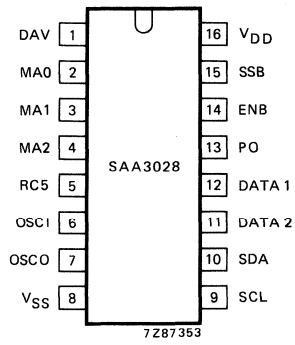


Fig.2 Pinning diagram.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March1991

SAA6579T
Radio data system demodulator (RDS)

FEATURES

- Anti-aliasing filter (2nd order)
- Integrated 57 kHz bandpass subcarrier filter (8th order)
- Reconstruction filter (2nd order)
- 57 kHz carrier regeneration
- Synchronous demodulator for 57 kHz modulated RDS signals
- 4.332 MHz crystal oscillator with variable dividers
- Clock regeneration with lock on biphase rate
- Biphase symbol decoder with integrate and dump functions
- Differential decoder
- Signal quality detector
- Subcarrier output

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5	5.5	V
V_{DDD}	digital supply voltage (pin 12)	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current	-	6	-	mA
V_i	RDS input amplitude (peak-to-peak value, pin 4)	3.0	-	5.0	mV
$V_{o\ H}$	output level HIGH for signals RDDA, RDCL, QUAL and T57	4.4	-	-	V
$V_{o\ L}$	output level LOW for signals RDDA, RDCL, QUAL and T57	-	-	0.4	V
T_{amb}	operating ambient temperature	–40	-	+85	°C

GENERAL DESCRIPTION

The integrated CMOS circuit SAA6579T is a RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting.

The data signal RDDA and the clock signal RDCL are provided as outputs for further processing by a suitable decoder (microcomputer).

The operational functions of the device are in accordance with the EBU specification EN 50067.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA6579T	16	mini-pack	plastic	SOT162A

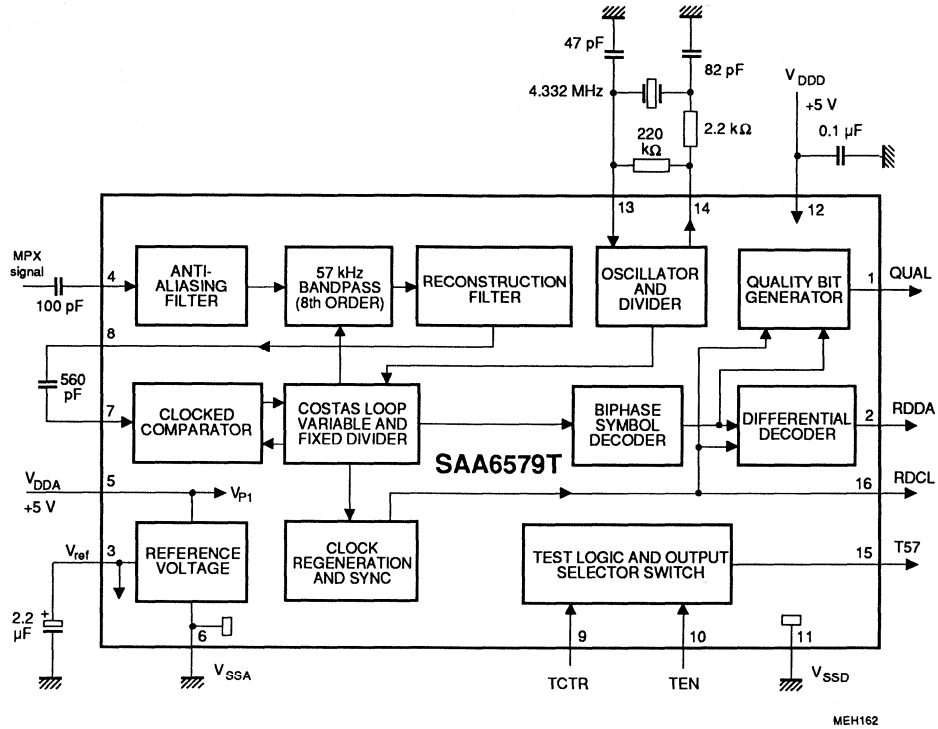


Fig.1 Block diagram, test and application circuit.

Radio data system demodulator (RDS)

SAA6579T

PINNING

SYMBOL	PIN	DESCRIPTION
QUAL	1	quality indication output
RDDA	2	RDS data output
V_{ref}	3	reference voltage output (0.5 V_{DDA})
MPX	4	multiplex input signal
V_{DDA}	5	+5 V supply voltage for analog part
V_{SSA}	6	ground for analog part (0 V)
CIN	7	subcarrier input to comparator
SCOUT	8	subcarrier output of reconstruction filter
TCTR	9	test control
TEN	10	test enable
V_{SSD}	11	ground for digital part (0 V)
V_{DDD}	12	+5 V supply voltage for digital part
OSCI	13	oscillator input
OSCO	14	oscillator output
T57	15	57 kHz clock signal output
RDCL	16	RDS clock output

PIN CONFIGURATION

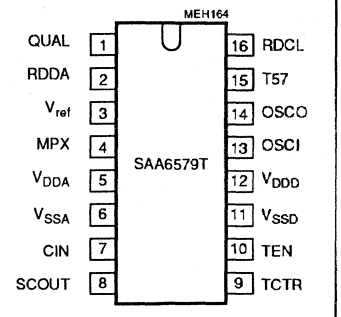


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA6579T is a demodulator circuit for RDS applications. It contains a 57 kHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX).

Filter part

The MPX signal is band-limited by a second-order antialiasing-filter and followed by a 57 kHz Bessel filter (8^{th} order bandpass filter with 3 kHz bandwidth) to separate the RDS signals. This filter is formed in switched capacitor technique and clocked by 541 kHz clock frequency derived from the 4.332 MHz crystal oscillator. Then the signal is fed to the reconstruction filter to smooth the sampled and filtered RDS signal before it is output on pin 8.
The signal is AC-coupled to the clocked comparator (pin 8) to digitize the RDS signal for processing in the digital part.

Digital part

The synchronous demodulator (Costas loop block) with carrier regeneration demodulates the internal coupled, digitized signal. The suppressed carrier is recovered from the two sidebands (Costas loop). The demodulated signal is low-pass-filtered in such a way that the overall pulse shape (transmitter and receiver) approaches a cosinusoidal form in conjunction with the following "Integrate and Dump" circuit.
The data-spectrum sharpening is split into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts. The overall data-channel-spectrum sharpening of the transmitter and the receiver is about 100% roll-off.
The "Integrate and Dump" circuit integrates over one clock period to achieve a valid, demodulated RDS signal (biphase symbols). This signal is decoded in the biphase symbol decoder and in the differential decoder. The RDS data are clocked by data clock RDCL (pin 16), and the data signal RDDA is output (pin 2). The biphase symbol decoder output signal is checked and the quality bit generator generates a quality bit on pin 1 (QUAL = HIGH means data valid, QUAL = LOW means data invalid).

Timing

Fixed and variable dividers are applied to the 4.332 MHz crystal oscillator to generate the 1.1875 kHz RDS clock RDCL, which is synchronized by the incoming data. Which ever clock edge is concidered

(positive or negative going edge) the data will remain valid for 417 µs after the clock transition. The timing of data change is 4 µs before a clock changes. Which clock transition the data change (positive or negative going clock) occurs in, depends on the lock conditions and is arbitrary (bit slip).

During poor reception it is possible that faults in phase occur, then the clock signal stays uninterrupted, and data is constant for 1.5 clock periods. Normally, faults in phase do not occur on a cyclic basis. If however, faults in phase do not occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be shorter than 16 clock periods.

The quality bit changes only at the time of a data change.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134); ground pins 6 and 11 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	supply voltage (pin 5)	0	6	V
V_{DDD}	supply voltage (pin 12)	0	6	V
V_n	voltage on all pins, grounds excluded	−0.5	V_{DD}+0.5	V
T_{stg}	storage temperature range	−40	150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{ESD}	electrostatic handling* for all pins	-	±200	V
	electrostatic handling** for all pins	-	±2000	V

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	supply voltage range (pin 5)		4.5	5	5.5	V
V_{DDD}	supply voltage range (pin 12)		4.5	5	5.5	V
$I_{DD\ tot}$	total supply current	I_1+I_2	-	6	-	mA
V_{ref}	reference voltage (pin 3)	$V_{DDA} = 5$ V	-	2.5	-	-V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MPX Input (pin 4)						
$V_{i\,MPX}$	maximum input signal (peak-to-peak value)	f = 57 ±2 kHz	200	-	-	mV
		f < 50 kHz	0.5	-	-	V
		f < 15 kHz	1.0	-	-	V
		f > 70 kHz	t.b.n.	-	-	mV
	RDS amplitude (peak-to-peak value)		3.0	-	50	mV
R_4	input resistance	f = 0 to 100 kHz	40	-	-	kΩ
G_{8-4}	signal gain	f = 57 kHz	17	20	23	dB
Δf_d	group delay variation	f = 55 to 59 kHz	-	-	40	µs
		f = 55.8/58.2 kHz	-	-	20	µs
57 kHz bandpass filter						
f_o	centre frequency	T = 25°C	56.8	57.0	57.2	kHz
		T = –40 to +85°C	56.5	57.0	57.5	kHz
B	bandwidth	–3 dB	2.5	3.0	3.5	kHz
G	stopband attenuation	Δf = ±7 kHz	31	-	-	dB
		f < 45 kHz	40	-	-	dB
		f < 20 kHz	50	-	-	dB
		f > 70 kHz	40	-	-	dB
R_8	output resistance (pin 8)	f = 57 kHz	0.5	10	18	Ω
Comparator input						
V_i	minimum input level (RMS value, pin 7)	f = 57 kHz	-	1	10	mV
R_7	input resistance		50	120	200	kΩ
Digital demodulator outputs QUAL, RDDA, T57 and RDCL, pins 1, 2, 15 and 16						
$V_{Q\,H}$	output voltage HIGH	I_Q = –20 µA; V_{DDD} = 4.5 V	4.4	-	-	V
$V_{Q\,L}$	output voltage LOW	I_Q = 3.2 mA; V_{DDD} = 5.5 V	-	-	0.4	V
f_{RDCL}	nominal clock frequency RDCL		-	1187.5	-	Hz
f_{SC}	nominal subcarrier frequency T57		-	57.0	-	kHz
4.332 MHz crystal parameters						
XTAL	4.332 MHz, absolute maximum			±50		10^{-6}
	load capacitance		-	30	-	pF
	adjustment tolerance of f_o	T = 25°C	-	-	20	10^{-6}
	frequency tolerance	T = –40 to +85°C	-	-	25	10^{-6}
	maximum resonant resistance		-	-	60	Ω
	Philips components part number			9922 520 00189		

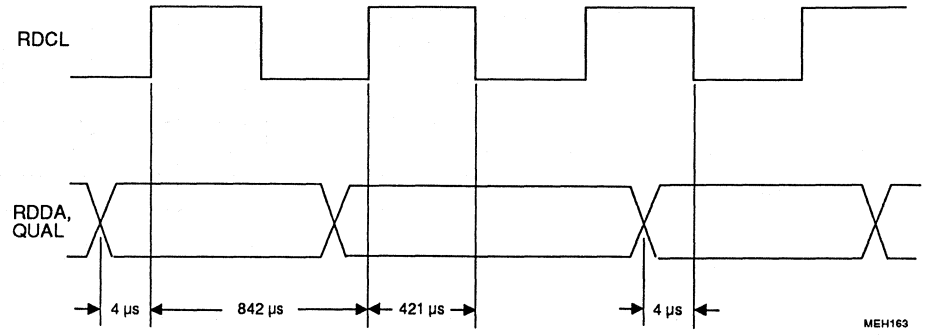


Fig.3 RDS timing diagram including a phase jump.

DIGITAL FILTER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7220 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. For descriptive purposes, the SAA7220 is referred to as the B-chip and the SAA7210 as the A-chip.

Features

- 16-bit serial data input (two's complement)
- Interpolated data replaces erroneous data samples
- −12 dB attenuation via the active LOW attenuation input control (ATSB)
- Smoothed transitions before and after muting
- Two identical finite impulse response transversal filters each with a sampling rate of four times that of the normal digital audio data
- Digital audio output of 32-bit words transmitted in biphase-mark code
- I²S data transfer between SAA7210, SAA7220 and 16-bit dual DAC (TDA1541)

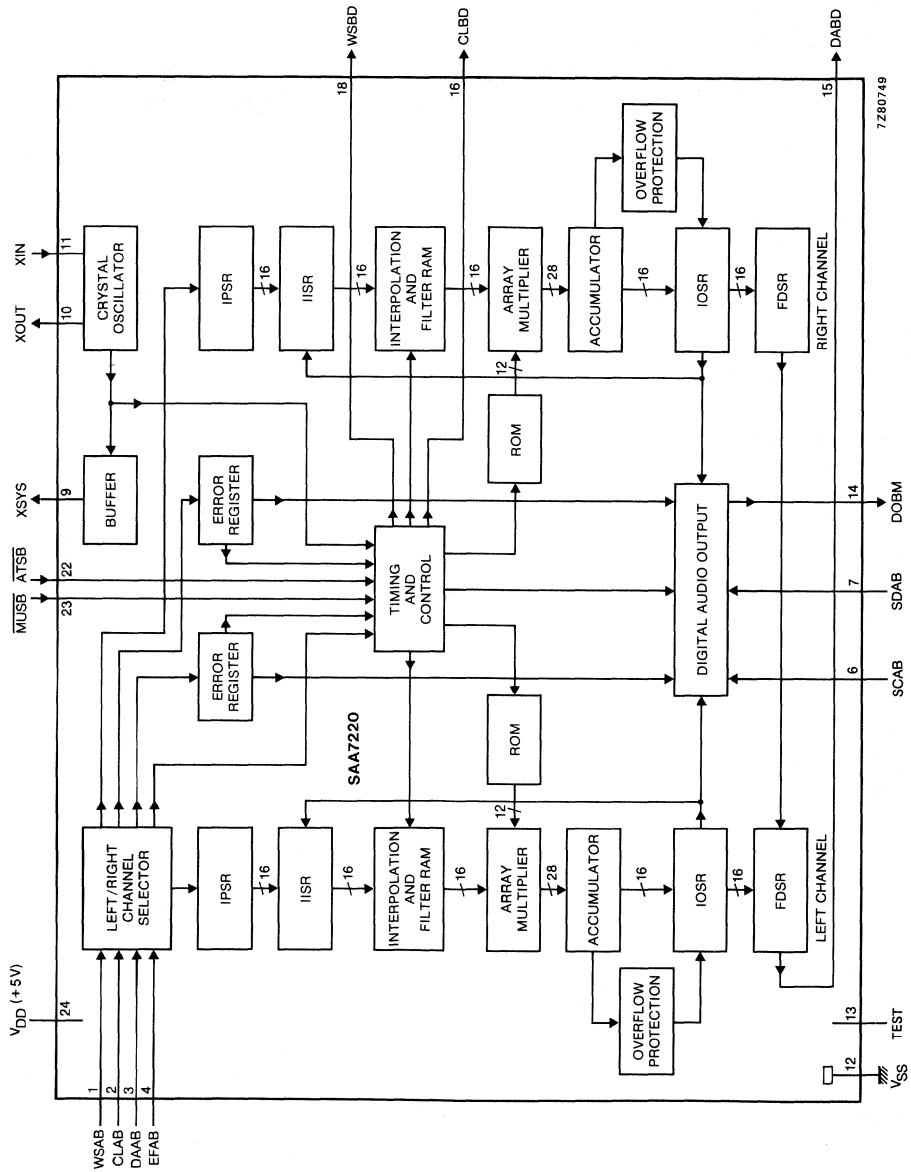
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 24)		V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)		I_{DD}	100	180	285	mA
Input voltage ranges						
WSAB, DAAB, EFAB, SDAB	note 2					
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$	note 3					
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Output voltage ranges						
DABD, CLBD, WSBD						
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
DOBM						
Voltage across a 75 Ω load via attenuator (peak-to-peak value)	see Fig. 10	$V_{L(p-p)}$	0,4	–	0,6	V
Operating frequency XTAL		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

For explanation of notes see "Notes to the characteristics".

PACKAGE OUTLINE

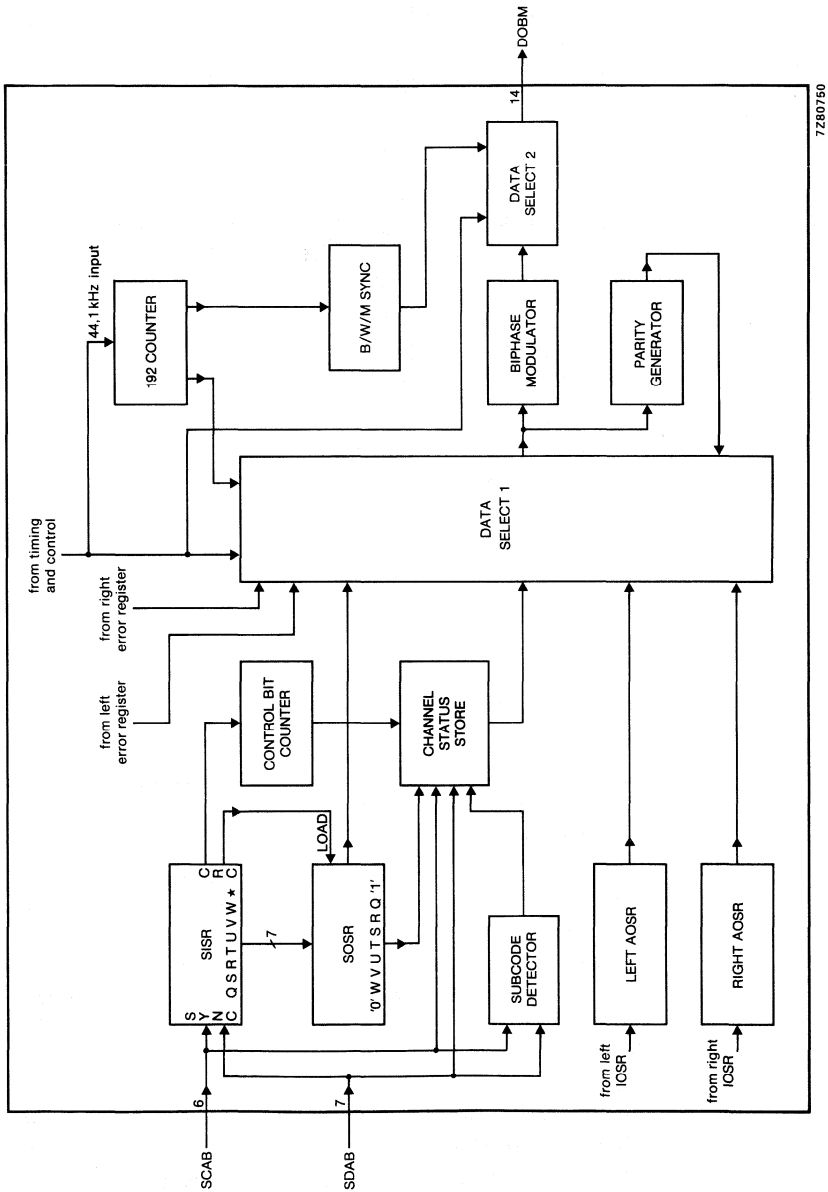
SAA7220P/A: 24-lead DIL; plastic (with internal heat spreader) (SOT101A).



Where:

IPSR = Input Shift Register
IISR = Intermediate Input Shift Register
IOSR = Intermediate Output Shift Register
FDSR = Filter Data Shift Register

Fig. 1 Digital filter block diagram.



Where:

SISR = Subcode Input Shift Register
SOSR = Subcode Output Shift Register
IOSR = Intermediate Output Shift Register
AOSR = Audio Output Shift Register
* = Subcode word error flag

Fig. 2 Digital audio output block diagram.

PINNING

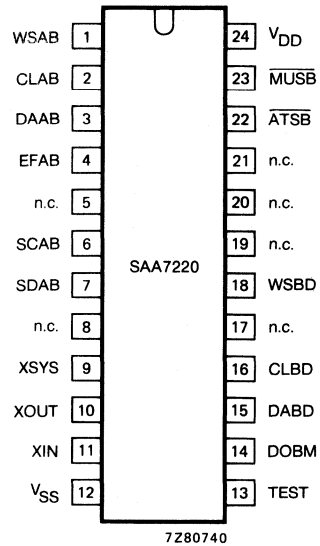


Fig. 3 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	WSAB	**Word Select:** input from A-chip.
2	CLAB	**Clock:** input from A-chip; has an internal pull-up.
3	DAAB	**Data:** input from A-chip.
4	EFAB	**Error Flag:** active HIGH input from A-chip indicating unreliable data. This input has an internal pull-down.
5	n.c.	not connected.
6	SCAB	**Subcode Clock:** a 10-bit burst clock 2,8224 MHz (typ.) input which synchronizes the subcode data. This input has an internal pull-up.
7	SDAB	**Subcode Data:** a 10-bit burst of data, including flags and sync bits serially input from the A-chip once per frame clocked by burst clock input SCAB (see Fig. 8). This input has an internal pull-down.
8	n.c.	not connected.
9	XSYS	**System clock output:** 11,2896 MHz (typ.) output to DAC and to A-chip as slave clock input.
10	XOUT	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
11	XIN	**Crystal oscillator input:** input from crystal oscillator or slave clock.

pin no.	mnemonic	description
12	V_{SS}	**Ground:** circuit earth potentional.
13	TEST	**Test input:** this input has an internal pull-down. In normal operation pin 13 should be open-circuit or connected to V_{SS}.
14	DOBM	**Digital audio output:** this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data. Transmission is by biphase-mark code.
15	DABD	**Data:** this output which is fed to the DAC, together with its clock (CLBD) and word select (WSBD) outputs, conforms to the I^2S format (see Fig. 7).
16	CLBD	**Clock:** output to DAC.
17	n.c.	not connected.
18	WSBD	**Word Select:** output to DAC.
19	n.c.	not connected.
20	n.c.	not connected.
21	n.c.	not connected.
22	$\overline{ATSB}$	**Attenuation:** when active LOW this control input provides −12 dB attenuation. This input has an internal pull-up.
23	$\overline{MUSB}$	**Mute:** active LOW control input with internal pull-up.
24	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).

FUNCTIONAL DESCRIPTION

General

The SAA7220 incorporates the following functions:

- Interpolation of data in error
- Attenuation
- Muting
- Finite impulse response transversal filtering with a four times increased sampling rate
- A digital audio output

Serial data formatted in two's complement (DAAB; pin 3) is clocked in by its bit clock (CLAB; pin 2) together with word select (WSAB; pin 1) and error flag (EFAB; pin 4) as shown in Fig. 1. After resynchronization with the internal clocks the data is separated into left and right channels and fed to two identical Input Shift Registers (IPSR). Internal timing and control loads the data into the interpolation RAM via the Intermediate Input Shift Register (IISR).

After interpolation, attenuation and muting the data is fed serially from the Intermediate Output Shift Register (IOSR) to the Audio Output Shift Register (AOSR) and to the IISR. From the IISR it is loaded into the filter RAM.

After filtering the data is passed to the Filter Data Shift Register (FDSR). From the FDSR it is transmitted serially to the data output (DABD; pin 15) together with the appropriate word select (WSBD; pin 18) and bit clock (CLBD; pin 16), in accordance with the I^2S bus specification. Data is again formatted in two's complement. Outputs DABD, WSBD and CLBD are strobed to maintain the correct timing relationship with the system clock output (XSYS) at pin 9 (see Fig. 13).

FUNCTIONAL DESCRIPTION (continued)

The subcode data (SDAB; pin 7) and 10-bit burst clock (SCAB; pin 6) are resynchronized to the internal clocks within the digital audio output block. SCAB clocks the data into the Subcode Input Shift Register (SISR; Fig. 2). Data is transferred to the Subcode Output Shift Register (SOSR) on receipt of all of the 10-bit burst clocks. The subcode data is then mixed with the data from the AOSR and the error flag to provide the output DOBM at pin 14. SISR is reset when no clocks are detected on the SCAB input.

Interpolation

When, for either left or right channel, unreliable samples are flagged between two correct samples, linear interpolation is used to replace the erroneous samples (up to a maximum of 8 consecutive errors).
When the error flag is set, the sample is replaced by a value calculated by the following formula:

$$S(n) = \frac{x}{x+1} \cdot S(n-1) + \frac{1}{x+1} \cdot S(n+x)$$

Where: S(n) = new sample value
x = number of successive erroneous samples following S (n−1)
S(n−1) = the preceding sample
S(n+x) = the first following correct sample

The value of x is detected (1 to 8) to determine the coefficients for the multiplications. Eight coefficient pairs are stored in the ROM. If x = 0 or ⩾ 9 then S(n) will remain unchanged.

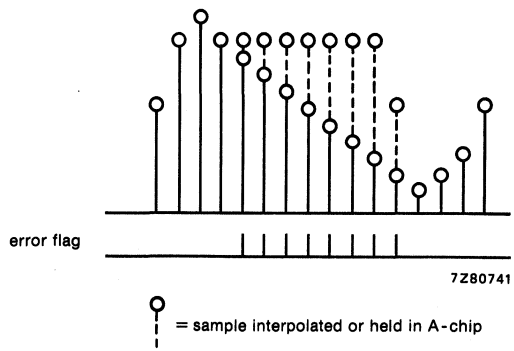


Fig. 4 Example of an eight sample linear interpolation.

Attenuation

Attenuation is controlled by the ATSB input at pin 22. When the input is active LOW the sample is multiplied by a coefficient that provides −12 dB attenuation. If the input is HIGH the multiplication factor is 1.

Mute

Mute is controlled by the MUSB input at pin 23. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. 32 coefficients are used to step down the value of the data, each one being used 31 times before stepping onto the next. When MUSB is released (pin 23 HIGH) the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order.

Filtering

The SAA7220 incorporates two identical finite impulse response transversal filters with the equivalent of 120 taps, one filter for each stereo channel. The corresponding 120 coefficients are structured as 4 sections of 30 coefficients.
(Each ROM contains only 60 filter coefficients, the same 60 being used a second time, but in the reverse order, to make a total of 120.) Plots of the filter characteristics are shown in Fig. 16.

Data is stored in a 480-bit RAM (30 words x 16 bits). The 30 words are sequentially addressed 4 times to generate the 4 output samples.

When a new word is moved from the interpolation RAM to the filter RAM, the oldest word is discarded and all other words moved one position with respect to the ROM coefficients. The data storage effectively forms a 30 sample wide moving window on the input data. The samples move within this window at 5,6448 MHz and the window moves one sample every 22,6 μs.

An output word is formed by multiplying 30 samples from the filter RAM with 30 coefficients from the ROM using a 16 x 12 array multiplier. The result is added in an accumulator. At the end of the 30 multiplications the 16 MSB's are passed from the accumulator via the IOSR to the FDSR, and the accumulator is reset. Overflow protection is incorporated so that the output always limits cleanly in the event of accumulator overflow. Also, to simplify the design of the digital-to-analogue converter a d.c. offset of + 5% is added to the accumulator.

The filtered data is output in the I^2S format at a 5,6448 MHz bit rate and a sample rate of 176,4 kHz.

Digital audio output

Audio 16-bit samples and subcode data are formatted according to the Philips/Sony proposal; "Digital audio interface for domestic use" (Reference Philips 'Red Book' CD-DA standard specification).
The digital audio output (DOBM; pin 14) consists of 32-bit words transmitted in biphase-mark code. That is, two transitions for a logic 1 and one transition for a logic 0. The 32-bit words are transmitted in blocks of 384 words. Table 1 shows the information contained in each word.
The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns (B, M and W) indicate the following situations:

- Sync B; start of a block of 384 words, contains left sample (11101000)
- Sync M; word contains left sample, but is not a block start (11100010)
- Sync W; word contains right sample (11100100)

In the SAA7220 sync words are always preceded by 0. A typical biphase-mark code output is shown in Fig. 11.

Left and right samples are transmitted alternately.
Audio samples are available for digital audio output after interpolation, attenuation and muting, but before filtering.
Data held in the Subcode Output Shift Register (SOSR) is transmitted via the user data bit and is asynchronous with the block rate.

Digital audio output (continued)

Table 1 Composition of the 32-bit digital audio output word

bit number	description	information
1 to 4	sync	–
5 to 8	auxiliary	not used (always zero)
9 to 28	audio sample	bits 9 to 12 not used (always zero). bits 13 (LSB) to 28 (MSB) two's complement
29	audio valid	copy of the error flag
30	user data	used for subcode data
31	channel status	indication of control bits and category code
32	parity bit	even parity for all word bits excluding sync pattern

Channel status

The channel status bit is the same for both left and right words. Therefore a block of 384 words contains 192 channel status bits as shown in Table 2.

When there is no subcode the channel status will switch over to the general format. 'No subcode' is identified by the subcode detector when SCAB is a continuous HIGH or LOW.

Table 2 Channel status bit assignment

bit number	description	subcode provided	no subcode provided
1 to 4	control	copy of Q channel	bits 1 and 2 zero bit 3 image of SCAB bit 4 image of SDAB
5 to 8	reserved	always zero	always zero
9 to 16	category code	CD category bit 9 logic 1	general category all bits zero
17 to 192		always zero	always zero

If a subcode clock is provided but there is no subcode data (SDAB is a continuous HIGH or LOW) the control bits will be zero and the category code will be CD.

The SYNC bit and the cyclic redundancy check bit (CRC) in the subcode data from the A-chip to the B-chip have the format shown by Fig. 5. Typical subcode data input waveforms are shown by Fig. 8.

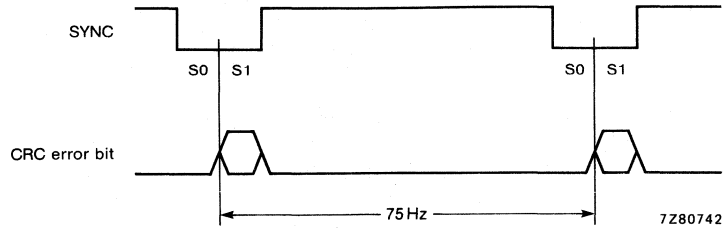


Fig. 5 Subcode data format for SYNC and CRC bits.

SYNC is active LOW and indicates the start of a subcode block, which contains 98 words including 2 sync words, S0 and S1.
CRC is always LOW except during SYNC S1 when:

- CRC = logic 1; previous Q block was true
- CRC = logic 0; previous Q block was false

Two 32-bit words are transmitted at the sample frequency of 44,1 kHz (2 x 32 x 44,1 kHz = 2,8224 Mbits/s data rate). An internal 5,6448 MHz clock (XSYS/2) is used in the biphase modulator.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0,5	–	+ 7,0	V
Maximum input voltage range	V_I	−0,5	–	V_{DD}+ 0,5	V
Storage temperature range	T_{stg}	−55	–	+ 125	°C
Operating temperature range	T_{amb}	−20	–	+ 70	°C
Electrostatic handling*	V_{es}	−1000	–	+ 1000	V

Ensure no electrical connections are made to the underside or ends of the package as there is the possibility of making accidental connection to the lead frame and/or internal heat spreader of the device.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 24)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)	I_{DD}	100	180	285	mA
Inputs					
WSAB, DAAB					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
EFAB, SDAB (note 2)					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 50	μA
Input capacitance	C_I	–	–	7	pF
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$ (note 3)					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−30	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
Crystal oscillator (see Fig. 9)					
Input XIN					
Output XOUT (note 4)					
Mutual conductance at 100 kHz	G_m	1,5	–	–	mA/V
Small signal voltage gain ($A_V = G_m \times R_O$)	A_V	3,5	–	–	V/V
Input capacitance	C_I	–	–	10	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Output capacitance	C_O	–	–	10	pF
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
Slave clock mode					
Input voltage (note 5) (peak-to-peak value)	$V_{I(p-p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW (note 6)	V_{IL}	0	–	1	V
Input voltage HIGH (note 6)	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 7)	t_r	–	–	20	ns
Input fall time (note 7)	t_f	–	–	20	ns
Input HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%
Outputs (note 4)					
DABD, CLBD, WSBD					
Output voltage LOW at I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
XSYS (note 8)					
Output voltage LOW	V_{OL}	0	–	0,4	V
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
DOBM					
Voltage across a 75 Ω load via attenuator; see Fig. 10 (peak-to-peak value)	$V_{L(p-p)}$	0,4	–	0,6	V
D.C. offset voltage	V_{LDC}	–0,05	–	+ 0,05	V
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Inputs (see Fig. 12)					
SCAB, CLAB (note 9)					
SCAB clock frequency (burst clock)	f_{SCAB}	–	2,8224	–	MHz
CLAB clock frequency	f_{CLAB}	–	2,8224	–	MHz
or (note 10)	f_{CLAB}	–	1,4112	–	MHz
Clock LOW time	t_{CKL}	110	–	–	ns
Clock HIGH time	t_{CKH}	110	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAAB, WSAB, EFAB (note 11)					
Data set-up time	$t_{SU;DAT}$	40	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
SDAB (note 12)					
Subcode data set-up time	$t_{SU;SDAT}$	40	–	–	ns
Subcode data hold time	$t_{HD;SDAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
Outputs (see Figs 13 and 14)					
WSBD (notes 9 and 13)					
Word select set-up time	$t_{SU;WS}$	40	–	–	ns
Word select hold time	$t_{HD;WS}$	0	–	–	ns
WSBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 13)					
Data set-up time	$t_{SU;DATD}$	40	–	–	ns
Data hold time	$t_{HD;DATD}$	0	–	–	ns
DABD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
CLBD (notes 9 and 13)					
Clock period	t_{CK}	161	177	197	ns
Clock LOW time	t_{CKL}	65	–	–	ns
Clock HIGH time	t_{CKH}	65	–	–	ns
Clock set-up time	$t_{SU;CLD}$	40	–	–	ns
Clock hold time	$t_{HD;CLD}$	0	–	–	ns
CLBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 14)					
Data set-up time	$t_{SU;DATBD}$	40	–	–	ns
Data hold time	$t_{HD;DATBD}$	60	–	–	ns

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
WSBD (notes 9 and 14)					
Word select set-up time	$t_{SU;DATWSD}$	40	–	–	ns
Word select hold time	$t_{HD;DATWSD}$	60	–	–	ns
DOBM (note 15)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Data bit 0 (note 16)					
pulse width HIGH	$t_{HIGH(0)}$	336	354	372	ns
pulse width LOW	$t_{LOW(0)}$	336	354	372	ns
Data bit 1 (note 17)					
pulse width HIGH	$t_{HIGH(1)}$	172	177	182	ns
pulse width LOW	$t_{LOW(1)}$	172	177	182	ns
XSYS					
Output rise time (note 9)	t_r	–	–	20	ns
Output fall time (note 9)	t_f	–	–	20	ns
Output HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

A Philips publication "I²S bus specification" is available on request.

Notes to the characteristics

1. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
2. Inputs EFAB and SDAB both have internal pull-downs.
3. Inputs CLAB, SCAB, $\overline{ATSB}$ and $\overline{MUSB}$ have internal pull-ups.
4. All outputs are short-circuit protected except crystal oscillator output.
5. If used in a.c. coupled mode.
6. $V_{IH} - V_{IL} \geqslant 1{,}6$ V.
7. Reference levels = 10% and 90%.
8. The output current conditions are dependent on the drive conditions.
   When a crystal oscillator is being used the output current capability is $I_{OL} = +0{,}8$ mA; $I_{OH} = -0{,}2$ mA. But if a slave input is being used the output currents are reduced to $I_{OL} = +0{,}2$ mA; $I_{OH} = -0{,}2$ mA.
9. Reference levels = 0,8 V and 2,0 V.
10. The signal CLAB can run at either 2,8 MHz (1/4 system clock) or 1,4 MHz (1/8 system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being 1/4 or 1/8 of the system clock frequency.
11. Input set-up and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0,8 V and 2,0 V.
12. Input set-up and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0,8 V and 2,0 V.
13. Output set-up and hold times measured with respect to system clock output (XSYS).
14. Output set-up and hold times measured with respect to clock output (CLBD).
15. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.
16. Data bit 0 pulse width times are typically system clock period $(1/f_{XTAL}) \times 4$. Maximum and minimum values are ± 5% of this time. Values shown are for $f_{XTAL} = 11{,}2896$ MHz, but these will change accordingly if f_{XTAL} changes.
17. Data bit 1 pulse width times are typically system clock period $(1/f_{XTAL}) \times 2$. Maximum and minimum values are ± 2,5% of this time. Values shown are for $f_{XTAL} = 11{,}2896$ MHz, but these will change accordingly if f_{XTAL} changes.

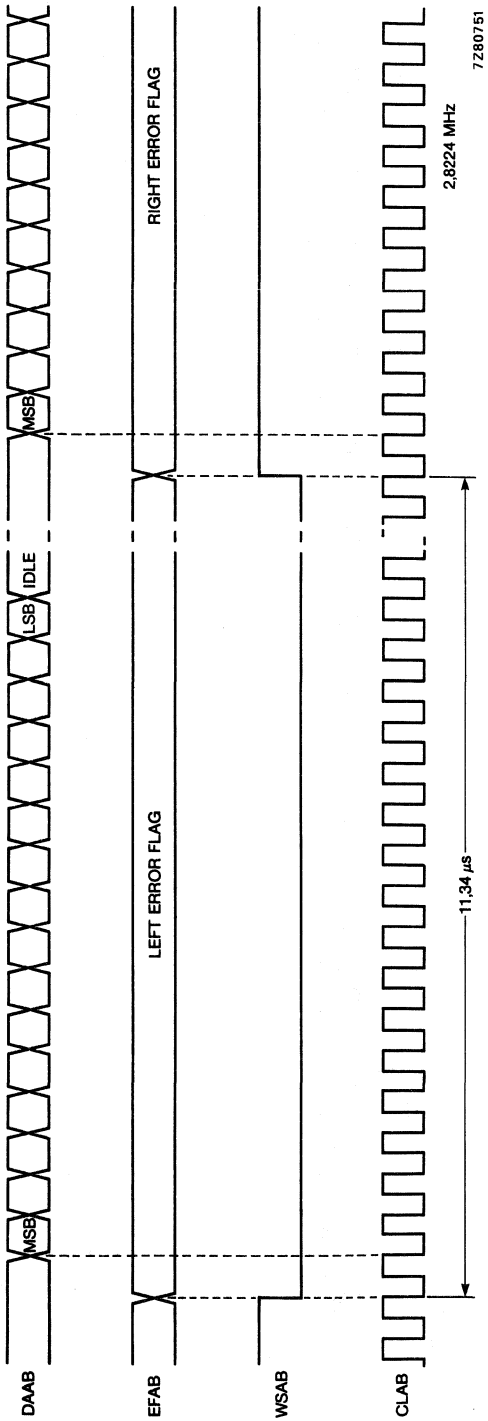


Fig. 6(a) Typical sample data input waveforms from A-chip at 2,8 MHz.

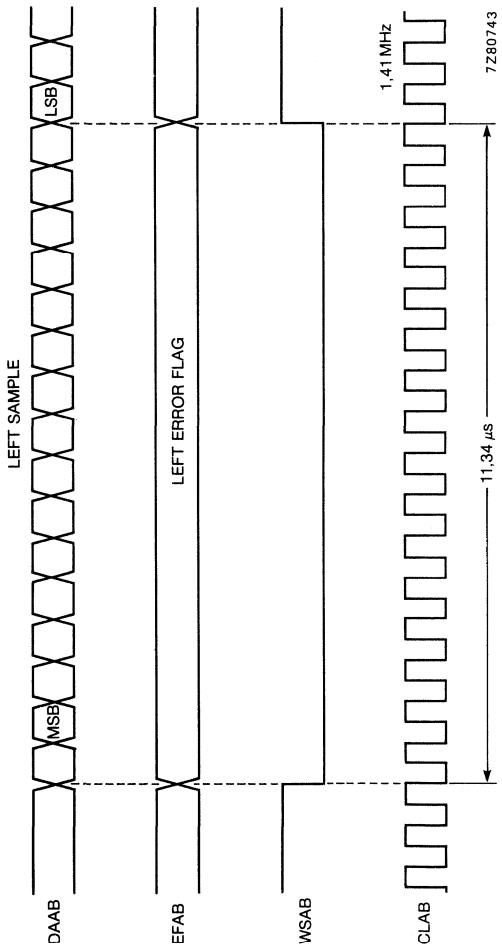


Fig. 6(b) Typical sample data input waveforms at 1,4 MHz.

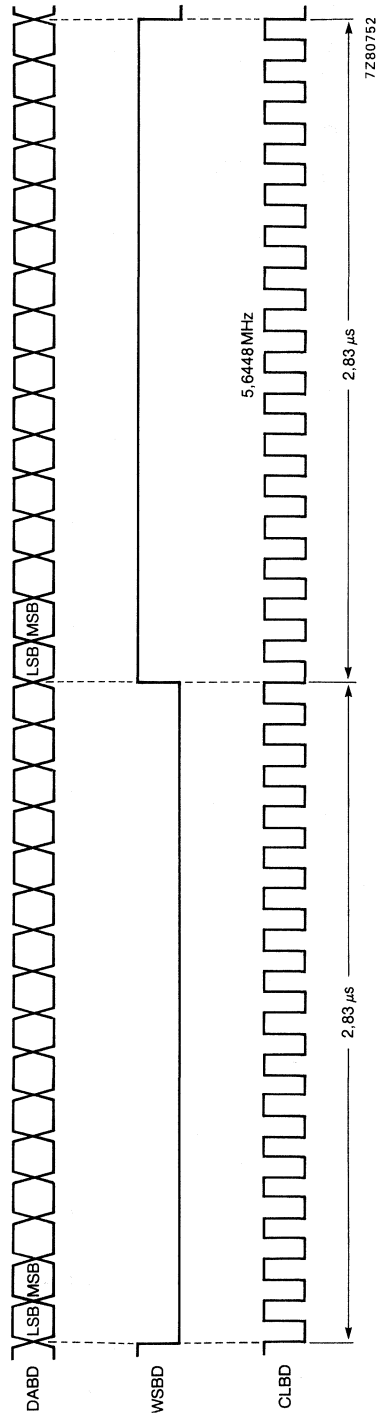
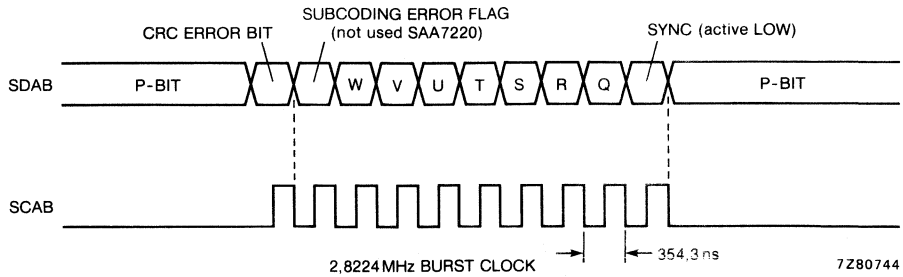
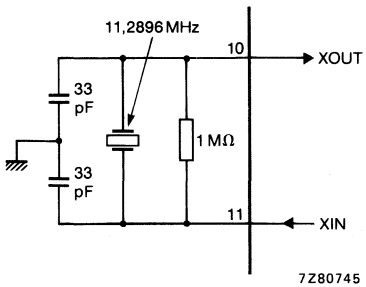


Fig. 7 Typical sample data output waveforms to DAC.



Subcode word frequency = 7,35 kHz.

Fig. 8 Typical subcode data input waveforms.



Oscillator catalogue no. 4322 143 05031

Fig. 9 Crystal oscillator circuit.

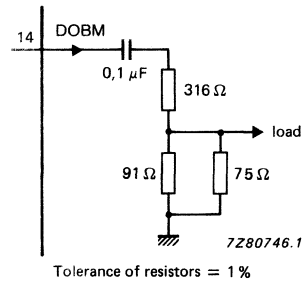


Fig. 10 Digital audio output load.

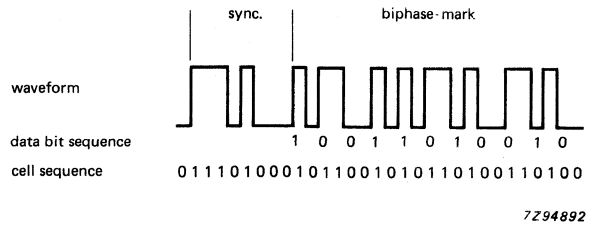


Fig. 11 Biphase-mark code.

TIMING

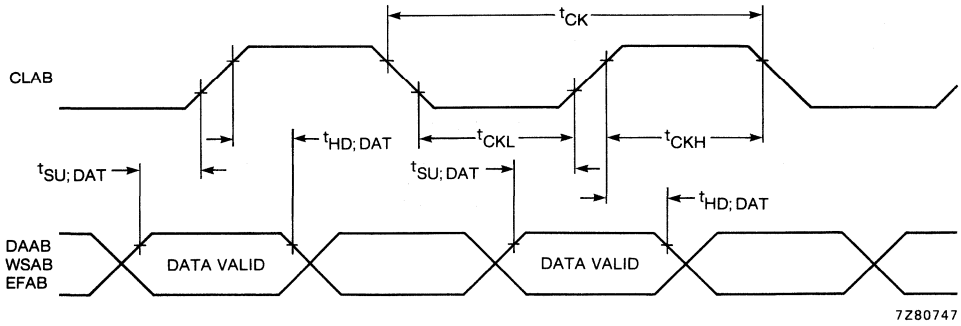


Fig. 12 Data input timings; reference levels = 0,8 V and 2,0 V.
(also applicable to subcode data input ($t_{SU;\,SDAT}$ and $t_{HD;\,SDAT}$).

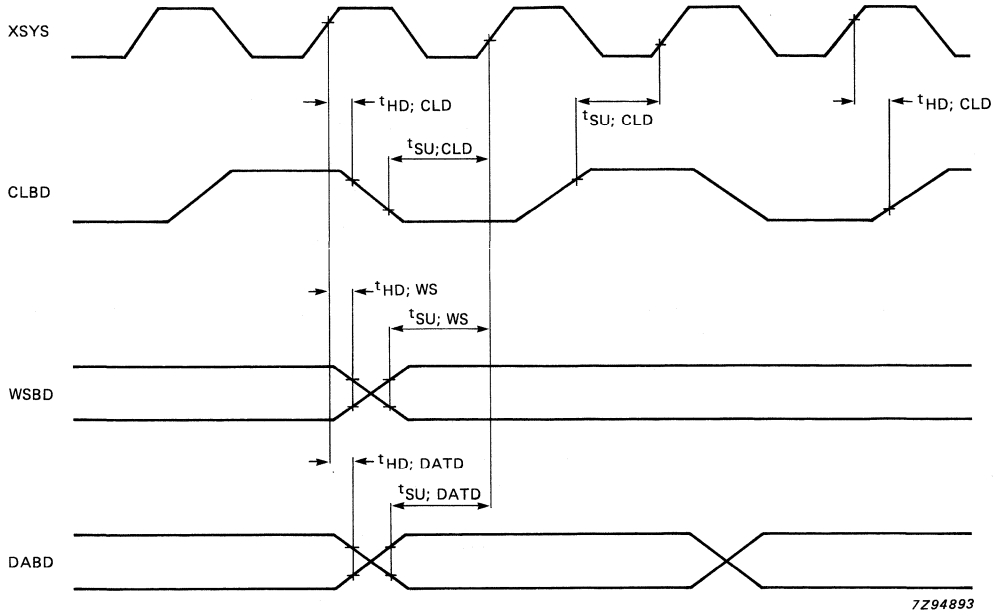


Fig. 13 Data output timings with respect to system clock output (XSYS); reference levels = 0,8 V and 2,0 V.

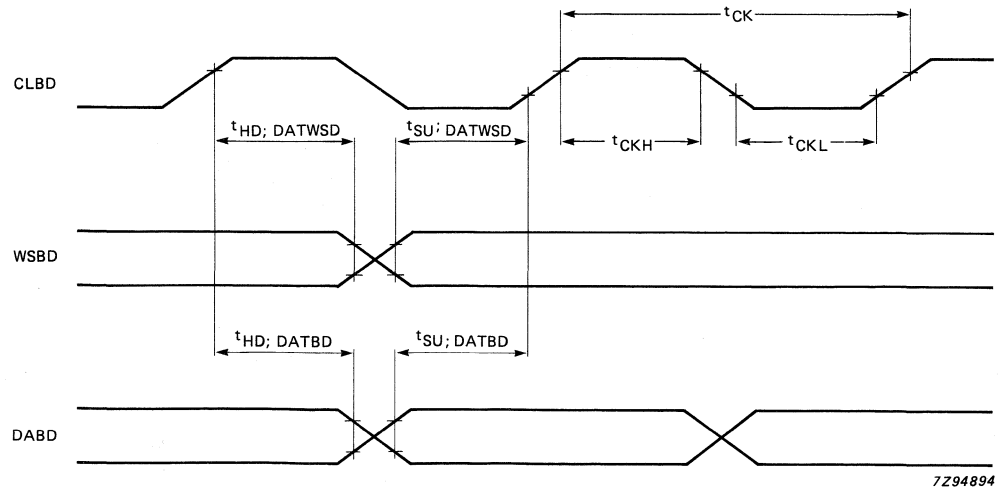


Fig. 14 Data output timings with respect to clock output (CLBD); reference levels = 0,8 V and 2,0 V.

APPLICATION INFORMATION

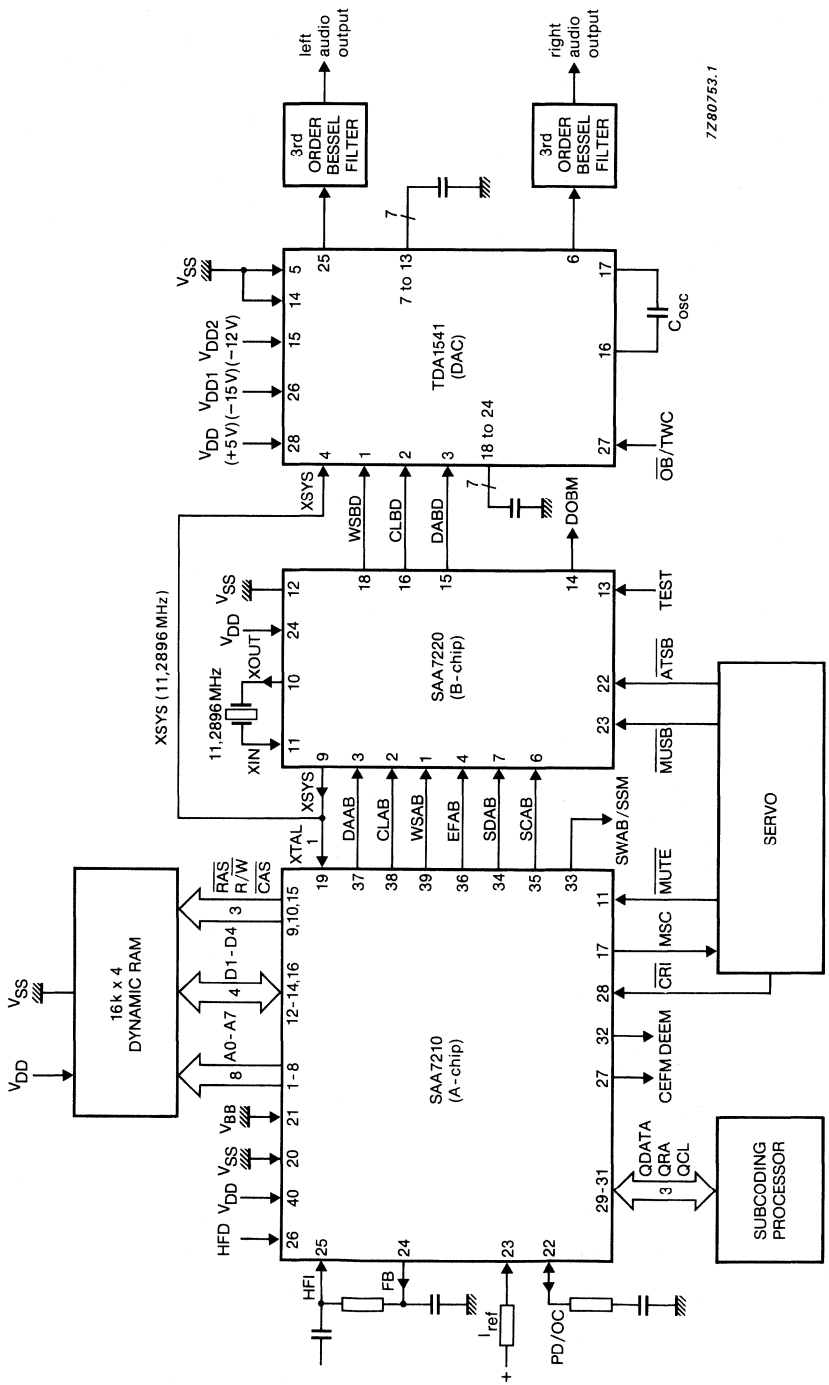


Fig. 15 System application diagram.

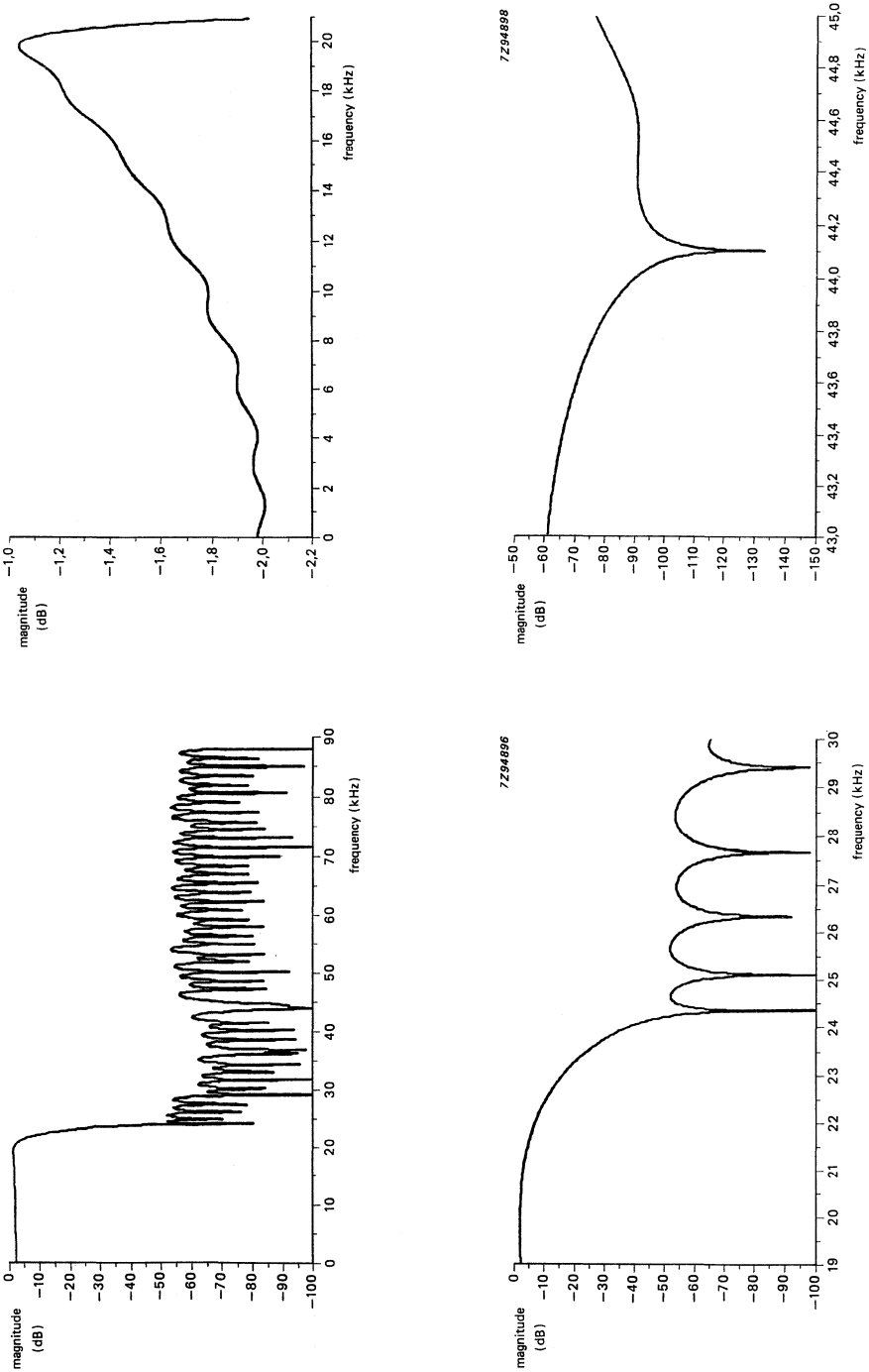


Fig. 16 Digital filter characteristics; magnitude as a function of frequency.

AUDIO DIGITAL INPUT CIRCUIT (ADIC)

GENERAL DESCRIPTION

The SAA7274 is an Audio Digital Input Circuit (ADIC) which converts digital audio signals in accordance with the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 into an equivalent binary value of data and control bits. The output function of this device is to convert the equivalent binary value of the data bits (for each channel) into a serial digital audio signal which conforms to the I²S format.

Features

- I²S bus output
- Biphase audio signal (Satellite radio, compact disc and DAT)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	–	5.5	V
Inputs	except IBIFA					
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current	V_I = 0 V	$-I_I$	–	–	1	μA
	V_I = 5.5 V	I_I	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
Output voltage HIGH		V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW		V_{OL}	–	–	0.4	V
Operating ambient temperature range		T_{amb}	–40	–	+70	°C

PACKAGE OUTLINES

SAA7274P: 24-lead DIL; plastic (SOT101A).
SAA7274T: 24-lead mini-pack; plastic (SO24; SOT137A).

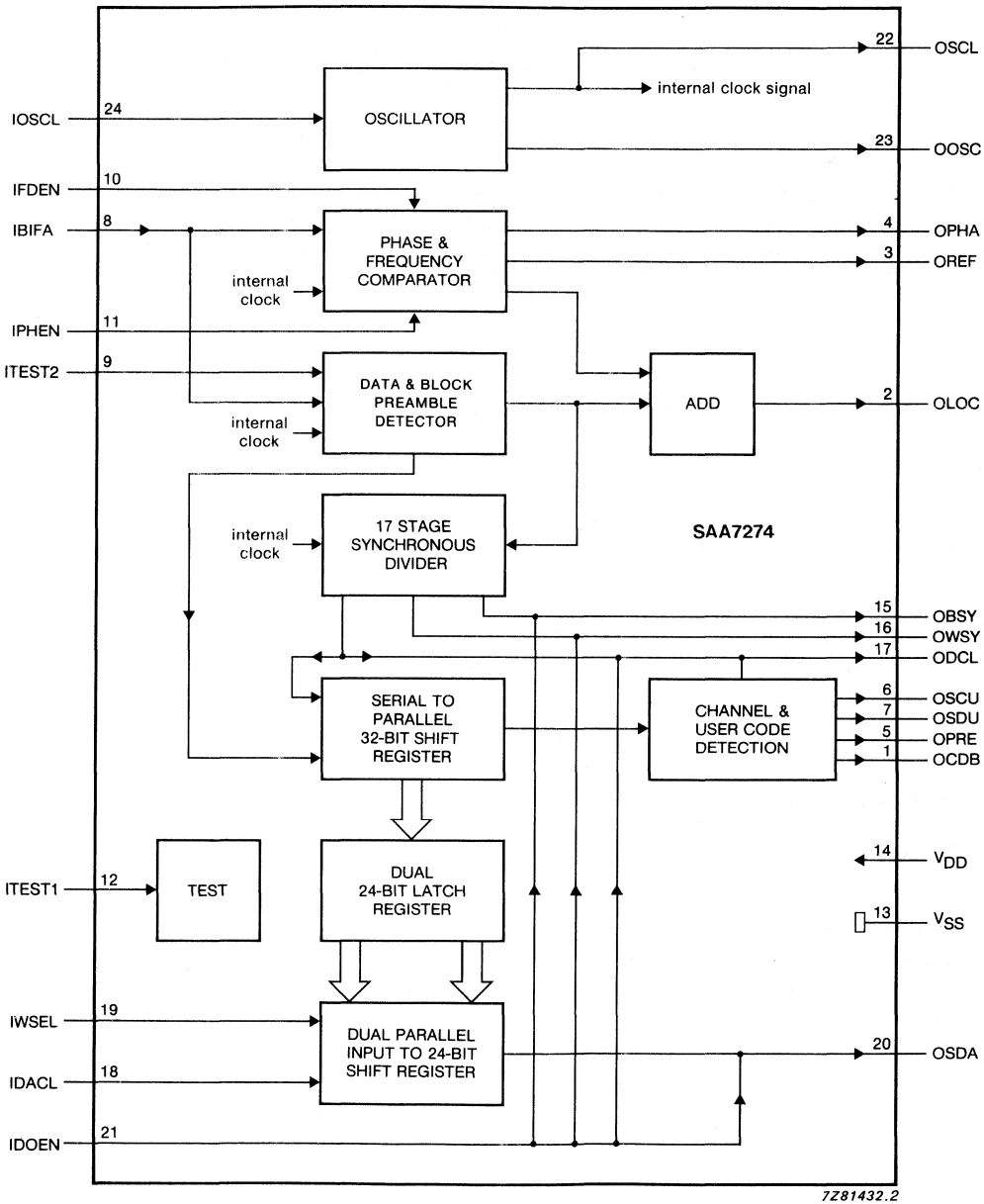


Fig.1 Block diagram.

PINNING

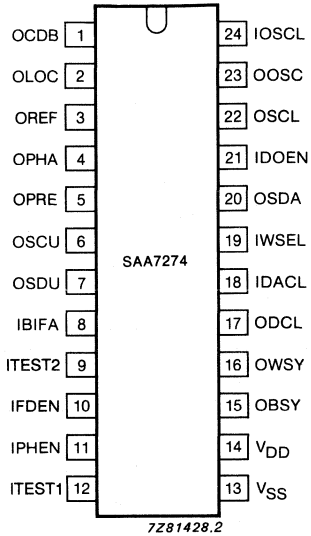


Fig.2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (5 V)
V_{SS}	ground (0 V)

Inputs (CMOS protection)

IBIFA	biphase input signal (min. 1 MHz; max. 3.1 MHz)
IFDEN	frequency detector enable
IPHEN	phase-locked loop edge selector
ITEST1	test input enable
ITEST2	test input enable
IDACL	data clock input signal (max. 5 MHz)
IWSEL	word select input signal (max. 50 kHz)
IDOEN	output enable
IOSCL	clock oscillator input (min. 8 MHz; max. 12.5 MHz)

Outputs (CMOS push-pull)

OCDB	control data bits (max. 400 kHz)
OLOC	out-of-lock signal
OREF	phase reference signal (max. 6.2 MHz)
OPHA	phase output signal (max. 6.2 MHz)
OPRE	pre-emphasis level
OSCU	user clock/copy-bit signal (max. 3.1 MHz)
OSDU	user data/pre-emphasis (max. 3.1 MHz)
OSCL	system clock buffer (min. 8 MHz; max. 12.5 MHz)
OOSC	clock oscillator output (min. 8 MHz; max. 12.5 MHz)

Outputs (3-state push-pull)

OBSY	block synchronization output signal (1/49152 system clock)
OWSY	word clock output signal (1/256 system clock)
ODCL	data clock output signal (1/4 system clock)
OSDA	data output signal (max. 2.5 MHz)

FUNCTIONAL DESCRIPTION

Main function

The biphase input signal must conform to the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 format, as well as satisfying the following conditions:

- number of channels: 2
- transmission code: biphase mark
- synchronization method: biphase violation
- number of data bits: 24, starting with the LSB
- number of control bits: 4
- preamble values:

preceding cell	0	1
block preamble	11101000	00010111

The main function performs the following tasks:

- Provides the output function with the equivalent binary value of the data bits separately for each of the two channels. These values are available until new information is received.
- Generates an out-of-lock output signal (OLOC) which is HIGH when the frequency of the biphase input signal is equal to 1/4 of the system clock frequency and when the block preambles are detected in the biphase input signal.
- If the biphase input signal is not present after 32 clock pulses, then the output OSCU is forced HIGH and outputs OSDU, OPRE, OLOC, OCDB and OSDA are forced LOW.
- Generates a data clock output signal (ODCL) with a frequency of 1/4 of the system clock. When a block preamble is detected in the biphase input signal ODCL is synchronized to a LOW value.
- Generates a word clock output signal (OWSY) with a frequency of 1/256 of the system clock. When a block preamble is detected in the biphase input signal OWSY is synchronized to a LOW value.
- Generates a block synchronization output signal (OBSY). This signal is HIGH during 4 system clock periods and has a frequency of 1/49152 of the system clock. The signal is synchronized with the block preambles of the biphase input signal.
- Generates a phase output signal (OPHA) and a phase reference signal (OREF). If the frequency of the biphase input signal (IBIFA) equals 1/4 of the system clock frequency ($f_{IOSCL}/4$) then the IC generates OPHA and OREF as shown in Fig.3.
  If the frequency of the biphase input signal (IBIFA) is greater or less than 1/4 of the system clock frequency then the IC generates OPHA and OREF as shown in Fig.4.

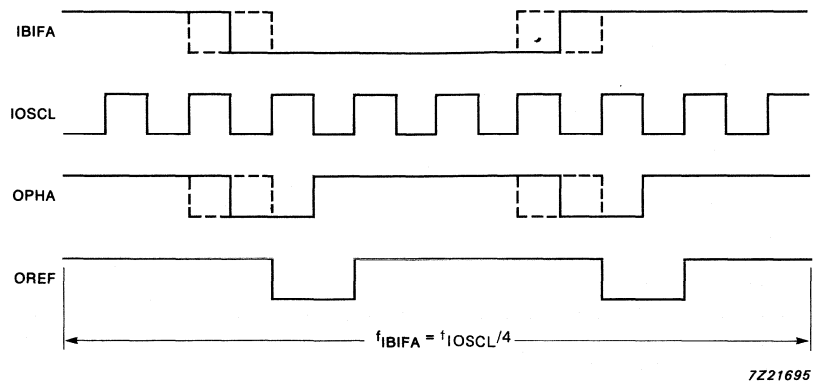


Fig.3 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

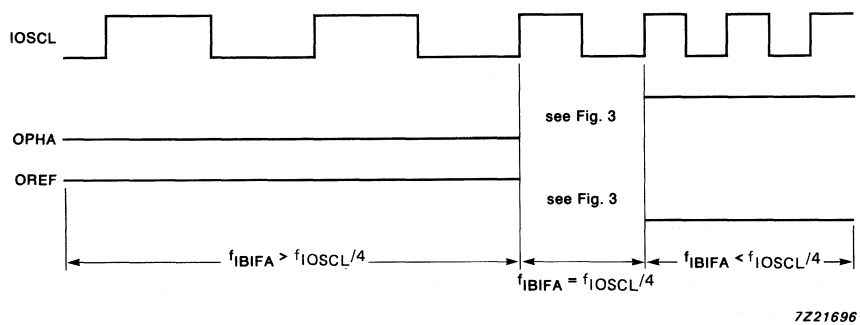


Fig.4 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} \neq f_{IOSCL}/4$.

Output function

The output function performs the following tasks:

- Provides the data output (OSDA) with the data bits from each channel in the following order:

MSB . . . . . LSB 0 0 0 0 0 0 0 0

- Outputs the data of the right and left channel. When word select input signal (IWSEL) is HIGH the data of the right channel is output and when LOW the data of the left channel is output.
- Delivers serial data to the OSDA output, if IDOEN = HIGH. This occurs on each negative transition of the data clock input signal (IDACL). Following a status change at the word select input (IWSEL), the data (MSB first) is output on the first negative transition of IDACL. If the number of clock pulses in a word exceeds 24, then the following bits will be internally set to zero.

FUNCTIONAL DESCRIPTION (continued)

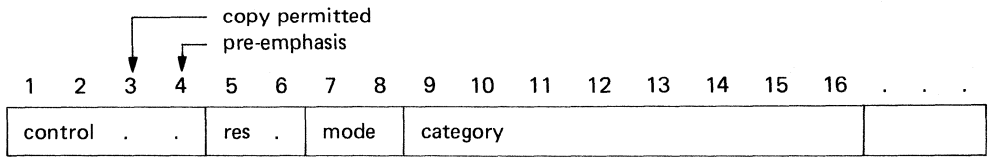
- Generates the following subcodes:

series 1,	0	0	U1	T1	S1	R1	Q1	1	0	0
series 2,	CRC	0	V1	U1	T1	S1	R1	Q1	1	0
series 3,	0	0	W1	V1	U1	T1	S1	R1	Q1	1

and after receiving the next user byte:

series 4,	0	0	W2	V2	U2	T2	S2	R2	Q2	1 etc.

- If the value of the category bits, bits 9 to 16 of the input signal, = 10000000 (compact disc format) and the value of the mode bits, bits 7 and 8, = 00, the user data output (OSDU) will deliver the bits of the subcode following the specified lay-out (above). The subcode starts only after receipt of at least 16 zero bits. Simultaneously a user clock signal (OSCU) consisting of 10 clock pulses is present. The output signal starts when a subcode is completed and is clocked on the negative transition of OSCU. The first data word of each subcode frame is output 3 times in succession with the data pattern shifted each time as outlined for series 1 through series 3 in the layout given above. The CRC performs a check on the 96 Q bits of the preceding subcode. If CRC is correct then the CRC bit = 1.
- Channel status:



If the value of the category bits **do not** equal 10000000 (compact disc format) and the value of the mode bits equals 00 (mode 0), then:

output OSDU indicates the status of bit 4 (pre-emphasis) of the channel status and output OSCU indicates the status of bit 3 (copy permitted) of the channel status provided the control bits conform to the 2-channel audio signal format.

- Uses the output pre-emphasis (OPRE) to indicate the status of bit 4 of the channel status for a 2-channel audio signal.
- Outputs the 4 control bits of the biphase input signal (IBIFA) represented by V, U, C and P at OCDB. The output delivers the bits in the same sequence during the next word, each bit continues for 32 clock pulses.

Additional input and output signals

The following input and output signals are available from this circuit:

- Phase output signal (OPHA) and phase reference signal (OREF) for use in a phase-locked loop (PLL). The OPHA signal is a result of the difference between the frequency and phase of the biphase input signal and the system clock. OREF signal provides the reference signal for the PLL.
- Input signal IFDEN enables the frequency detector. The frequency detection as present in the 2 signals OPHA and OREF can be enabled by making this signal LOW.
- Data clock output signal (ODCL), which has a frequency of 1/4 of the system clock frequency.
- Word clock output signal (OWSY), which has a frequency of 1/256 of the system clock frequency.
- Block synchronization output signal (OBSY), which has a frequency of 1/49152 of the system clock.
- ODCL, OWSY and OBSY will be synchronized to the block preambles in the biphase input signal IBIFA.

- Outputs ODCL, OWSY, OBSY and OSDA are enabled via a 3-state mode with a HIGH level on input IDOEN.
- IPHEN input selects dual or single edge detection of the input signal IBIFA in the phase detector. A low level selects the single-edge detection mode.
- Out-of-lock signal (OLOC). This output is LOW if the PLL is out-of-lock, or no block preambles are present in the biphase input signal IBIFA.
- User data/pre-emphasis output signal (OSDU). After receiving a category code of mode 0 from a non-compact disc source this signal outputs the pre-emphasis bit of the channel status bits in the biphase input signal. If the category code of mode 0 is from a compact disc source then the user data bits from the subcode channel including the CRC check on the 96 preceding Q bits are output.
- User clock/copy bit output signal (OSCU). After receiving a category code of mode 0 from a non-compact disc source then the copy bit of the channel status bits in the biphase input signal is output. If the category code of mode 0 is from a compact disc source then 10 clock pulses for the 'user data' are output.
- Pre-emphasis level output signal (OPRE), which indicates the value of the pre-emphasis bit of the channel status bits after receiving the two-channel audio fromat in the biphase input signal (IBIFA).
- Control data bits output signal (OCDB), which contains the 4 control bits of each word of the biphase input signal.
- The inputs ITEST1 and ITEST2 are used for device tests at the factory only, for normal operation they have to be connected to V_{SS}.

Clock oscillator

The clock oscillator of the circuit can be formed by connecting a crystal or a ceramic resonator between the oscillator input and output pins.

The circuit can also be driven by an external signal source applied to the oscillator input. The oscillator output is buffered and available at pin OSCL. The internal circuitry is driven via an inverter, which is connected to the buffered output. This allows all the output signals (especially ODCL, OWSY and OBSY) to change their state after a pulse from OSCL, independent of the capacitive load of the OSCL pin. All output signals of the circuit are triggered on the positive transition of the buffered OSCL signal.

Application note

If the capacitive load is to high for the SAA7274, a buffer circuit can be used. A suitable device is the PC74HC126 (3-state quad buffer/line driver). The input IDOEN to the SAA7274 must be made HIGH and the original 3-state enable signal must be connected to the OE inputs of the PC74HC126 (pins 1, 4, 10 and 13). Because the capacitive load of the SAA7274 is very low, the loss of speed is limited.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	7.0	V
Input voltage	note 1	V_I	−0.5	V_{DD}+0.5	V
Maximum input current		I_{IM}	−	±10	mA
Maximum output current		I_{OM}	−	±10	mA
Maximum supply current		I_{SS}, I_{DD}	−	±50	mA
Total power dissipation		P_{tot}	−	500	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−40	+70	°C

Note

1. Input voltage should not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current	note 1	I_{DD}	–	–	250	μA
	note 2	I_{DD}	–	10	–	mA
Inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current	$V_{SS} \leqslant V_I \leqslant V_{DD}$	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
OSCL						
Output voltage HIGH	$-I_{OH}$ = 8 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
OCDB, OLOC, OREF, OPHA, OPRE, OSCU, OSDU, OSDA						
Output voltage HIGH	$-I_{OH}$ = 2 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
OBSY, OWSY, ODCL, OOSC						
Output voltage HIGH	$-I_{OH}$ = 1.5 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 1.5 mA	V_{OL}	–	–	0.4	V
OSDA, ODCL, OWSY, OBSY						
Output leakage current	3-state	$\|I_{LO}\|$	–	–	15	μA

Notes to the DC characteristics

1. All inputs at V_{DD} or V_{SS}, except ITEST2 on V_{SS}, all outputs open circuit.
2. f_{OSCL} = 11.3 MHz.

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 70 °C; load capacitance (C_L): OSCL = 50 pF; OWSY, ODCL, OSDA = 30 pF (see application note); all other outputs = 20 pF; clock frequency f_{IOSCL} = ⩽ 12.5 MHz; IOSCL timing pulse LOW, t_{LOW} ⩾ 37 ns; rise and fall times, t_r, t_f = ⩽ 10 ns; delay lines are specified from clock input = 50% V_{DD} to output = 50% V_{DD}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Set-up and hold times						
IWSEL to IDACL	see Fig.5					
Data set-up time		t_{SU}	1	–	–	*
Data hold time		t_{HD}	–	–	1	*
Proagation delays						
IOSCL to OSCL		t_p	–	–	25	ns
IDACL to OSDA		t_p	–	–	60	ns
OSCL to OWSY and ODCL		t_p	5	–	50	ns
Rise and fall times						
OSCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	10	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	15	ns
OWSY and ODCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	15	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	25	ns

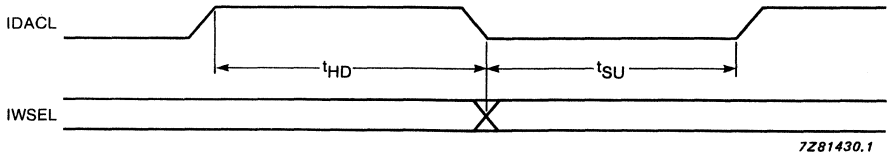
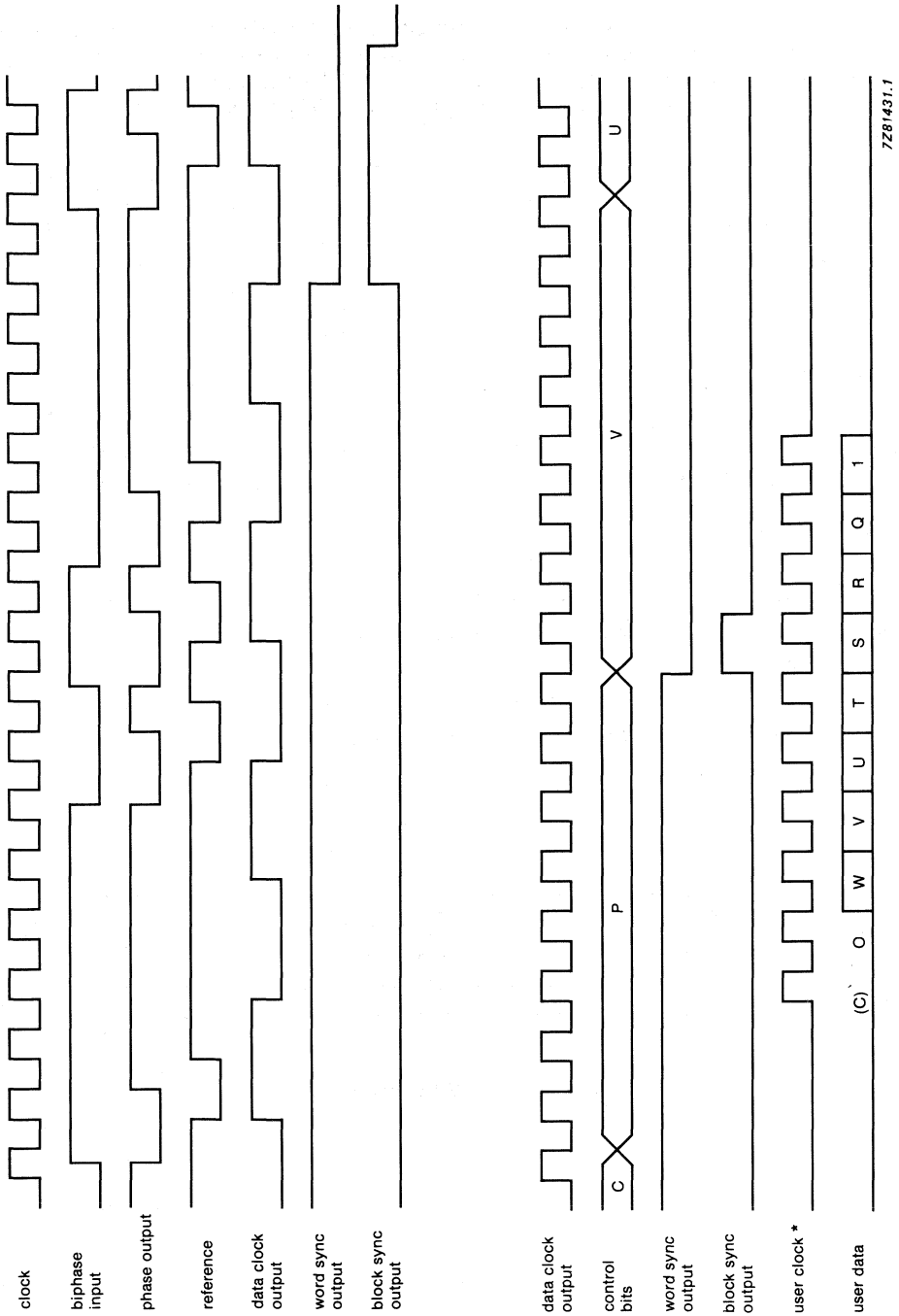


Fig.5 Set-up and hold time diagram.

* Clock periods of OSCL.



* user clock pattern is not necessarily synchronous with the block sync signal.

Fig.6 Timing diagram.

CMOS DECODER FOR COMPACT DISC SYSTEMS

GENERAL DESCRIPTION

The SAA7310 (CD3A) incorporates the functions of demodulator, subcoding processor, motor speed control, error corrector and concealment in one CMOS chip. The device accepts data from the disc and outputs serial data via the Inter IC signal bus (I^2S) directly to a digital-to-analogue converter (such as the stereo CMOS dual DAC; SAA7320). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering. The SAA7310 is available in both 40-pin DIL and 44-pin QFP packages.

Features

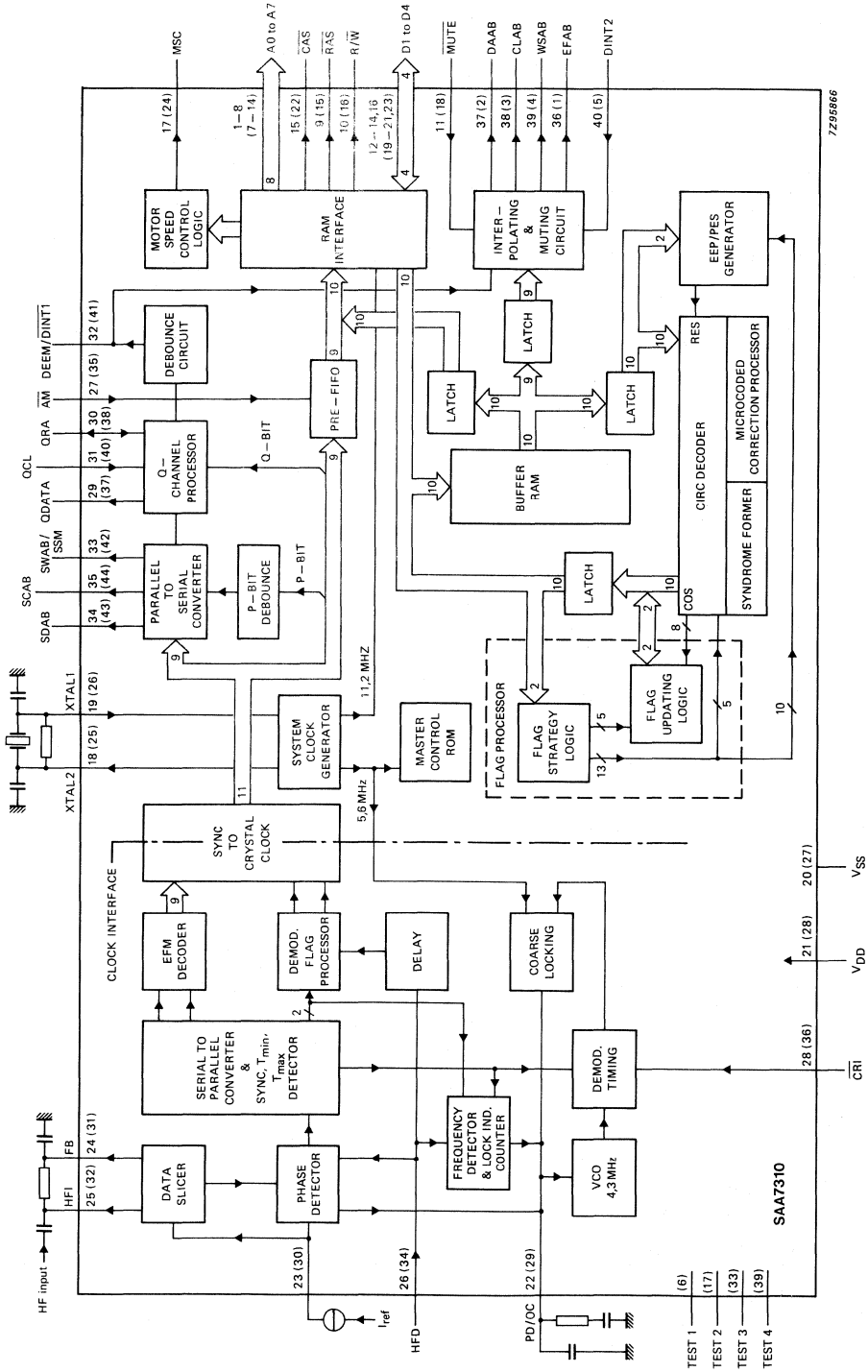
- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Adaptive CIRC error correction enabling 4 erroneous symbols per frame (32 symbols) to be corrected
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange
- Bidirectional data bus to external RAM (16 K x 4 bits) with 64-frame FIFO capacity
- Demodulator PLL requiring virtually no peripheral components
- Replacement for the CD2A
- Low power consumption (typ. 175 mW)
- Track loss correction by additional muting
- Non-digital audio interface application (such as CD-ROM or CD-I)
- 2-package option
- −40 to +85 °C operating temperature range

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	35	50	mA
Data slicer input voltage (peak-to-peak value)	$V_{I(p-p)}$	0,5	–	2,5	V
Oscillator operating frequency XTAL	f_{XTAL}	10,16	11,2896	12,42	MHz
VCO (PLL locked on to data)	f_{VCO1}	2,54	4,3218	6,21	MHz
Output current (each output)	I_O	−10	–	+ 10	mA
Operating ambient temperature	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINES

SAA7310P : 40-lead DIL; plastic (SOT-129).
SAA7310GP : 44-lead QFP; plastic (SOT-205A).



Pins in parenthesis relate to 44-pin QFP package.

Fig. 1 Block diagram.

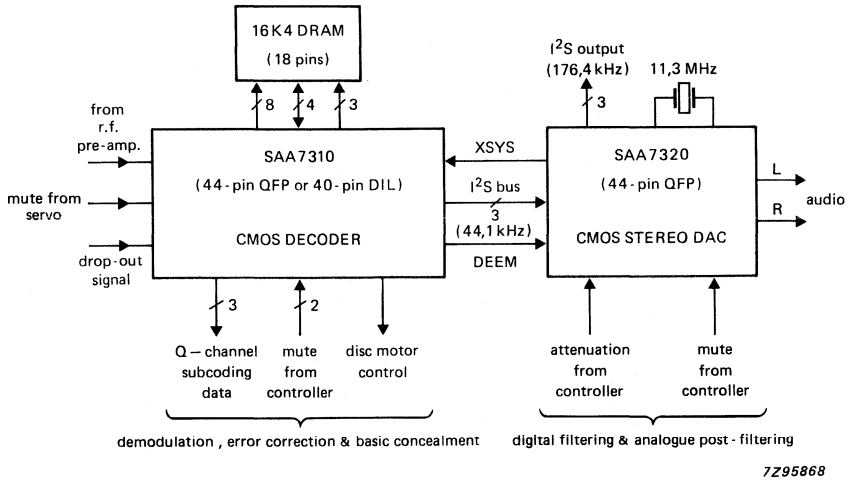


Fig. 2 (a) Block diagram of SAA7310 as used with SAA7320.

DEVELOPMENT DATA

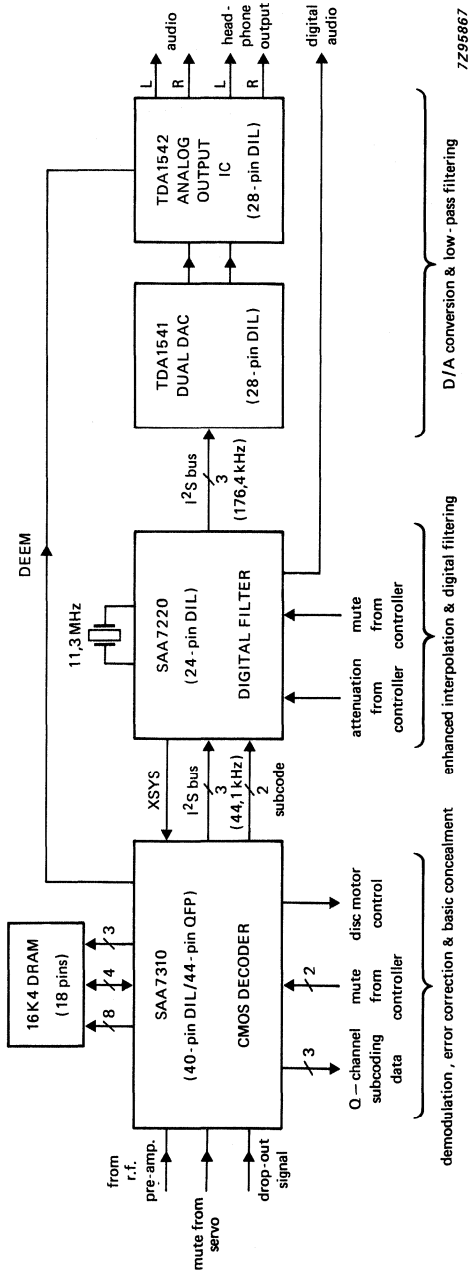


Fig. 2 (b) Block diagram of SAA7310 as used with SAA7220.

DEVELOPMENT DATA

PINNING

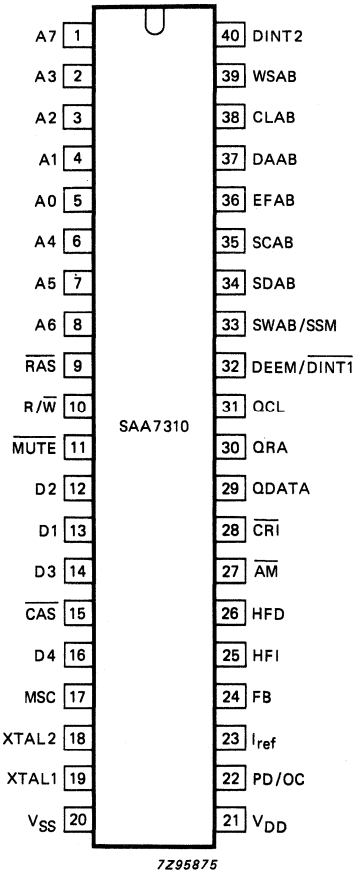


Fig. 3 Pinning diagram; for 40-lead DIL package.

PINNING (continued)

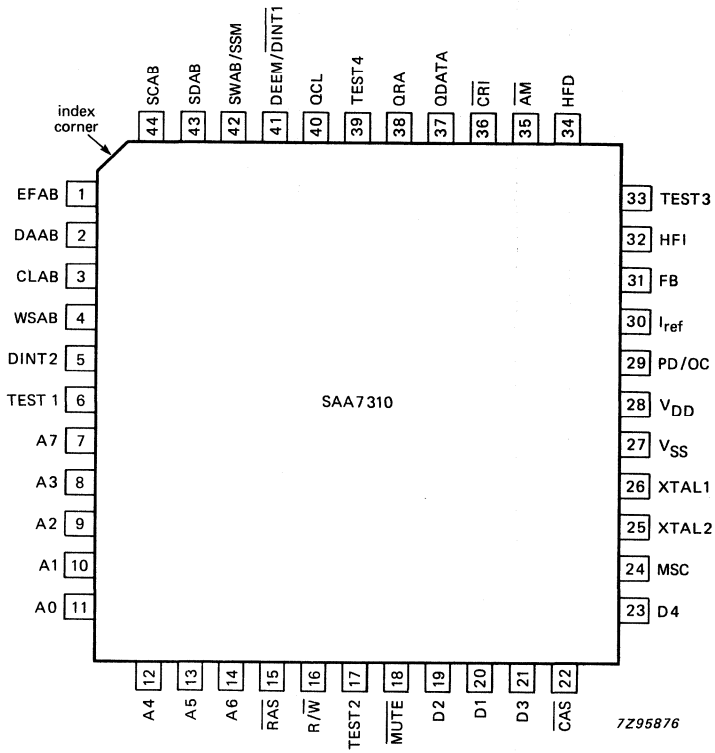


Fig. 4 Pinning diagram; for 44-lead QFP package.

DEVELOPMENT DATA

Pin functions

pin no. DIL	pin no. QFP	mneumonic	description
1 - 8	7 - 14	A0 - A7	**Address:** address outputs to external RAM.
9	15	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	16	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	18	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB, pin 37 (2), is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first 'good' value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12 - 14	19 - 21	D1 - D3	**Data:** data inputs/outputs to external RAM.
15	22	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	23	D4	**Data:** data input/output to external RAM.
17	24	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (42) (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continuous 50% duty factor.
18	25	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	26	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	27	V_{SS}	**Ground:** circuit earth potential.
21	28	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).
22	29	PD/OC	**Phase Detector output/ Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	30	I_{ref}	**Current reference:** external reference input to the phase detector and data slicer. This input is required to minimize the spread in the charge pump output of the phase detector and data slicer.
24	31	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input HFI at pin 25 (32) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD at pin 26 (34) is LOW, this output goes to a high impedance state.

Pin functions (continued)

pin no. DIL	pin no. QFP	mneumonic	description
25	32	HFI	**High-Frequency Input:** level detector input to the data slicer. A differential signal of between 0,5 and 2,5 V (peak-to-peak value) is required to drive the data slicer correctly. When a T_{max} violation is detected or when HFD is LOW, this input is biassed directly to its threshold voltage
26	34	HFD	**High-Frequency Detector:** when HIGH this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer. An internal voltage clamp of 3 V (typ.) requires the HFD input to be fed via a high impedance. This input has an internal pull-up of 50 kΩ (typ.).
27	35	$\overline{AM}$	**Additional Mute:** This pin is normally held HIGH. Should track loss occur the pin should be taken LOW and then the data is forced LOW at the pre-FIFO stage. The muted data will then be corrected after de-interleaving. **Note** With DINT2, DEEM/$\overline{DINT1}$, FB set to logic 0 and SDAB, SCAB set to logic 1, this pin becomes the demodulator clock output (CEFM) of the SAA7210 (CD2A).
28	36	$\overline{CRI}$	**Counter Reset Inhibit:** when LOW this input signal allows the divide-by-588 master counter in the DEMOD timing to run-free. This input has an internal pull-up of 50 kΩ (typ.).
29	37	QDATA	**Q-channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol).
30	38	QRA	**Q-channel Request input/Acknowledge output:** the output has an internal pull-up of nominally 10 kΩ. (see subcoding microprocessor handshaking protocol).
31	40	QCL	**Q-channel Clock:** clock input generated by the microprocessor when it detects a QRA LOW signal.
32	41	DEEM/$\overline{DINT1}$	**De-emphasis output and data interpolated input:** signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit in DEEM mode. When using the CD3A in a non-digital audio application this pin should be set HIGH (with DINT2 set LOW) to prevent data being interpolated. **Note** This pin should **only** be used in its input mode when DINT2 is LOW.
33	42	SWAB/SSM	**Subcoding Word clock output and Start/Stop Motor input:** open drain output which is sensed during each HIGH period and if externally forced LOW a motor-stop condition will be decoded and fed to the motor control logic circuit. When allowed to return HIGH, the motor will start. This open-drain output has an internal pull-up of 10 kΩ (typ.).

Pin functions

pin no. DIL	pin no. QFP	mneumonic	description
34	43	SDAB	**Subcoding Data:** a 10-bit burst of data, including flags and sync bits, is output serially once per frame clocked by burst clock output SCAB (see Fig. 6).
35	44	SCAB	**Subcoding Clock:** a 10-bit burst clock 2,8224 MHz (typ.) output which is used to synchronize the subcoding data.
36	1	EFAB	**Error Flag:** output from interpolation and mute circuit indicating unreliable data.
37	2	DAAB	**Data:** this output together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Fig. 7).
38	3	CLAB	**Clock:** I^2S output.
39	4	WSAB	**Word Select:** I^2S output.
40	5	DINT2	**Data interpolated input:** this pin should normally be set HIGH. When using the CD3A in a non-digital audio application this pin should be set LOW (with DEEM/$\overline{\text{DINT1}}$ set HIGH) to prevent data being interpolated.

The following pins apply to the 44-pin QFP package only:

–	6	TEST1	**Test output 1**
–	17	TEST2	**Test output 2**
–	33	TEST3	**Test output 3**
–	39	TEST4	**Test output 4**

DEVELOPMENT DATA

Note to the pin functions

The pin sequence of the address outputs (A0 - A7) and the data outputs (D1 - D4) has been selected to be compatible with various dynamic 16 K x 4-bit RAMs including the 4416.

FUNCTIONAL DESCRIPTION

All references to pin numbers show the 40-lead DIL pin first followed by the 40-lead QFP pin in parenthesis.

Demodulation

Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at the input data rate (typically at 4,3218 MHz), its frequency being dependent on the voltage at pin 22 (29) (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output provides the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (29), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source I_{ref} connected to pin 23 (30).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input at pin 28 (36) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.

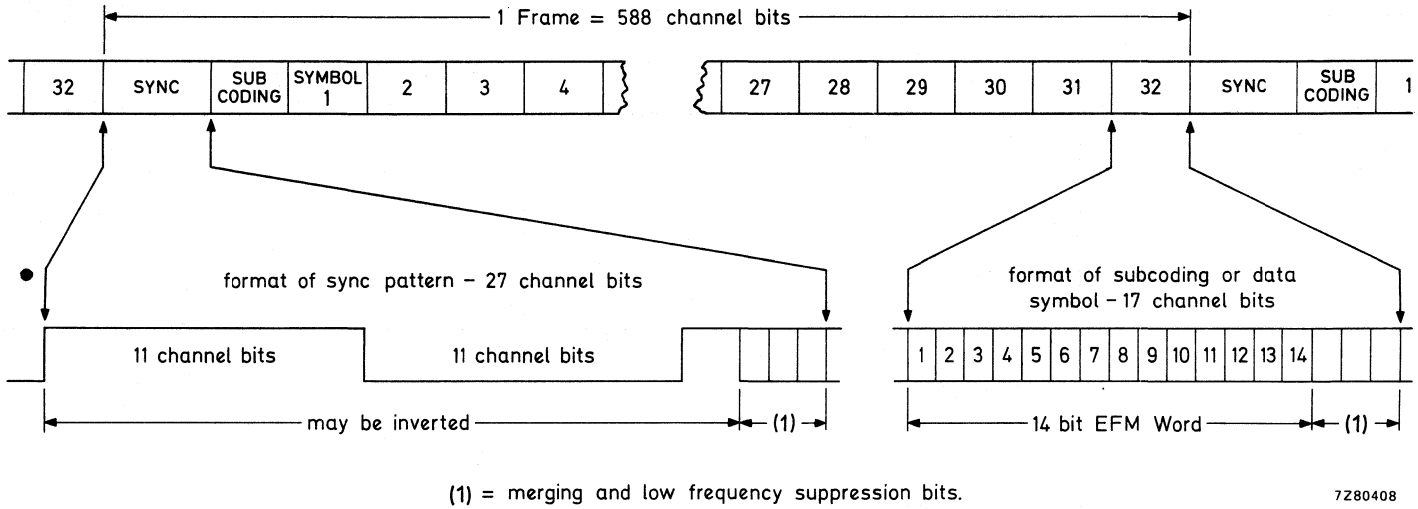


Fig. 5 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output pin 32 (41) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34 (43). The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally in the rising edge of SWAB at pin 33 (42); see Fig. 6.

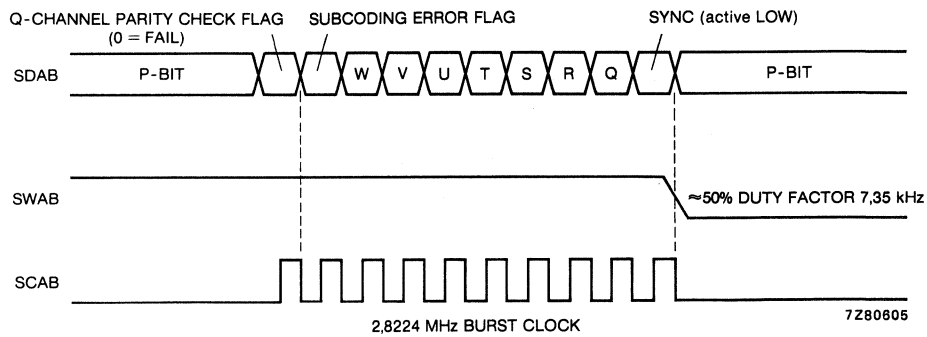


Fig. 6 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4-symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency.

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 8) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address $\overline{RAS}$ pin 9 (15) is set up first and then three 4-bit nibbles are accessed using sequential column addresses $\overline{CAS}$ pin 15 (22). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good' data (flags = 00) and three levels of error can be indicated.
The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

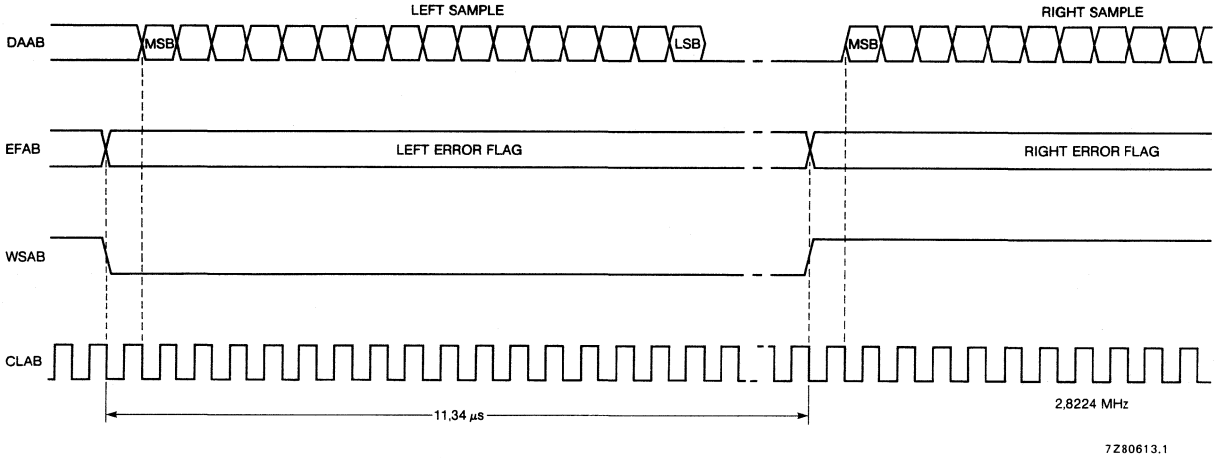


Fig. 7 Typical I²S waveform outputs to SAA7220 or SAA7320.

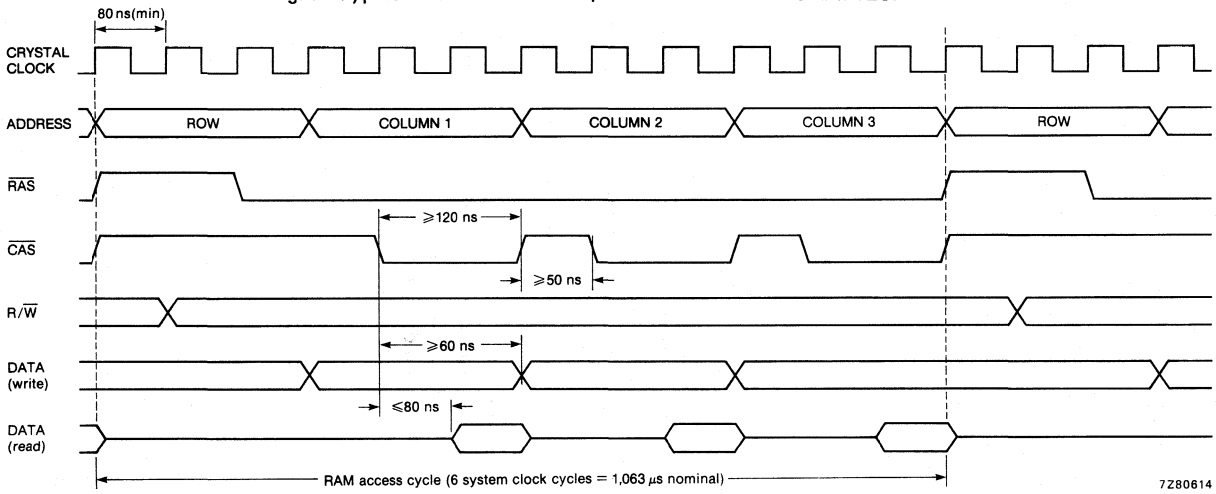


Fig. 8 RAM timing waveforms: timings based on RAM TMS4416; $\overline{G}$ input to RAM held LOW.

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

When using the CD3A in a non-digital audio application, pins DINT2 and DEEM/$\overline{\text{DINT1}}$ should be set to logic 0 and logic 1 respectively. The URD flag will then be disabled to prevent data being interpolated.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the SAA7220 where it receives additional and more efficient concealment (see Fig. 9).

FUNCTIONAL DESCRIPTION (continued)

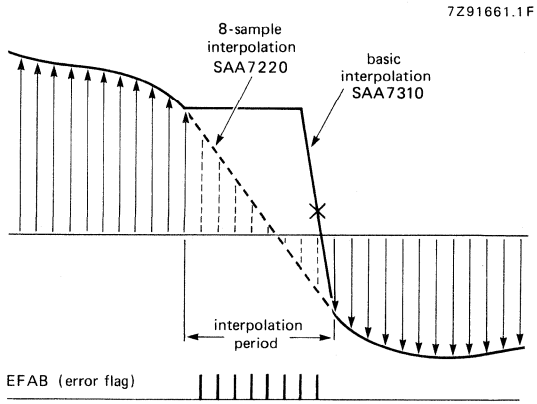


Fig. 9 The SAA7220 can make an 8-sample linear interpolation, the SAA7310 a hold and single-sample interpolation. When interpolating more than 8 samples, a hold function operates in the SAA7220 before the interpolation.

Non-digital audio applications

The CD3A contains a special mode for non-digital applications such as CD-ROM and CD-I. In this mode the concealment section is not allowed to operate. The flagged output words of the error correction circuit are passed to the output DAAB without being affected by the interpolation circuit. The EFAB output signal indicates unreliable output words on a sample basis when one or both bytes in a sample are unreliable. This is necessary as the CD-ROM/CD-I player performs its own error correction strategy on the data. The level of data integrity has to be much higher to ensure no errors occur in text or numerical information.

Specifications of CD-ROM and CD-I modes are available on request.

Motor speed control (see Fig. 10)

The motor speed control (MSC) output from pin 17 (24) is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

Track loss correction

The CD3A also incorporates a function to provide extra correction during track loss. Should track loss occur, the additional mute pin ($\overline{AM}$) should be taken LOW, which forces the data LOW at the pre-FIFO stage. This muted data is then corrected after de-interleaving. This function is particularly useful for applications where mechanical shock is likely to occur.

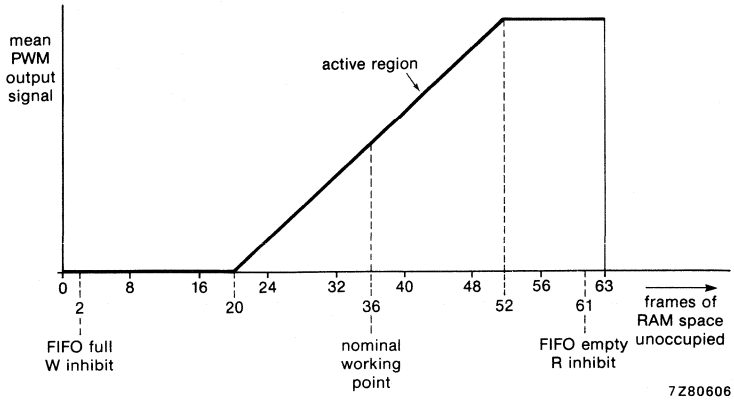


Fig. 10 Motor speed control.

DEVELOPMENT DATA

CD2A replacement

The CD3A can become a direct replacement for the CD2A by externally connecting pin 21 to V_{DD} and modifying the PLL peripheral components (see Fig. 12).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage, pin 21 (28)	V_{DD}	−0,5	+ 6,5	V
Maximum input voltage	V_I	−0,5	V_{DD} + 0,5	V
Input current, pin 23 (30)	I_I	−	5	mA
Maximum output voltage MSC, QRA, SWAB/SSM	V_O	−0,5	+ 6,5	V
Output current (each output)	I_O	−	± 10	mA
DC V_{SS} or V_{DD} current	I_{DD} or I_{SS}	−	± 100	mA
DC input diode current	I_{IK}	−	± 20	mA
DC output diode current	I_{OK}	−	± 20	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*	V_{es}	−1000	+ 1000	V

INTER·IC I²S SOUND

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

Detailed information on the I²S bus specification is available on request.

Supply of this Compact Disc IC does not convey an implied licence under any patent right to use this IC in any Compact Disc application.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage, pin 21 (28)		V_{DD}	4,5	5,0	5,5	V
Supply current, pin 21 (28)		I_{DD}	–	35	50	mA
Inputs						
D1 – D4, QCL, $\overline{AM}$, DEEM/$\overline{DINT1}$, DINT2						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
$\overline{MUTE}$, $\overline{CRI}$						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance	V_I = 0 V	$\|Z_I\|$	18	50	110	kΩ
Input capacitance		C_I	–	–	10	pF
QRA, SWAB/SSM						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance		C_I	–	–	10	pF
Internal pull-up impedance	V_I = 0 V	$\|Z_I\|$	3,9	10	18	kΩ
HFD						
Input voltage LOW		V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH		V_{IH}	2,0	–	clamped	V
Input clamping voltage	I_I = 100 μA	V_{CL}	2,0	3,0	4,5	V
Input source current		I_S	−100	–	100	μA
Input capacitance		C_I	–	–	10	pF
Internall pull-up impedance	V_I = 0 V	$\|Z_I\|$	18	50	110	kΩ

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs						
A0–A7, R/$\overline{W}$, D1–D4, $\overline{CAS}$, $\overline{RAS}$, QDATA, DEEM/$\overline{DINT1}$, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB, TEST1, TEST2, TEST3, TEST4						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD}	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
MSC (open drain)						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	0	–	0,35	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
SWAB/SSM, QRA (open drain)						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance		C_L	–	–	50	pF
Internal load resistance		R_L	3,9	10	18	kΩ
ANALOGUE CIRCUITS						
Data slicer (see Fig. 11)						
Input HFI						
AC input voltage range (peak-to-peak value)		$V_{I(p-p)}$	0,5	–	2,5	V
Input impedance						
normal (HFD HIGH)		$\|Z_I\|$	500	–	–	kΩ
disabled (HFD LOW)		$\|Z_I\|$	50	100	200	kΩ
Input capacitance		C_I	–	–	10	pF
Output FB						
Output current	V_{FB} = 2 V	I_O	$I_{ref}/5$ −20%	$I_{ref}/5$	$I_{ref}/5$ +20%	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase detector						
Output PD/OC	see Fig. 12					
Output current	PD/OC = 1 to 3 V	I_O	$\pm I_{ref}-20\%$	$\pm I_{ref}$	$\pm I_{ref}+20\%$	μA
Control range	note 3	α	±2,1	–	–	rad
Input I_{ref}	see Fig. 13					
Input reference current		I_{ref}	–	500	*	μA
Fine frequency detector						
Output PD/OC						
Output impedance		$\|Z_O\|$	2	4,1	5,6	kΩ
Output voltage LOW	$I_{OL} = 1\ \mu A$	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH} = 1\ \mu A$	V_{OL}	4	–	V_{DD}	V
Coarse frequency detector						
Output PD/OC	note 4					
Output impedance		$\|Z_O\|$	1	2,3	3,2	kΩ
Output voltage LOW	$I_{OL} = 1\ \mu A$	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH} = 1\ \mu A$	V_{OL}	4	–	V_{DD}	V
Voltage controlled oscillator						
Input PD/OC						
Oscillator constant		K_{osc}	–	3,5	–	MHz/V
Crystal oscillator	see Fig. 14					
Input XTAL1						
Output XTAL2						
Mutual conductance	100 kHz	G_m	1,5	–	–	ms
Small signal voltage gain	$G_V = G_m \times R_o$	G_V	3,5	–	–	V/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
Output capacitance		C_O	–	–	10	pF
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Slave clock mode	see Fig. 15					
Input voltage (peak-to-peak value)		$V_{I(p-p)}$	3,0	–	$V_{DD}+0,5$	V
Input voltage LOW	note 1	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	note 1	V_{IH}	2,4	–	$V_{DD}+0,5$	V
Input rise time	note 5	t_r	–	–	20	ns
Input fall time	note 5	t_f	–	–	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	–	55	%
TIMING						
Operating frequency (XTAL)		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)	PLL locked on to data	f_{VCO1}	2,54	4,3218	6,21	MHz
Operating frequency (VCO)	VCO absolute limits; PLL not locked on to data	f_{VCO2}	2	–	7,5	MHz
Outputs	Figs. 16 and 17					
CEFM	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
Output HIGH time		t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (I^2S format)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB						
Data set-up time		$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB						
Data hold time		$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (subcoding outputs)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
SDAB to SCAB						
Subcoding data set-up time		$t_{SU;SDAT}$	100	–	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
SCAB to SDAB						
Subcoding data hold time		$t_{HD;SDAT}$	100	–	–	ns
SWAB/SSM	note 6					
Output rise time		t_r	–	–	1	ns
Output fall time		t_f	–	–	100	ns
Output duty factor			–	50	–	%
Q-channel I/O	Figs 18 and 19					
QRA, QCL, QDATA						
Access time	note 7					
normal mode		$t_{ACC;N}$	0	–	13,3 + n x 13,3	ms
refresh mode		$t_{ACC;F}$	13,3	–	n x 13,3	ms
QCL to QRA						
acknowledge delay		t_{DACK}	–	–	500	ns
request hold time		$t_{HD;R}$	750	–	–	ns
QCL clock input LOW time		$t_{CK;LOW}$	750	–	–	ns
QCL clock input HIGH time		$t_{CK;HIGH}$	750	–	–	ns
QCL to QDATA delay time		t_{DD}	–	–	750	ns
Data hold time before new frame is accessed		$t_{HD;ACC}$	2,3	–	–	ms
Acknowledge time		t_{ACK}	–	–	10,8	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{LI(min)}$ and $I_{LO(min)}$ measured at $V_I = 0$ V; $I_{LI(max)}$ and $I_{LO(max)}$ measured at $V_I = V_{DD}$.
3. 1 rad = $\frac{180^o}{(3,14)}$.
4. Coarse frequency detector output PD/OC active for VCO frequencies
   $> \frac{f_{XTAL}}{2}$ and $< \frac{f_{XTAL}}{4}$.
5. Reference levels = 0,5 V and 2,5 V.
6. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
7. Q-channel access times dependent on cyclic redundancy check (CRC);
   n = number of cycles until CRC is 'good'.

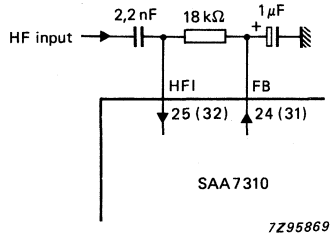


Fig. 11 Data slicer HFI input.

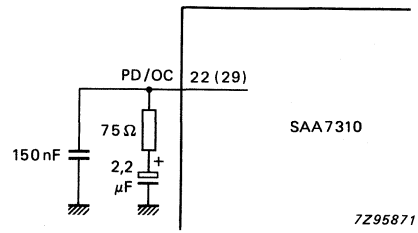


Fig. 12 PLL circuit.

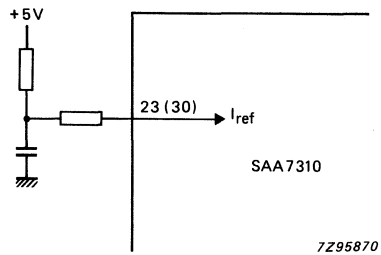


Fig. 13 I_{ref} circuit.

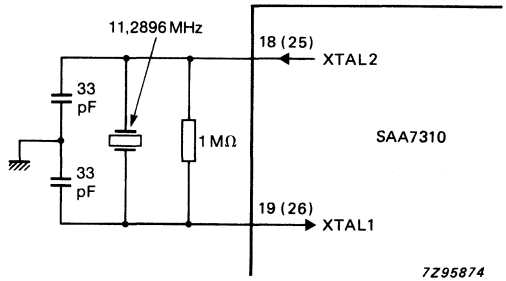


Fig. 14 Crystal oscillator circuit; using crystal type: 4322 143 05031.

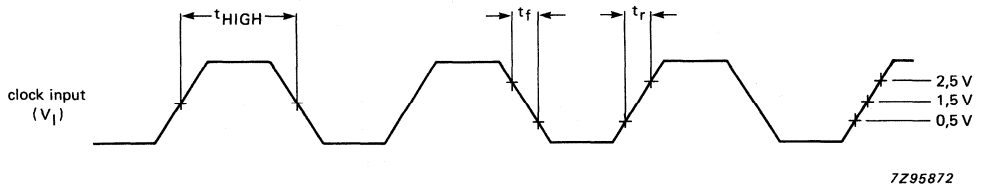


Fig. 15 Input clock timing diagram; reference levels 0,5 V, 1,5 V and 2,5 V.

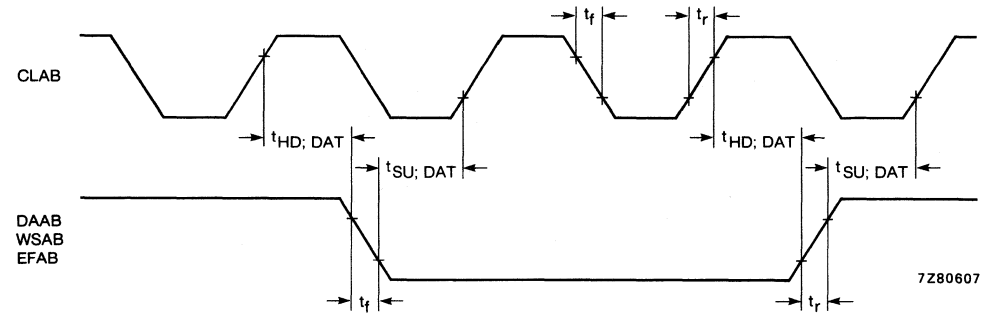


Fig. 16 Typical I^2S data output waveforms; reference levels = 0,8 V and 2,0 V.

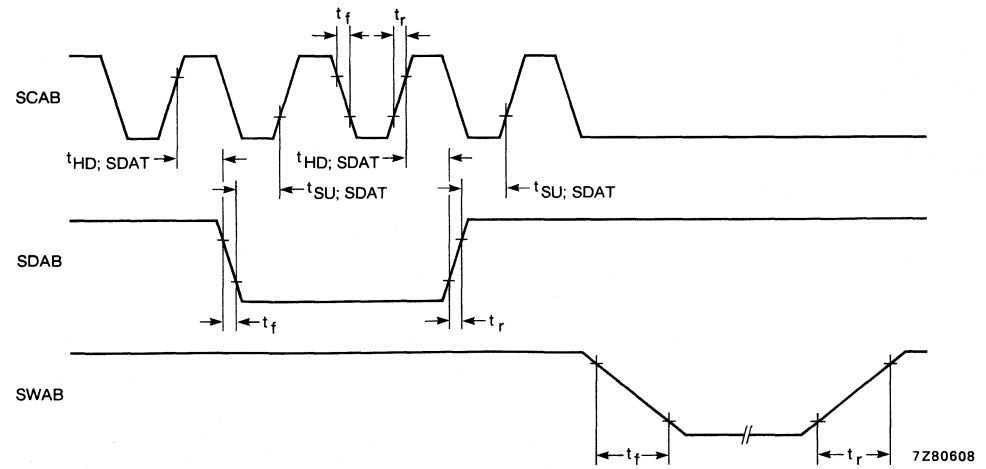


Fig. 17 Typical subcoding data output waveforms; reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

DEVELOPMENT DATA

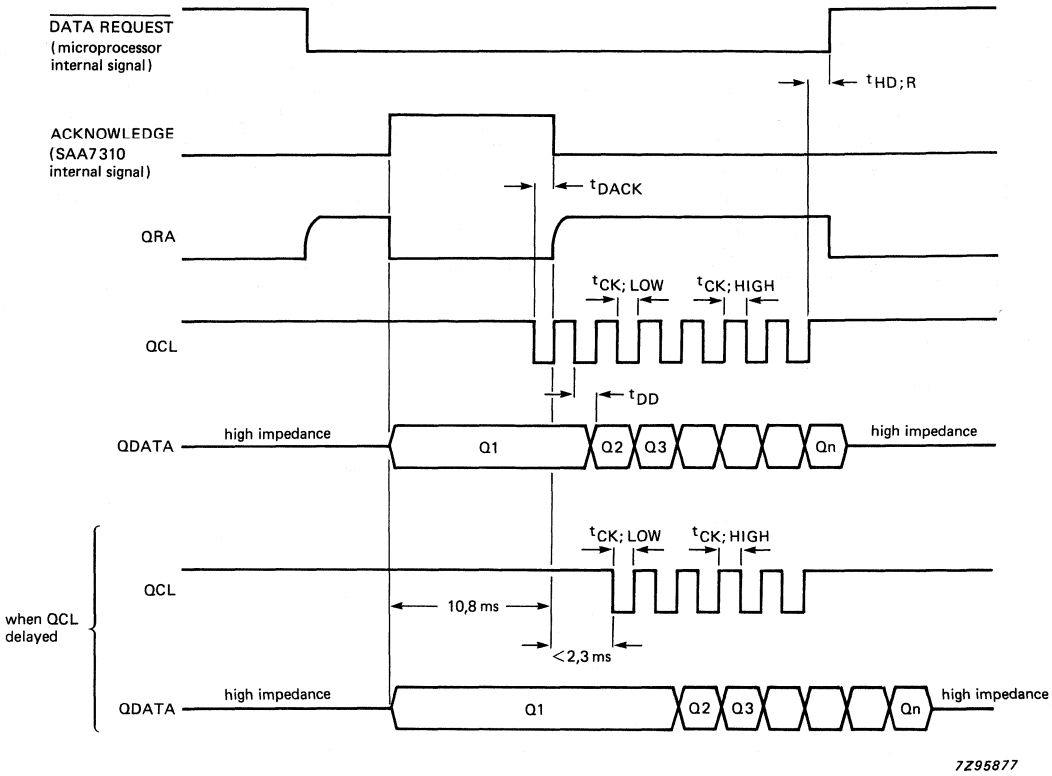


Fig. 18 Q-channel timing waveforms (normal mode).

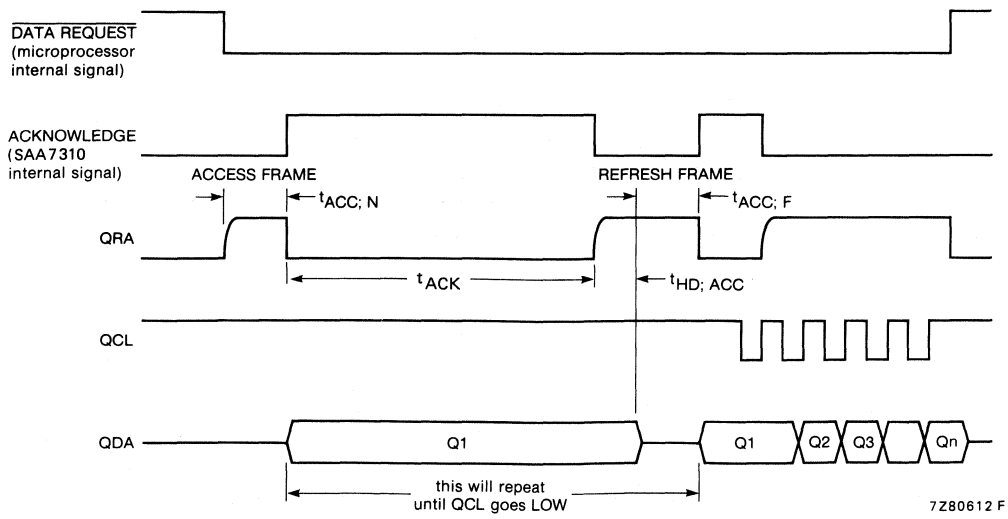


Fig. 19 Q-channel timing waveforms (refresh mode).

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a DC free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the DC content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 20).

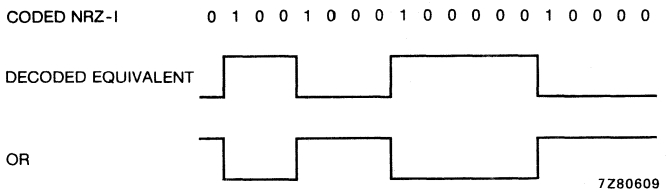


Fig. 20 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

APPLICATION INFORMATION (continued)

Table 2 EFM code conversion

No.	DNZ data symbol D1 D8	equivalent code word C1 C14	No.	DNZ data symbol D1 D8	equivalent code word C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11 to 119			139 to 247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

Subcoding microprocessor handshaking protocol (see Figs. 18, 19 and 21)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7310.

The SAA7310 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7310 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7310 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowlegde signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7310 now disabled the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7310 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7310 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

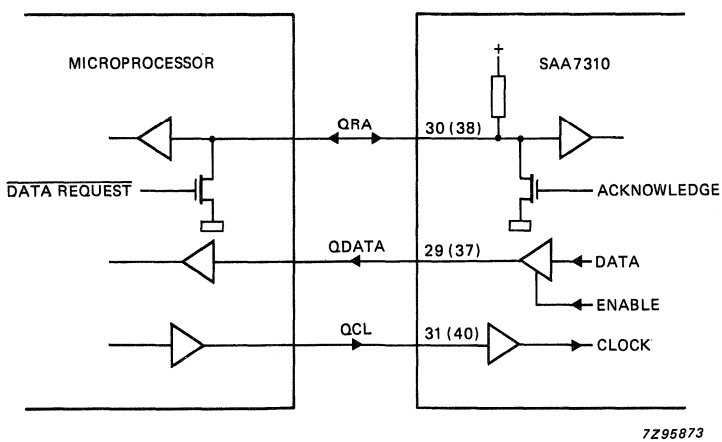


Fig. 21 Microprocessor handshaking protocol.

DIGITAL SATELLITE RADIO BROADCASTING TUNER DECODER (SAT-2)

GENERAL DESCRIPTION

The SAA7500 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.**

Features

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in case of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in case of synchronization loss

QUICK REFERENCE DATA

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	4.5	5.5	V
Power dissipation	P_{tot}		500	mW
Clock frequency	T_{20N}	20.48		MHz

PACKAGE OUTLINE

68-lead plastic leaded chip carrier (PLCC); 'pocket' version (SOT188AA).

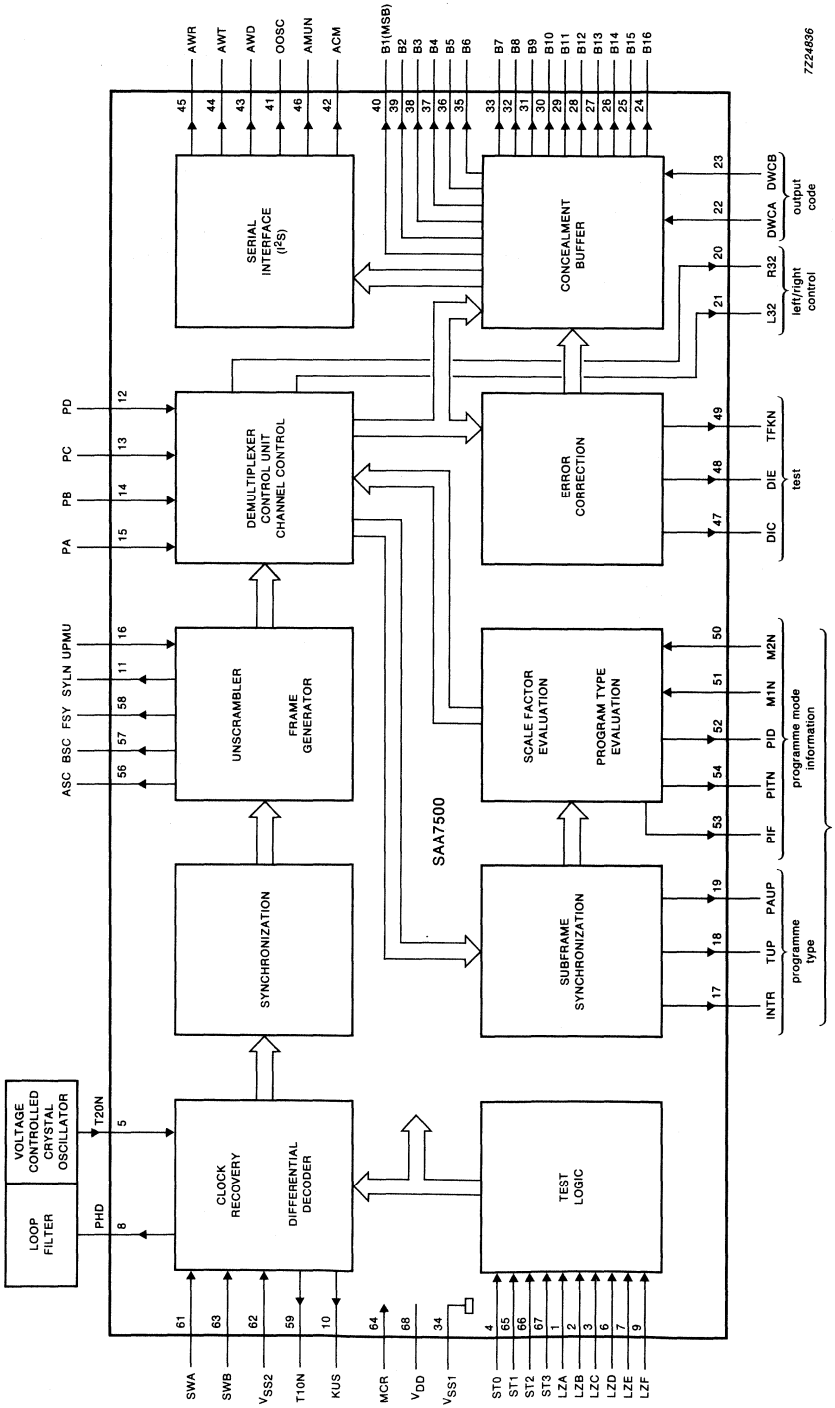


Fig.1 Block diagram.

PINNING

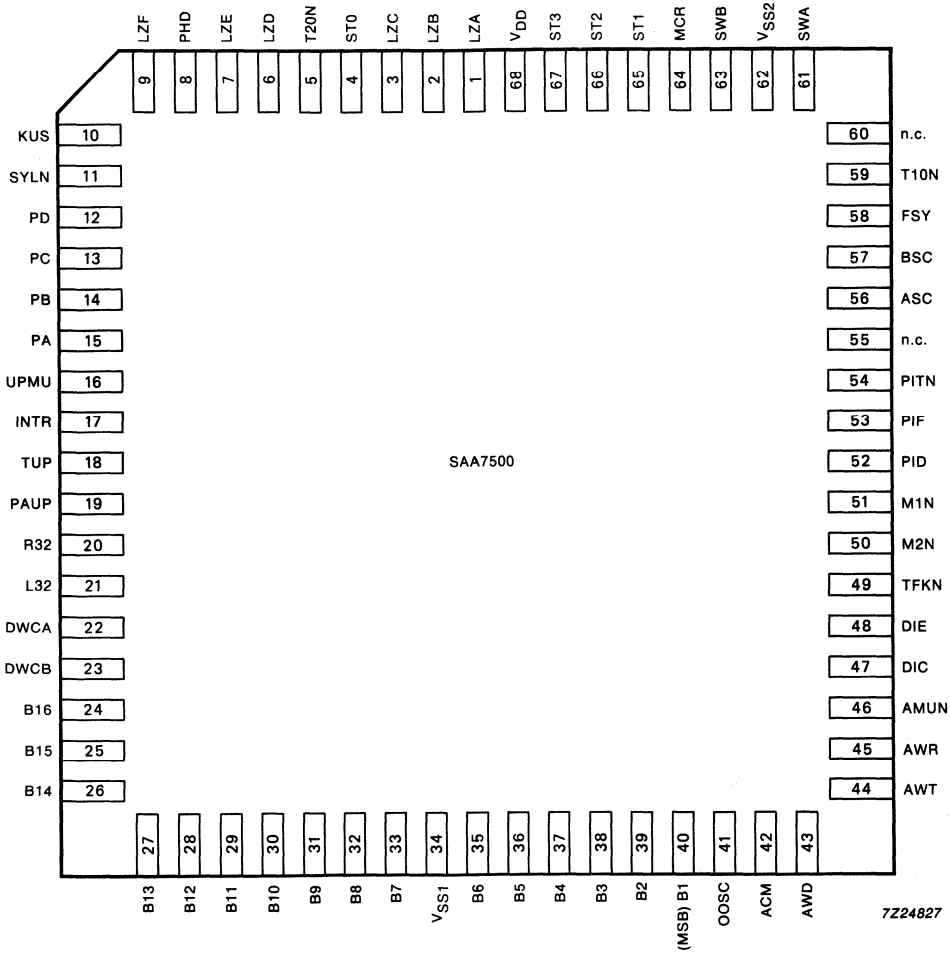


Fig.2 Pinning diagram; for pin functions see next page.

Pin functions

(1) = CMOS level input. (2) = TTL level input. (3) = CMOS level input with pull down resistor.

pin no.	mnemonic		description
1	LZA	I(3)	phase adjustment for the internal clock.
2	LZB	I(3)	phase adjustment for the internal clock.
3	LZC	I(3)	phase adjustment for the internal clock.
4	ST0	I(3)	control input for testing.
5	T20N	I(1)	20.48 MHz clock input from voltage controlled oscillator (VCX).
6	LZD	I(3)	control input for testing.
7	LZE	I(3)	control input for testing.
8	PHD	O	phase control signal for VCX.
9	LZF	I(3)	control input for testing.
10	KUS	O	test output (A'B' swap).
11	SYLN	O	synchronization indication flag.
12	PD	I(2)	programme number input selector (MSB)
13	PC	I(2)	programme number input selector.
14	PB	I(2)	programme number input selector.
15	PA	I(2)	programme number input selector (LSB).
16	UPMU	I(2)	mute input (controlled by microcomputer).
17	INTR	O	interrupt flag for microcomputer.
18	TUP	O	programme type interface (clock).
19	PAUP	O	programme type interface (data).
20	R32	O	multiplex control signal for right channel.
21	L32	O	multiplex control signal for left channel.
22	DWCA	I(3)	DA-converter mode select input.
23	DWCB	I(3)	DA-converter mode select input.
24-33	B16-7	O	audio data for parallel interface, bits 16 (LSB) to 7.
34	V_{SS1}	I	ground (supply).
35-40	B6-1	O	audio data for parallel interface, bits 6 to 1 (MSB).
41	OOSC	O	4.096 MHz clock output.
42	ACM	O	concealment flag (for SAA7220P/C).
43	AWD	O	audio data (for SAA7220P/C).
44	AWT	O	bit clock (for SAA7220P/C).
45	AWR	O	word select signal (for SAA7220P/C).
46	AMUN	O	mute signal (for SAA7220P/C).
47	DIC	O	data output for testing.
48	DIE	O	data output for testing.

pin no.	mnemonic		description
49	TFKN	O	burst clock for test data.
50	M2N	I(2)	channel mode select input.
51	M1N	I(2)	channel mode select input.
52	PID	O	programme information (PI) interface output (data).
53	PIF	O	programme information (PI) interface output (window signal).
54	PITN	O	programme information (PI) interface output (clock).
55	n.c.		not connected.
56	ASC	O	data output for 10.24 Mbit/s interface.
57	BSC	O	data output for 10.24 Mbit/s interface.
58	FSY	O	window signal for 10.24 Mbit/s interface.
59	T10N	O	10.24 MHz clock output.
60	n.c.		not connected.
61	SWA	I(2)	10.24 Mbit/s data input.
62	V_{SS2}	I	ground (screen).
63	SWB	I(2)	10.24 Mbit/s data input.
64	MCR	I(1)	master reset.
65	ST1	I(3)	control input for testing.
66	ST2	I(3)	control input for testing.
67	ST3	I(3)	control input for testing and mode select for 10.24 Mbit/s interface.
68	V_{DD}	I	power supply.

FUNCTIONAL DESCRIPTION

General

The SAA7500 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.** The channel carrying the sound broadcast programme is selected and converted into an intermediate frequency by a frontend. The signal is then amplified and demodulated (4 PSK (Phase Shift Keying) with carrier recovery). The outputs from the demodulator are two differential coded signals that are input into the SAA7500. The SAA7500 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, as well as stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7500 transmits serial data to the microcomputer on the type of programme (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7500 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7500 also sends to the microcomputer, programme information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of about 6 dB is obtained. The residual error rate is nearly zero for transmit error rates $\leqslant 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7500. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker codewords. The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also a synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the case of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of

a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half frame A is taken out. The rest of both half frames are unscrambled and demultiplexed so that each half frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the programme selector (inputs PA, PB, PC and PD) the demultiplexer locks on to the selected programme block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the result controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, programme type evaluation and shift sunction

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (three times transmitted) are fed into a majority selection circuit working at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7500 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The programme type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the programme selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations needed to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

FUNCTIONAL DESCRIPTION (continued)

Digital-to-analogue conversion and interfaces

The SAA7500 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.
For DACs with a parallel interface in a multiplex mode the audio data are available at the B1(MSB)-B16 outputs. The multiplexing is controlled by the L32 and R32 outputs. Using the mode outputs DWCA and DWCB the code (offset binary or two's complement) and polarity can be selected.

Additional information, including the scale factor is available through the programme information (PI) interface (PID, PITN and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to 'clock recovery' section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

Truth tables

Table 1 Delay adjustment

pins 1 to 3

LZC	LZB	LZA	delay
0	0	0	$4 \times \tau$
0	0	1	$3 \times \tau$
0	1	0	$2 \times \tau$
0	1	1	$1 \times \tau$
1	0	0	$0 \times \tau$
1	0	1	$-1 \times \tau$
1	1	0	$-2 \times \tau$
1	1	1	$-3 \times \tau$

$\tau \approx 1.5$ x gate delay time (NAND)

Table 2 Master reset

pin 64

MCR	function
0	operation
1	master reset

Table 3 Mute

pin 16

UPMU	function
0	no
1	yes

Table 4 Programme number

pins 12 to 15

PD	PC	PB	PA	programme no.
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal

pin 8

PHD	phase
0	lead phase
1	lag phase

Table 6 Synchronization indication

pin 11

SYLN	synchronization
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface

pin 67

ST3	data ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Data converter mode select B1(MSB) to B16

pins 22 and 23

DWCB	DWCA	DA converter mode
0	0	compl. offset binary
0	1	offset binary
1	0	compl. 2's complement
1	1	2's complement

Table 9 Channel mode select

pins 50 and 51

M2N	M1N	channel mode
0	0	mono (1 + 2)
0	1	mono R(2)
1	0	mono L(1)
1	1	stereo

Table 10 Concealment

pin 42

ACM	function
0	no
1	yes

Table 11 Mute

pin 46

AMUN	mute
0	yes
1	no

Table 12 Interrupt

pin 47

INTR	interrupt
0	no
1	yes

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	7.0	V
Input voltage range*	V_I	−0.5	V_{DD} + 0.5	V
Input current	I_I	−	± 10	mA
Output current	I_O	−	± 10	mA
Supply current in V_{SS}	I_{SS}	−	28	mA
Supply current in V_{DD}	I_{DD}	−	28	mA
Total power dissipation	P_{tot}	−	500	mW
Operating ambient temperature range	T_{amb}	−25	+85	°C
Storage temperature range	T_{stg}	−55	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

* V_{DD} + 0.5 must not exceed 7.0 V.

DC CHARACTERISTICS

T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current	Fig.10	I_{DD}	–	12.5	–	mA
Quiescent supply current	note 1	I_{DDq}	–	–	50	μA
Inputs I(1)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(2)						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(3)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Pull down resistor		R_I	25	50	100	kΩ
Outputs O						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	–	–	0.5	V
Output voltage HIGH	I_{OH} = 1 mA	V_{OH}	4.0	–	–	V

Notes to DC characteristics

1. T_{amb} = 25 °C, all inputs at V_{SS} or V_{DD}, all outputs open.
2. At 25 °C max. 1 μA.

AC CHARACTERISTICS

T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
T20N clock pulse	Fig.3					
Pulse width HIGH		t_{WH}	15	20	–	ns
Pulse width LOW		t_{WL}	15	22	–	ns
T20N pulse period		t_{P20}	48	48.8	–	ns
Data input timing	Fig.4					
Set-up time for data SWA and SWB to T10N	note 1	t_{SWL}	–	50	–	ns
T10N pulse period T_{PSW}	note 2	t_{P10}	–	97.6	–	ns
Main frame timing	Fig.5					
Main frame sync pulse		t_{SYNC}	–	$11t_{P10}$	–	ns
Audio data timing	Fig.6					
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
Load pulse width HIGH		t_{LPH}	–	6.25	–	μs
Audio data hold		t_{ADH}	–	1	–	μs
I²S timing	Fig.7					
Frequency AWT signal		f_{AWT}	–	1.024	–	MHz
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
PI interface timing	Fig.8					
Frequency PITN signal		f_{PITN}	–	32	–	kHz
PITN pulse period		t_{PITN}	–	31.25	–	μs
PIF pulse width HIGH		t_{PIFH}	–	$22t_{PITN}$	–	μs
PIF pulse period		t_{ZI}	–	2	–	ms
Output timing Programme type interface	Fig.9					
INTR pulse period		t_{INTR}	–	250	–	μs
INTR pulse width HIGH		t_{PINH}	–	31.25	–	μs

Notes to AC characteristics

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period time t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

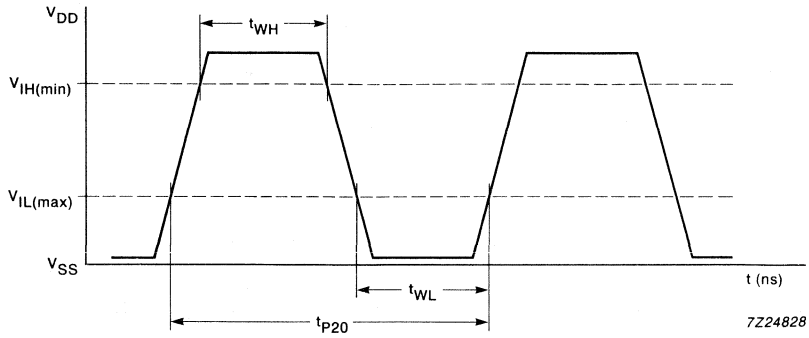


Fig.3 Waveform at clock input T20N (pin 5).

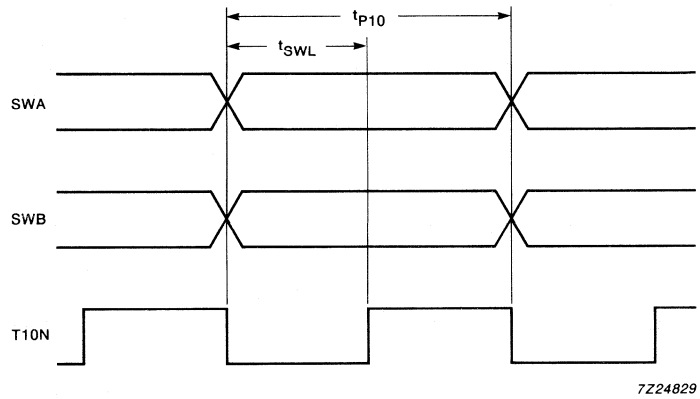


Fig.4 Data input timing (pins 59, 61 and 63).

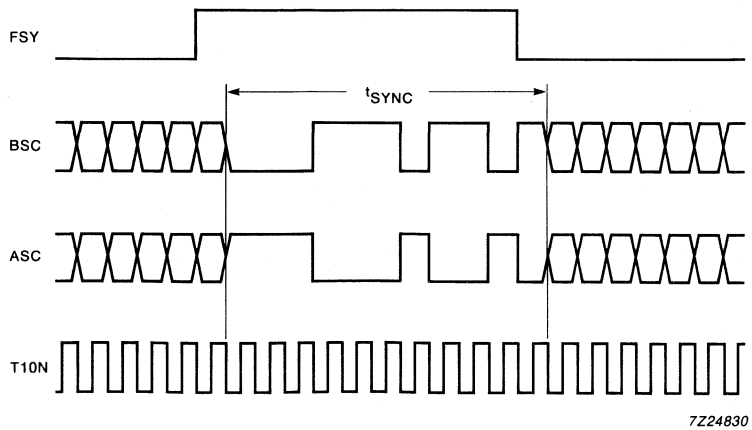


Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

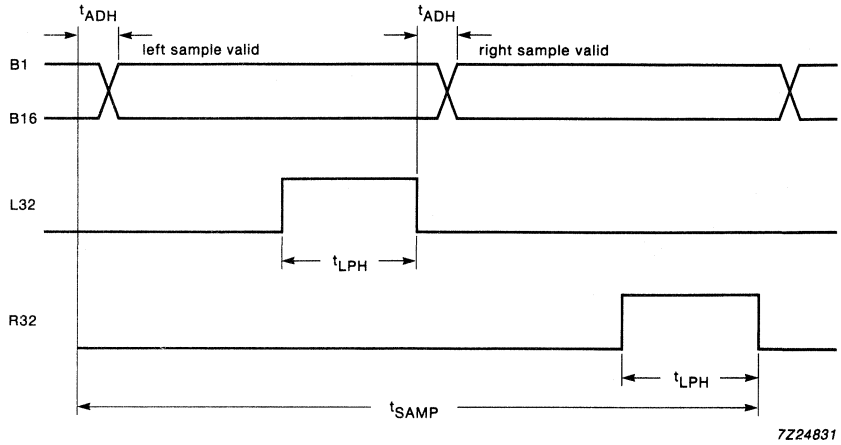


Fig.6 Audio data timing parallel out (pins 40 to 35, 33 to 24, 21 and 20).

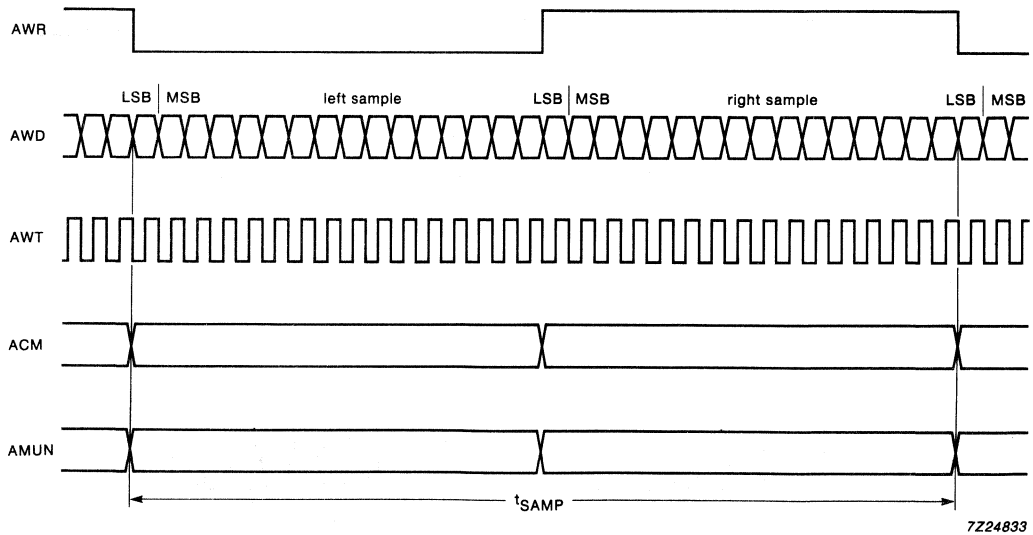


Fig.7 Inter-IC Sound (I^2S) timing and mute and interpolation flags (pins 42 to 46).

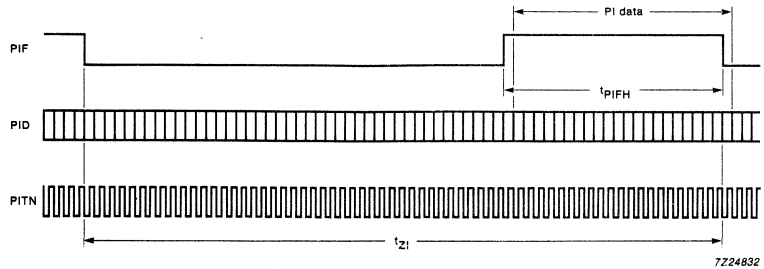
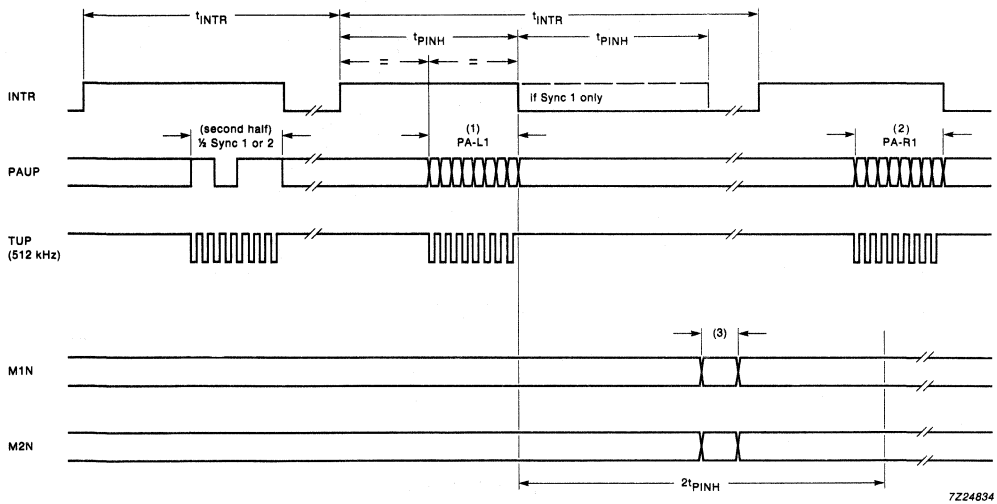


Fig.8 PI interface timing (pins 52 to 54).



(1) Programme type - left
(2) Programme type - right
(3) This time is approximately 10 μs

Fig.9 Output timing programme type interface (pins 17 to 19).

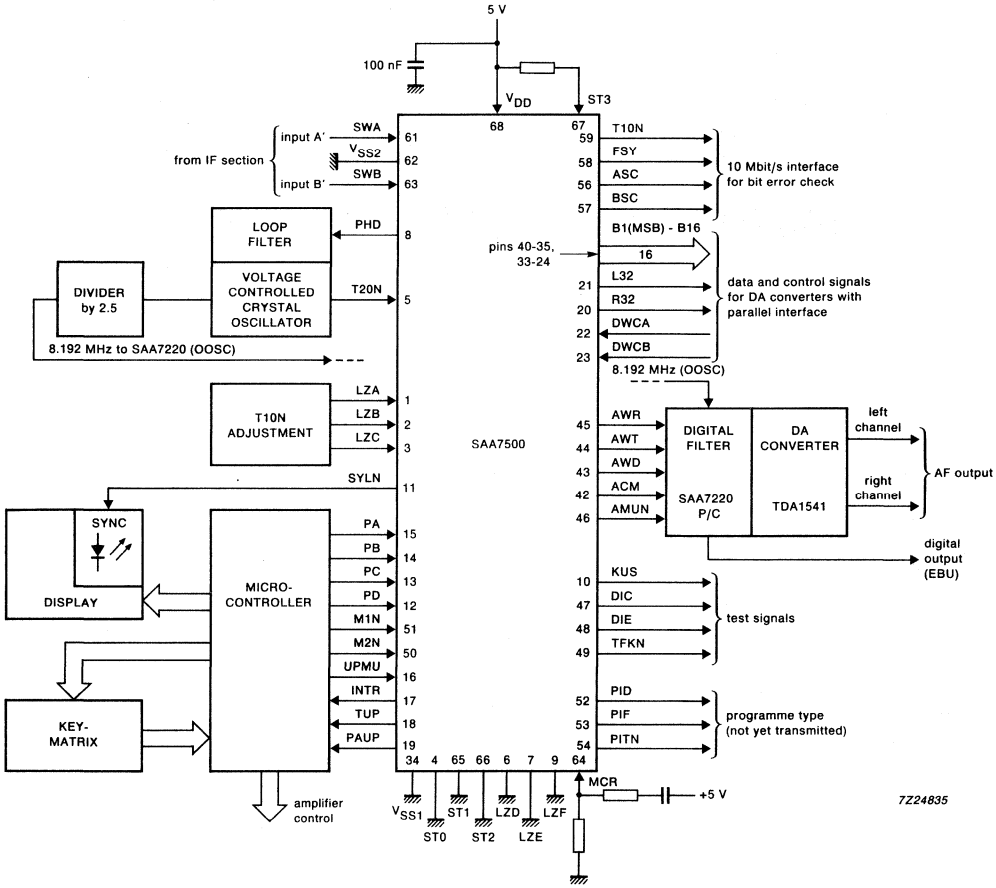


Fig.10 Application proposal.

RADIO DATA SYSTEM (RDS) DEMODULATOR

GENERAL DESCRIPTION

The CMOS IC, SAF7579, recovers the additional inaudible information from the Radio Data System (RDS) which is transmitted on FM sound channels.

The data signal, RDDA, and the clock signal, RDCL, are provided as outputs for further processing by a suitable microcomputer.

The operating functions within the device are in accordance with the EBU specification TECH 3244-E.

Features

- 57 kHz carrier regeneration (Costas loop)
- Synchronous demodulator for 57 kHz modulated RDS signals
- 4.332 MHz crystal oscillator with variable dividers
- Clock generation with lock on and biphase data rate
- Biphase symbol decoder with "Integrate and Dump" function
- Differential decoder
- Indicator output for ARI (Autofahrer Rundfunk Information) detection and RDS signal quality

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (at idle, oscillator on)	I_{DD}	–	1.5	–	mA
Oscillator frequency	f_{osc}	–	4.332	–	MHz
Operating ambient temperature range	T_{amb}	−40	–	+85	°C

PACKAGE OUTLINES

SAF7579T: 16-lead mini-pack; plastic (SO16L; SOT162A).
SAF7579U/F: chips uncased, on foil.
SAF7579U/T: chips on wafer.

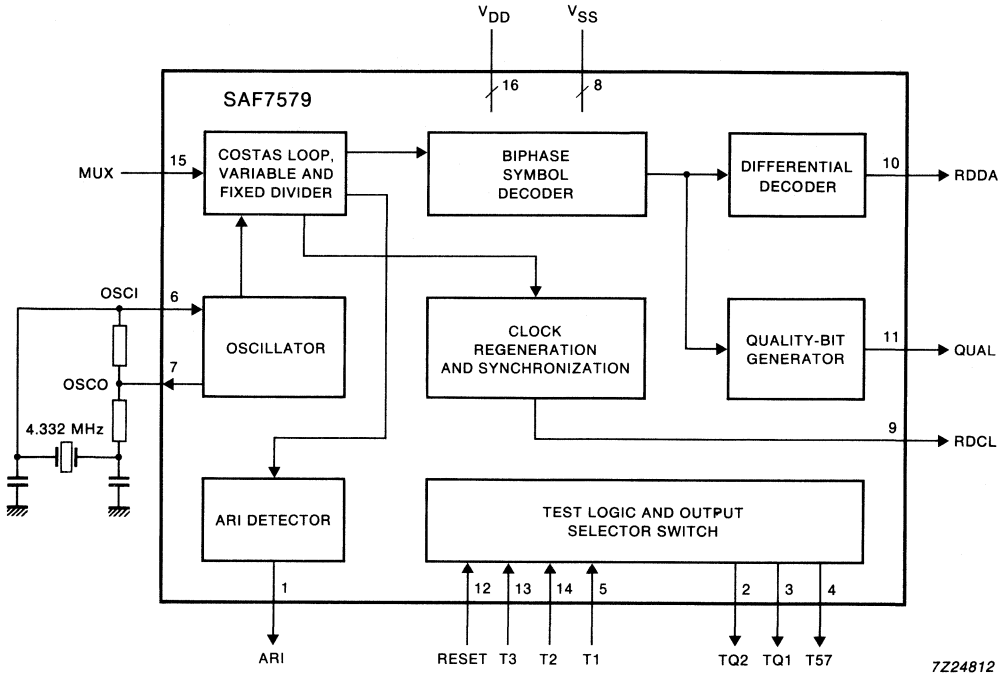


Fig.1 Block diagram.

PINNING

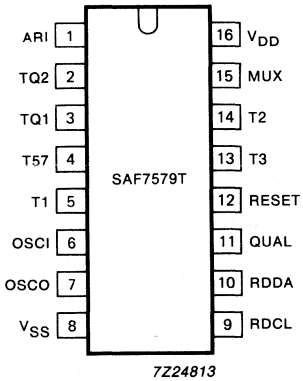


Fig.2 Pinning diagram.

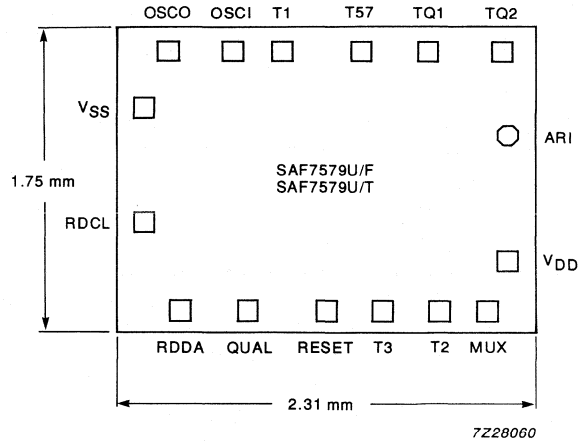


Fig.3 Bonding pad locations.

pin	mnemonic	description
1	ARI	Output for ARI indication (ARI = HIGH when ARI present)
2	TQ2	Test output 2
3	TQ1	Test output 1
4	T57	57 kHz output
5	T1	Test input 1
6	OSCI	Oscillator input
7	OSCO	Oscillator output
8	V_{SS}	Ground
9	RDCL	Output for RDS clock
10	RDDA	Output for RDS data
11	QUAL	Output for signal quality indication (HIGH = good)
12	RESET	Reset input for test logic
13	T3	Test input 3
14	T2	Test input 2
15	MUX	RDS input signal (band and amplitude limited)
16	V_{DD}	Supply voltage

FUNCTIONAL DESCRIPTION

The multiplex output signal from the FM demodulator is passed through a narrow band-pass filter to produce the 57 kHz RDS and ARI information. This signal is then limited and amplified to TTL levels. The resultant 57 kHz square wave is fed to the MUX input of the SAF7579.

The RDS information is demodulated by a synchronous demodulator with carrier regeneration and the suppressed carrier is recovered from the two received sidebands (Costas loop). This demodulated signal is then low-pass filtered in such a way that the overall pulse shape approaches a cosine. This occurs in conjunction with the following "Integrate and Dump" circuit.

The data-spectrum shaping has been split equally between the transmitter and receiver so that, ideally, the data filtering at the receiver should be the same as that of the transmitter. The overall data-channel spectrum shaping of the transmitter and receiver should then be 100% roll-off.

The "Integrate and Dump" circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in the form of biphase symbols being outputted from the "Integrate and Dump" circuit. The final stages of RDS data processing are biphase symbol decoding and differential decoding. After synchronization with the clock the RDS data appears at the RDDA output of the device.

The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of good or corrupt data at the QUAL output (HIGH = good data, LOW = corrupt data).

The existence of an ARI signal in the multiplex signal is indicated by a HIGH on the ARI output (pin 1).

A 4.332 MHz ($\pm 10^6$ absolute maximum)* crystal oscillator is used (with both, fixed and variable dividing) to run the SAF7579. This oscillator also produces the 1187.5 Hz RDS clock (RDCL), which is synchronized with the incoming data. Which ever clock edge is considered (positive or negative) the data will remain valid for 417 μs after the clock transition. The timing of a data change is 4 μs before a clock change. Which clock transition (positive or negative edge) the data change occurs in, depends on the lock conditions and is arbitrary (bit-slip).

During poor reception it is possible for phase faults to occur. In this situation the clock signal will continue uninterrupted and the data will be constant for 1.5 clock periods. In normal conditions phase faults do not occur on a cyclic basis. If however, phase faults do occur in this way, the minimum spacing between two possible phase faults will depend on the data being transmitted. The minimum spacing cannot be shorter than 16 clock periods.

The quality signal (QUAL) will only change at the time of a data change.

* Philips Components part no. 9922 520 00189.

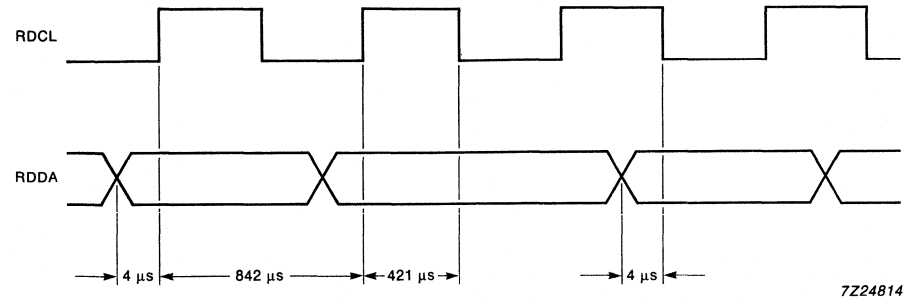


Fig. 4 Timing diagram for RDS signals with phase shift (bit-slip).

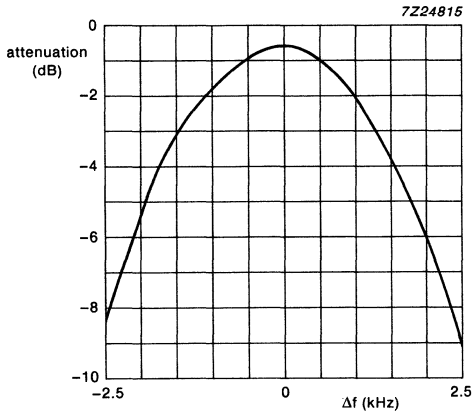
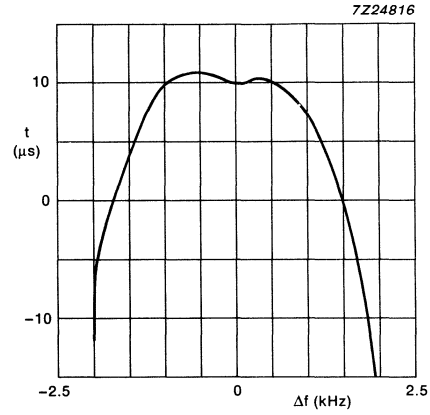


Fig. 5 Transmission curve.



0 ≙ +200 µs.

Fig. 6 Relative group delay.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

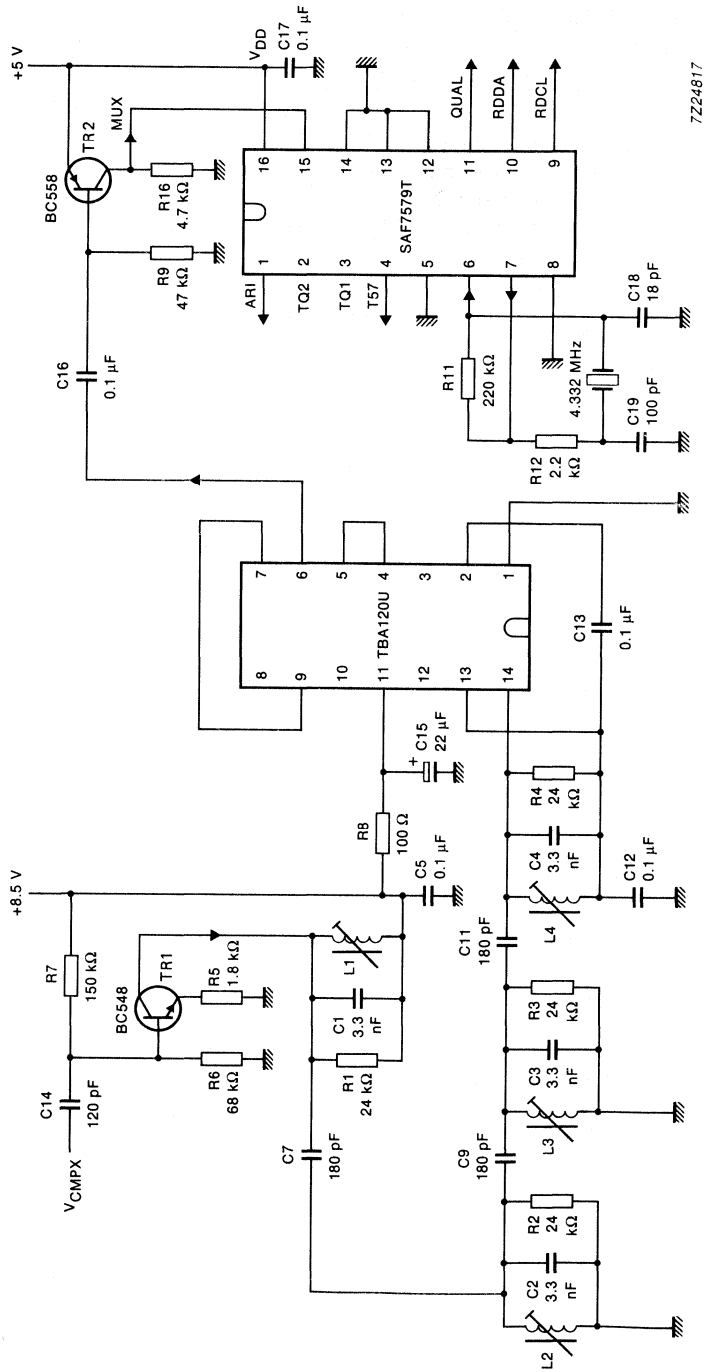
parameter	symbol	min.	typ.	max.	unit
Supply current	V_{DD}	−0.5	–	7	V
Supply current	I_{DD}, I_{SS}	–	–	60	mA
Input and output voltage	V_I, V_O	−0.5	–	V_{DD} + 0.5 (max. 7 V)	V
Input and output currents	$\pm I_I$, $\pm I_O$	–	–	10	mA
Total power dissipation*	P_{tot}	–	–	500	mW
Operating ambient temperature range	T_{amb}	−40	–	+85	°C
Storage temperature range	T_{stg}	−65	–	+150	°C

* Above +70 °C derate linearly with 8 mW/K.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4.5	5	5.5	V
Supply current	no load-current but oscillator on; T_{amb} = 25 °C; V_{DD} = 5 V	I_{DD}	–	1.5	–	mA
Quiescent supply current	all inputs at V_{DD} or V_{SS}, all outputs open	I_{DD}	–	–	50	μA
MUX RESET and OSCI inputs (inputs with hysteresis)						
Input voltage						
HIGH		V_{IH}	80% V_{DD}	–	V_{DD}	V
LOW		V_{IL}	0	–	20% V_{DD}	V
Hysteresis		V_{hyst}	–	0.5	–	V
Input leakage current		$\pm I_{LI}$	–	–	1	μA
Inputs T1, T2 and T3						
Input voltage						
HIGH		V_{IH}	70% V_{DD}	–	V_{DD}	V
LOW		V_{IL}	0	–	30% V_{DD}	V
Input leakage current		$\pm I_{LI}$	–	–	1	μA
Outputs RDDA, RDCL, QUAL, ARI, TQ1, TQ2 and T57						
Output voltage						
HIGH	$-I_O$ = 3.2 mA	V_{OH}	V_{DD}−0.4	–	–	V
LOW	I_O = 3.2 mA	V_{OL}	–	–	0.4	V
Output OSCO						
Output voltage						
HIGH	$-I_O$ = 1.6 mA	V_{OH}	V_{DD}−0.4	–	–	V
LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Data rate for RDS data		f_{RDCL}	–	1187.5	–	Hz
Carrier frequency		f_{T57}	–	57	–	kHz



TOKO coils: 126 ANS/A 3561 HM

Fig.6 Application diagram.

INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12 V
Supply current (pin 9)	I_P	typ.	14 mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1 V
Input resistance (pin 1)	R_i	min.	35 kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5 dB
Total harmonic distortion	THD	typ.	0,25 %
Bandwidth	B	typ.	70 kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19 mV
Suppression pulse duration	t_s	typ.	27 μs
Supply voltage range (pin 9)	V_P		7,5 to 16 V
Operating ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT38).
TDA1001BT: 16-lead mini-pack; plastic (SO16; SOT109A).

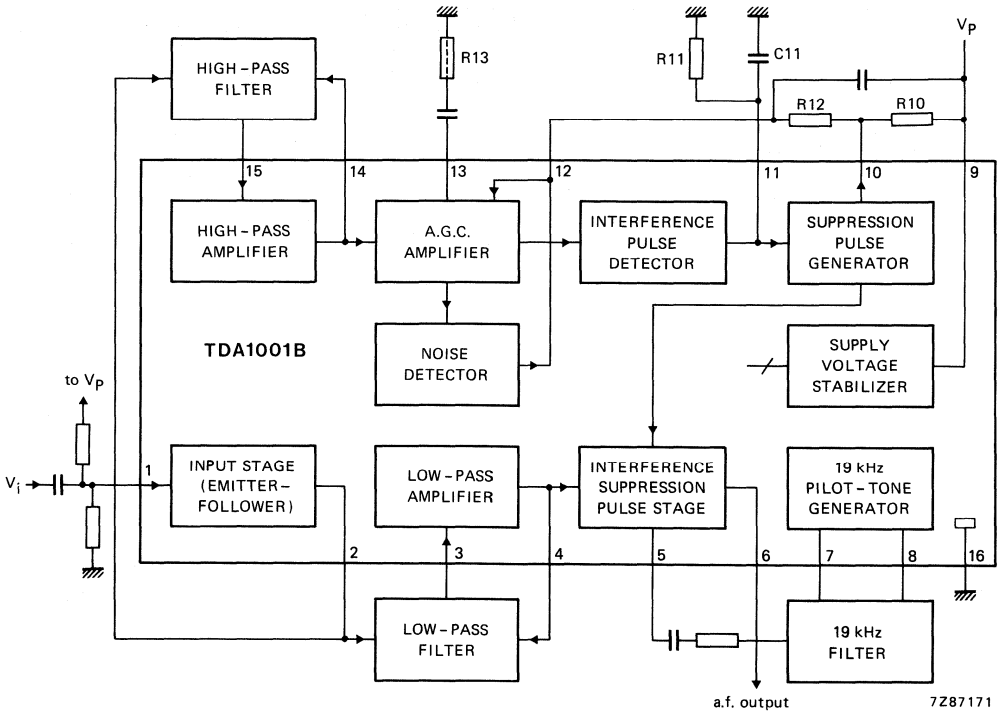


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18 V
Input voltage (pin 1)	V_{1-16}	max.	V_P V
Output current (pin 6)	I_6	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +80	°C

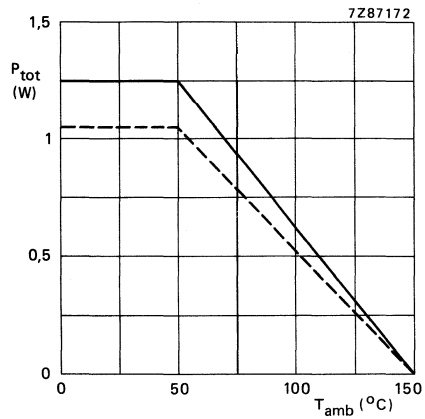


Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\|Z_{i1}\|$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$	–	6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\|Z_{i8}\|$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\|Z_{o7}\|$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\ m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\ m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
($V_{i(tr)O}$ + 3 dB)	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11) 1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\lvert Z_{i1}\rvert$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V					
at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value					
at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4)					
$V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a deemphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

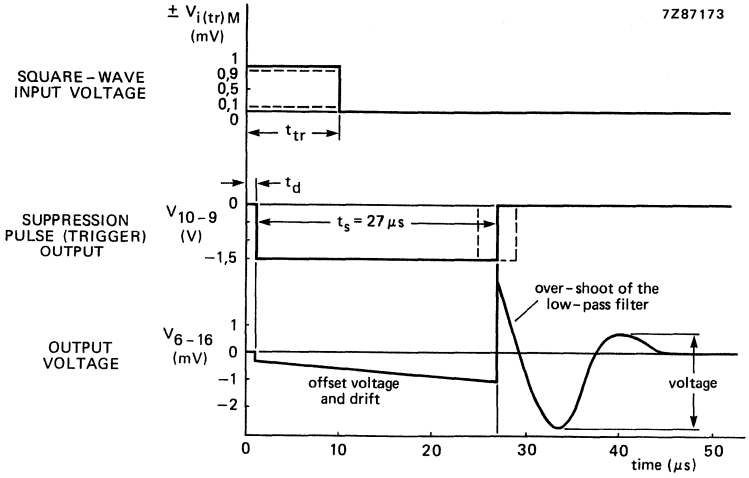


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

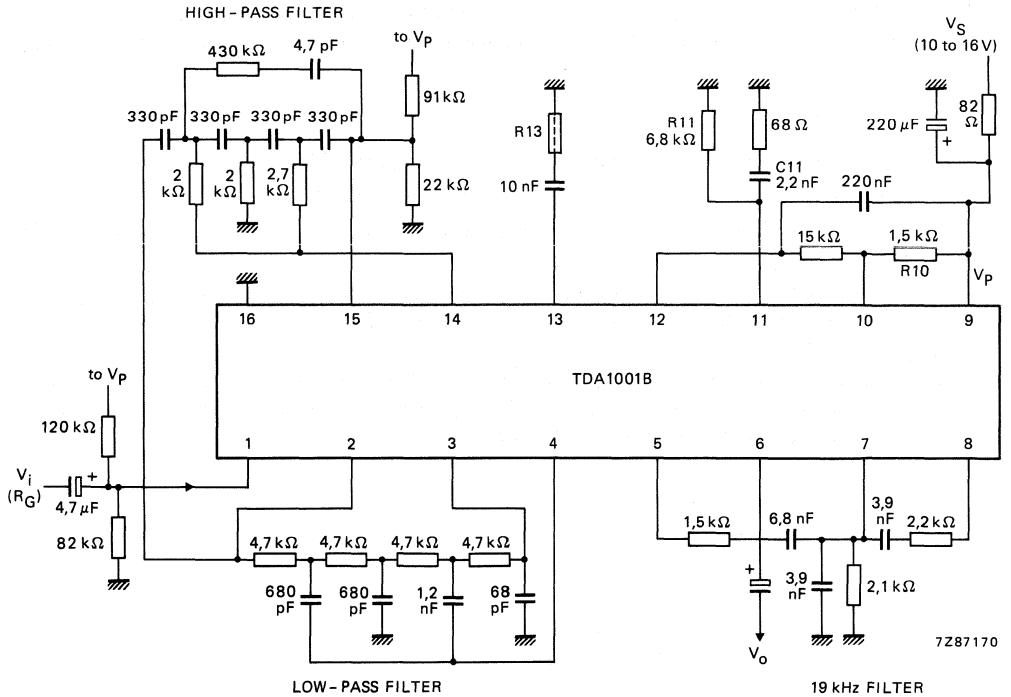


Fig. 4 Application circuit diagram.

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24 V
Repetitive peak output current	I_{ORM}	max.	3 A
Output power at pin 2; d_{tot} = 10%			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4 W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31 mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

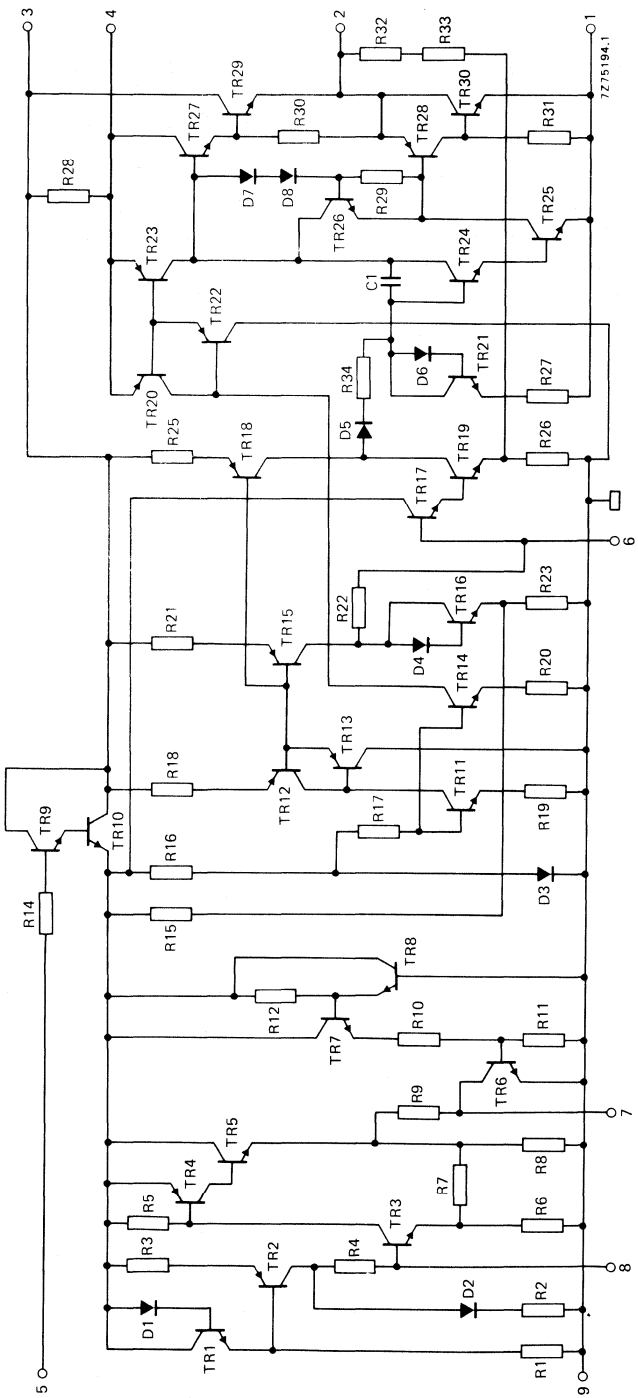


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	5 A
Repetitive peak output current	I_{ORM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100 hours

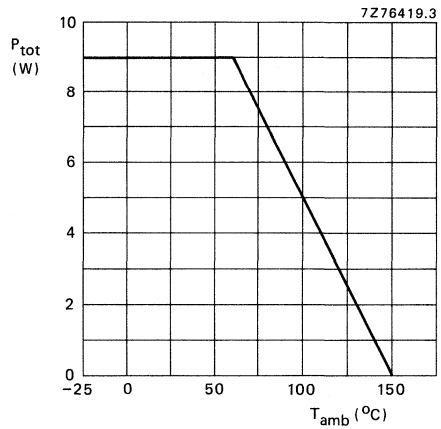


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$R_{th\ h\text{-}a}$ = 23 − (10 + 1) = 12 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	6 to 24	V
Repetitive peak output current	I_{ORM}	< 3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ. 31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap			
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ. 6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	> 5,9 typ. 6,2	W W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ. 3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ. 5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ. 9	W
Voltage gain			
preamplifier (note 3)	G_{v1}	typ. 24 21 to 27	dB dB
power amplifier	G_{v2}	typ. 30 27 to 33	dB dB
total amplifier	$G_{v\,tot}$	typ. 54 51 to 57	dB dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ. 0,2	%
Efficiency at P_o = 6 W	η	typ. 75	%
Frequency response (–3 dB)	B	80 Hz to 15	kHz
Input impedance			
preamplifier (note 4)	$\lvert Z_i \rvert$	typ. 30 20 to 40	kΩ kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ. 20 14 to 26	kΩ kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ. 20 14 to 26	kΩ kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 6)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ. 0,7 < 1,4	mV mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	> 42	dB
at f = 100 Hz; C2 = 1 μF	RR	> 37	dB
Sensitivity for P_o = 5,8 W	V_i	typ. 10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

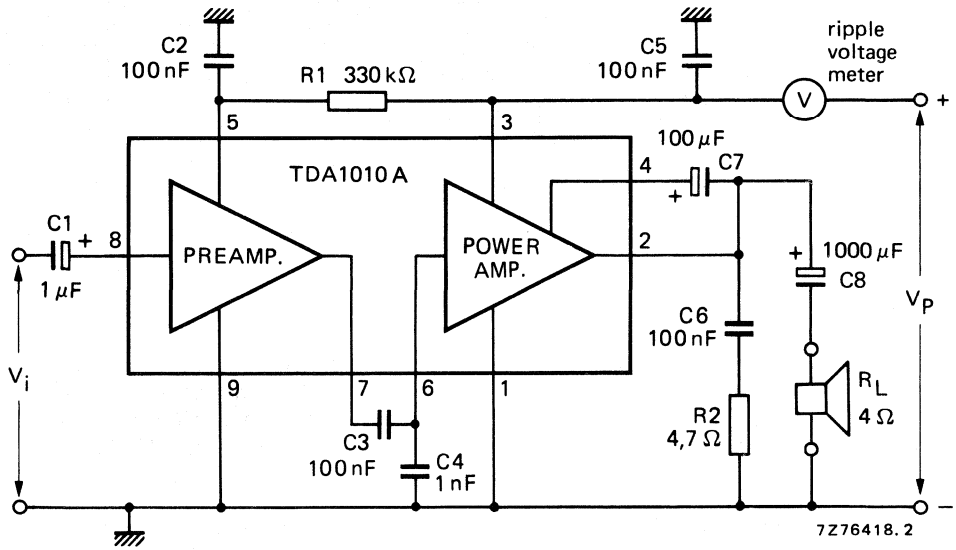


Fig. 3 Test circuit.

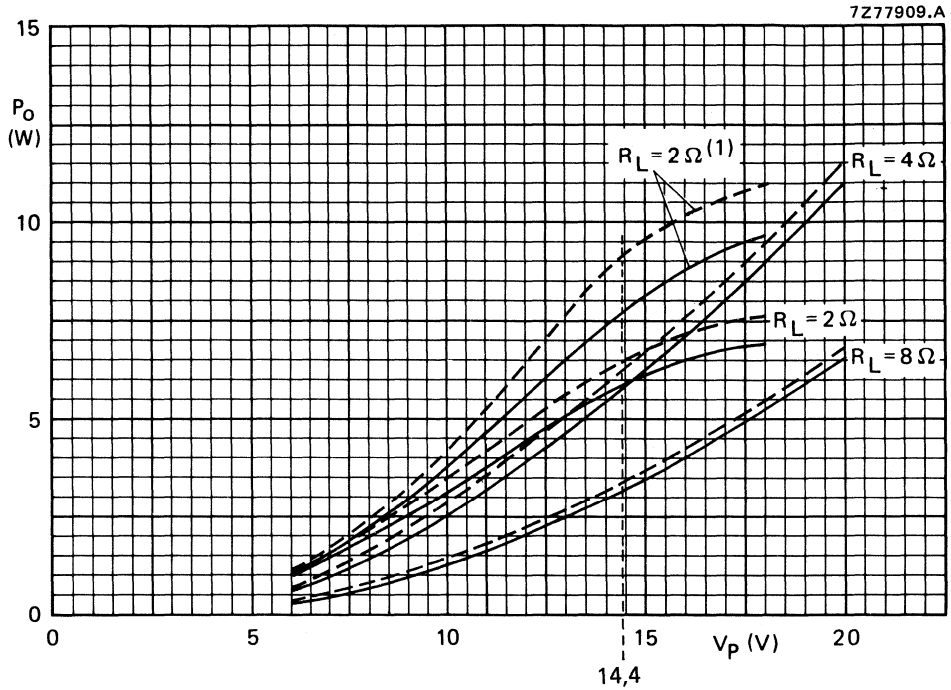


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

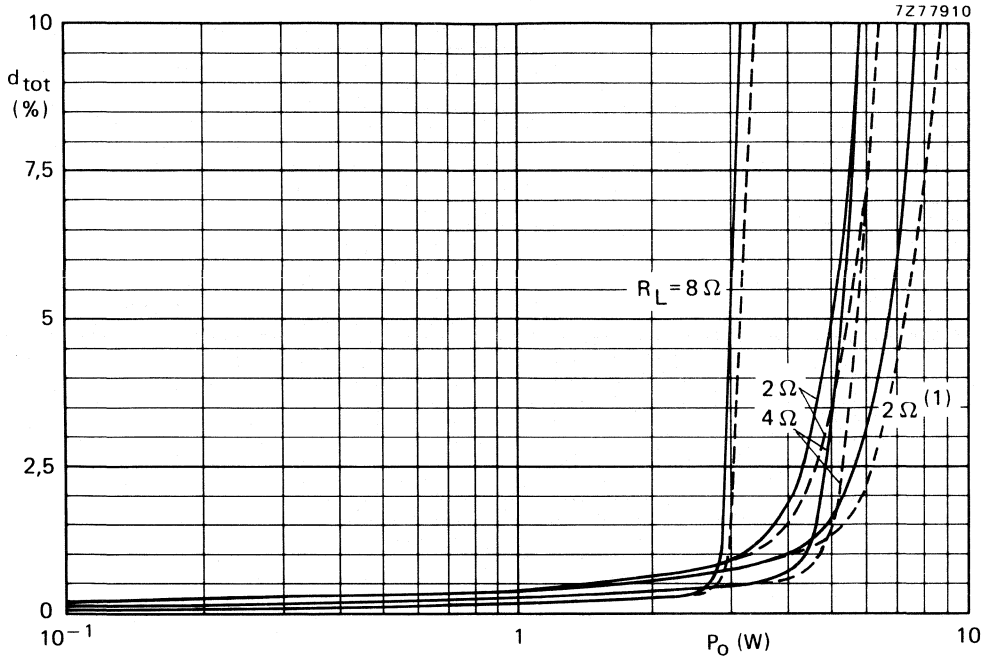


Fig. 5 For caption see preceding page.

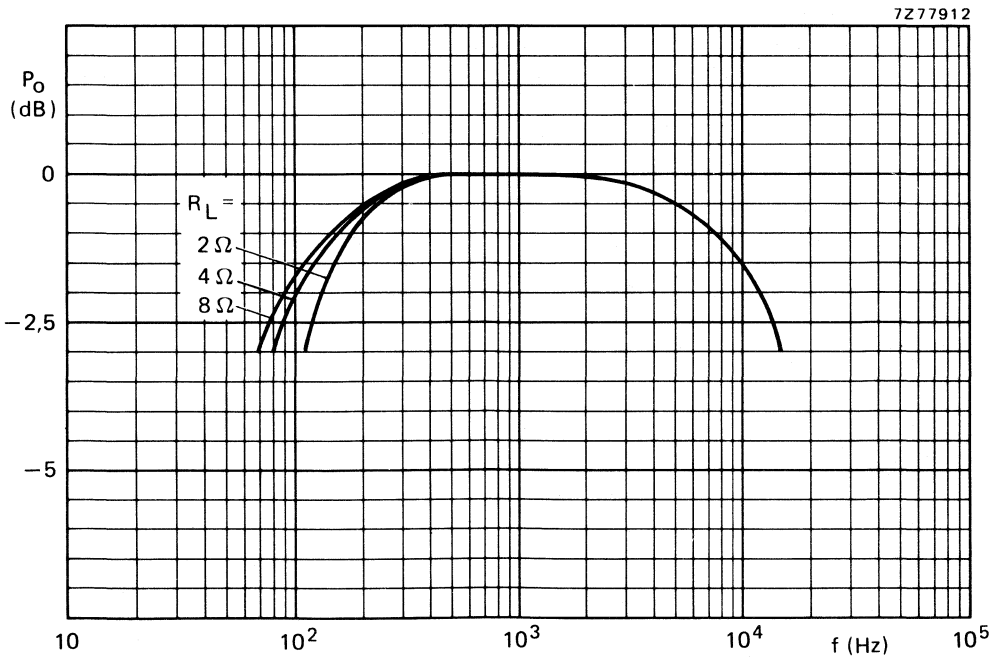


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_O relative to 0 dB = 1 W; V_P = 14,4 V.

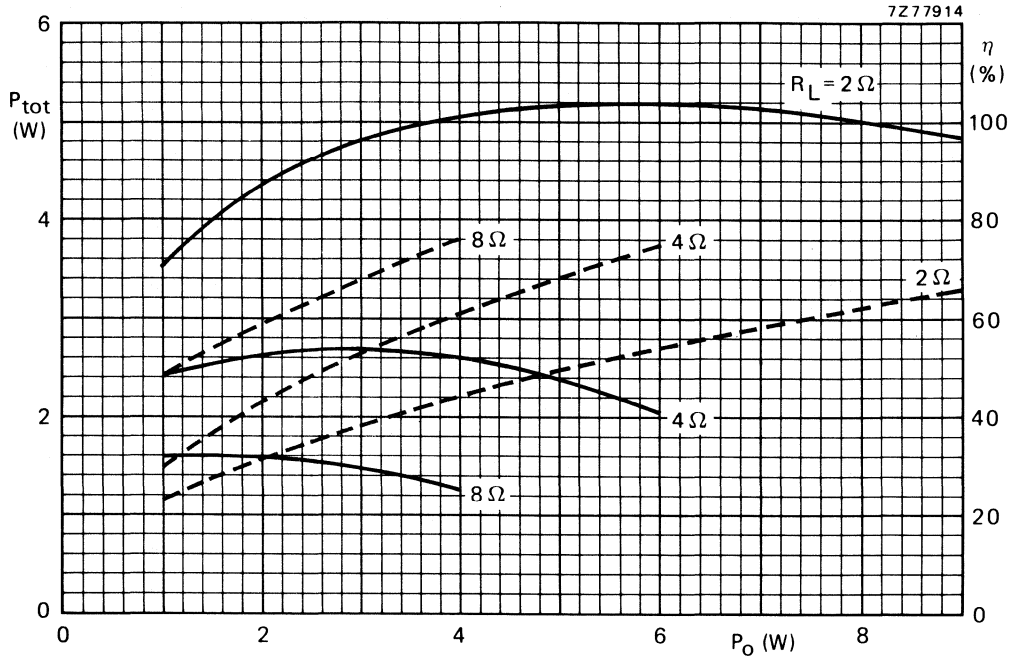


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\,\Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

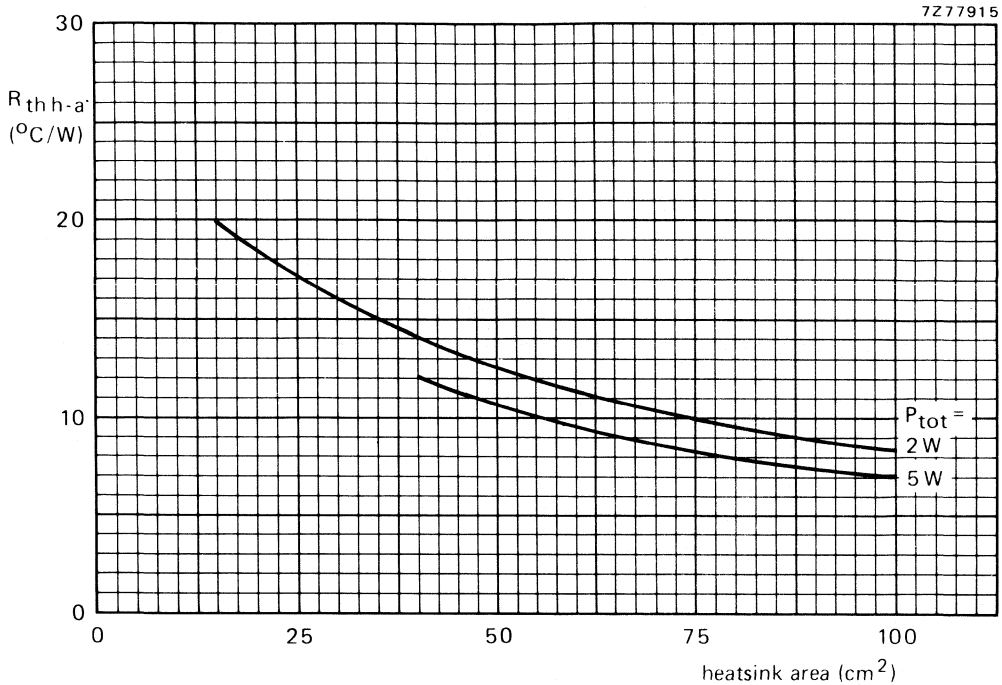


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

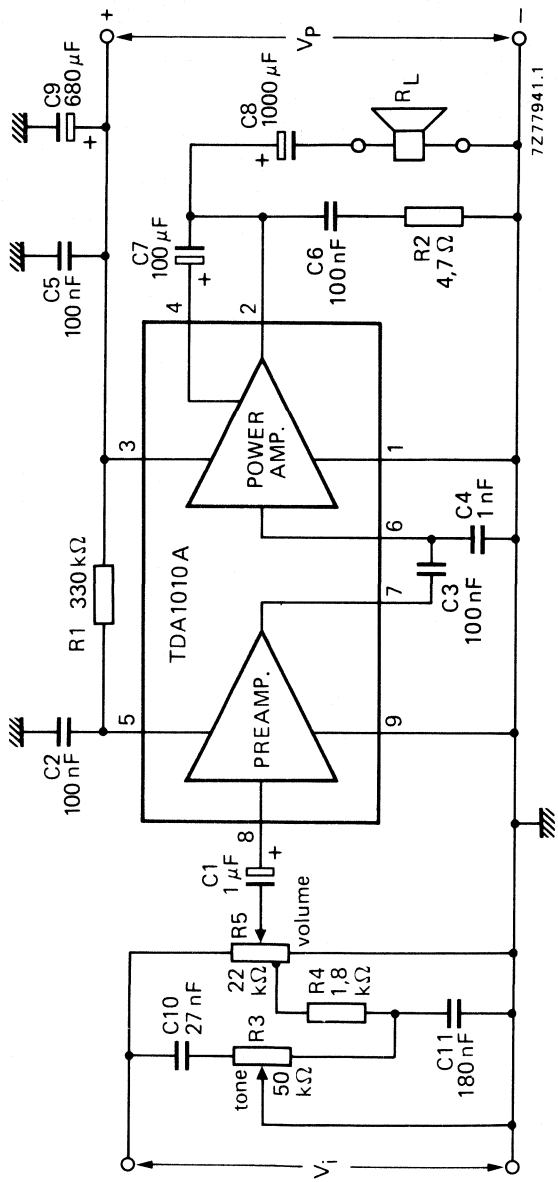


Fig. 9 Complete mono audio amplifier of a car radio.

APPLICATION INFORMATION

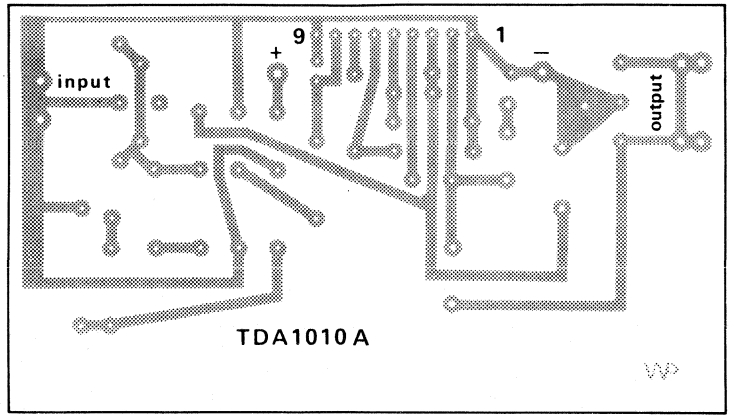


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

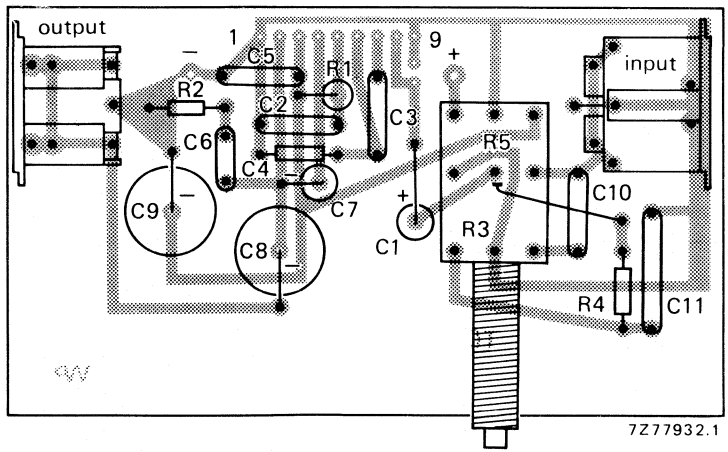


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

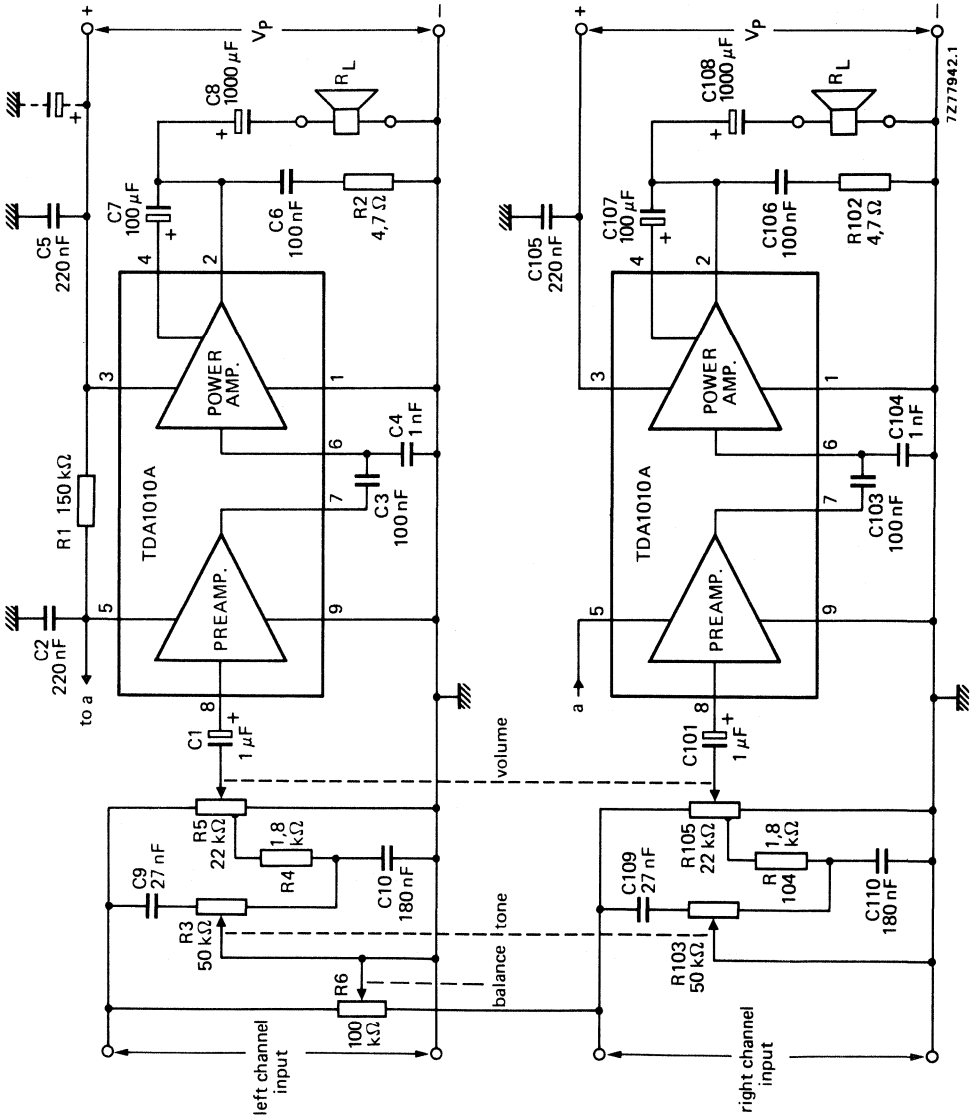


Fig. 12 Complete stereo car radio amplifier.

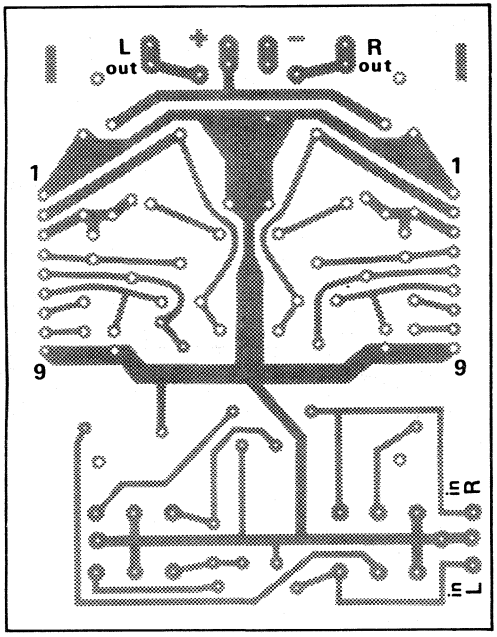


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

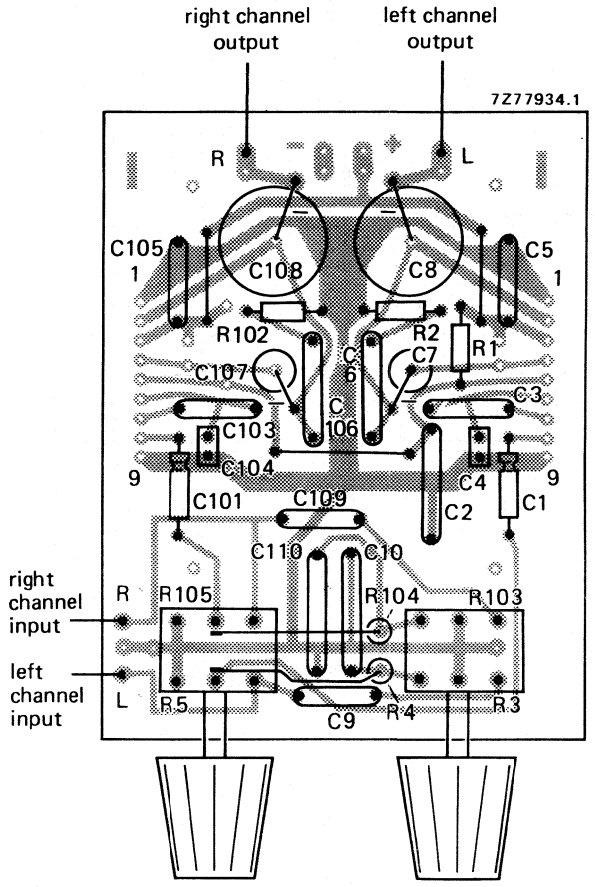


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

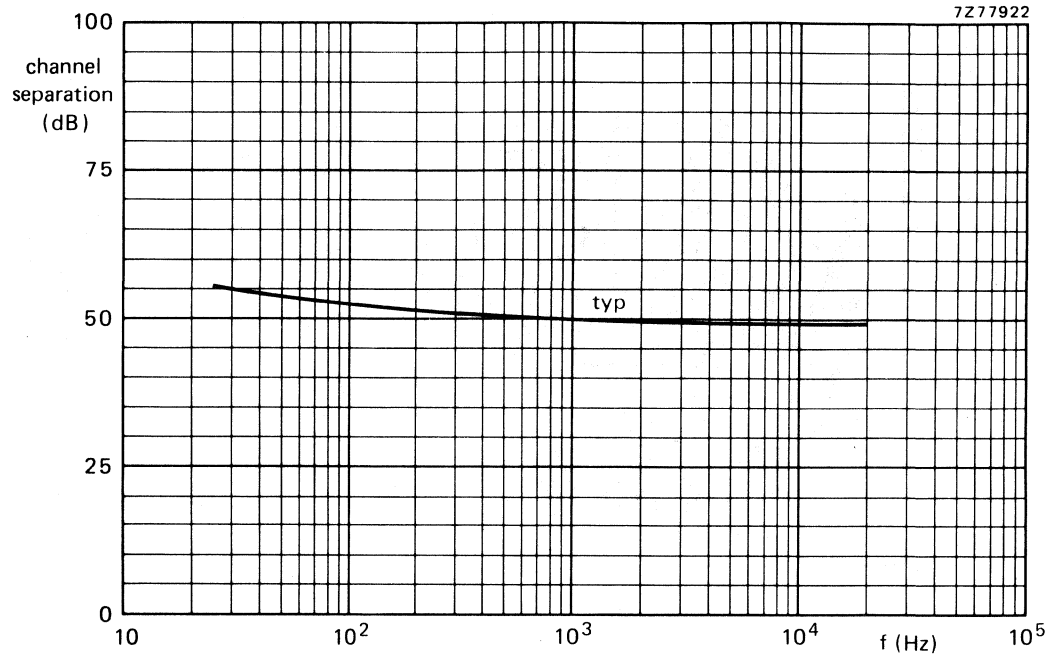


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

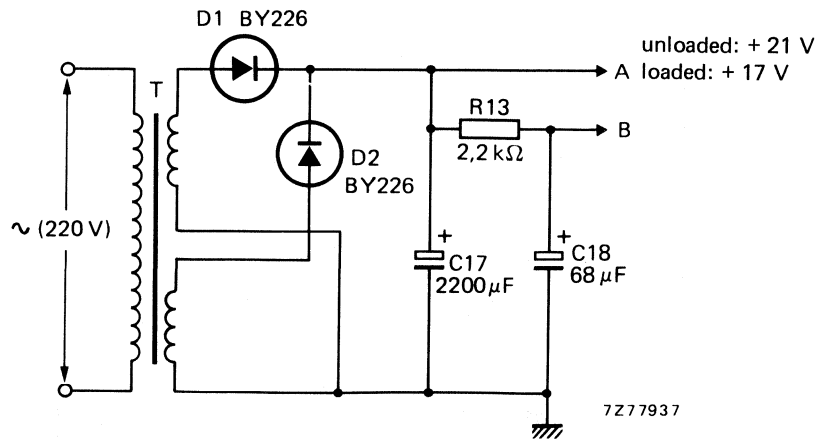


Fig. 16 Power supply of circuit of Fig. 17.

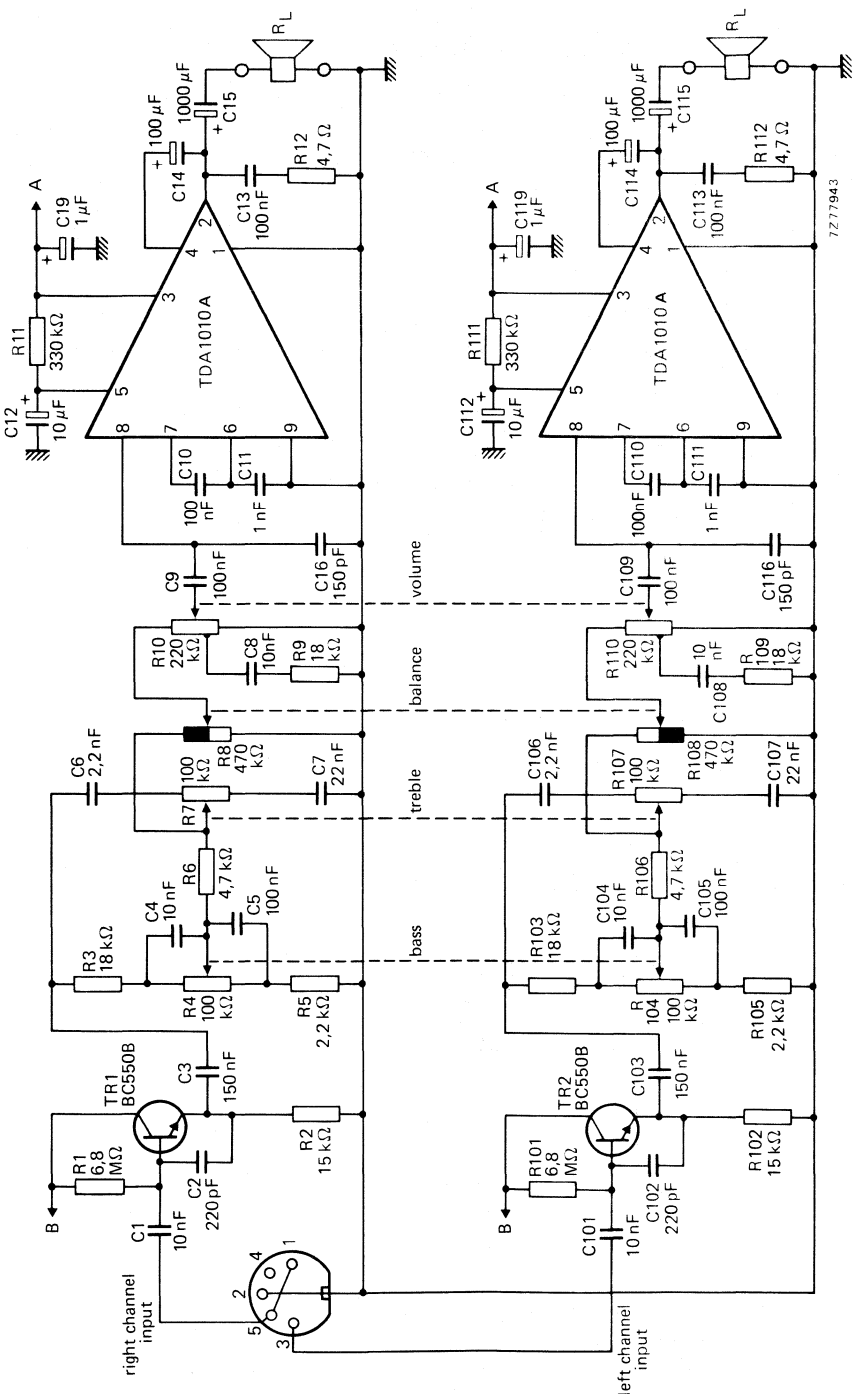


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

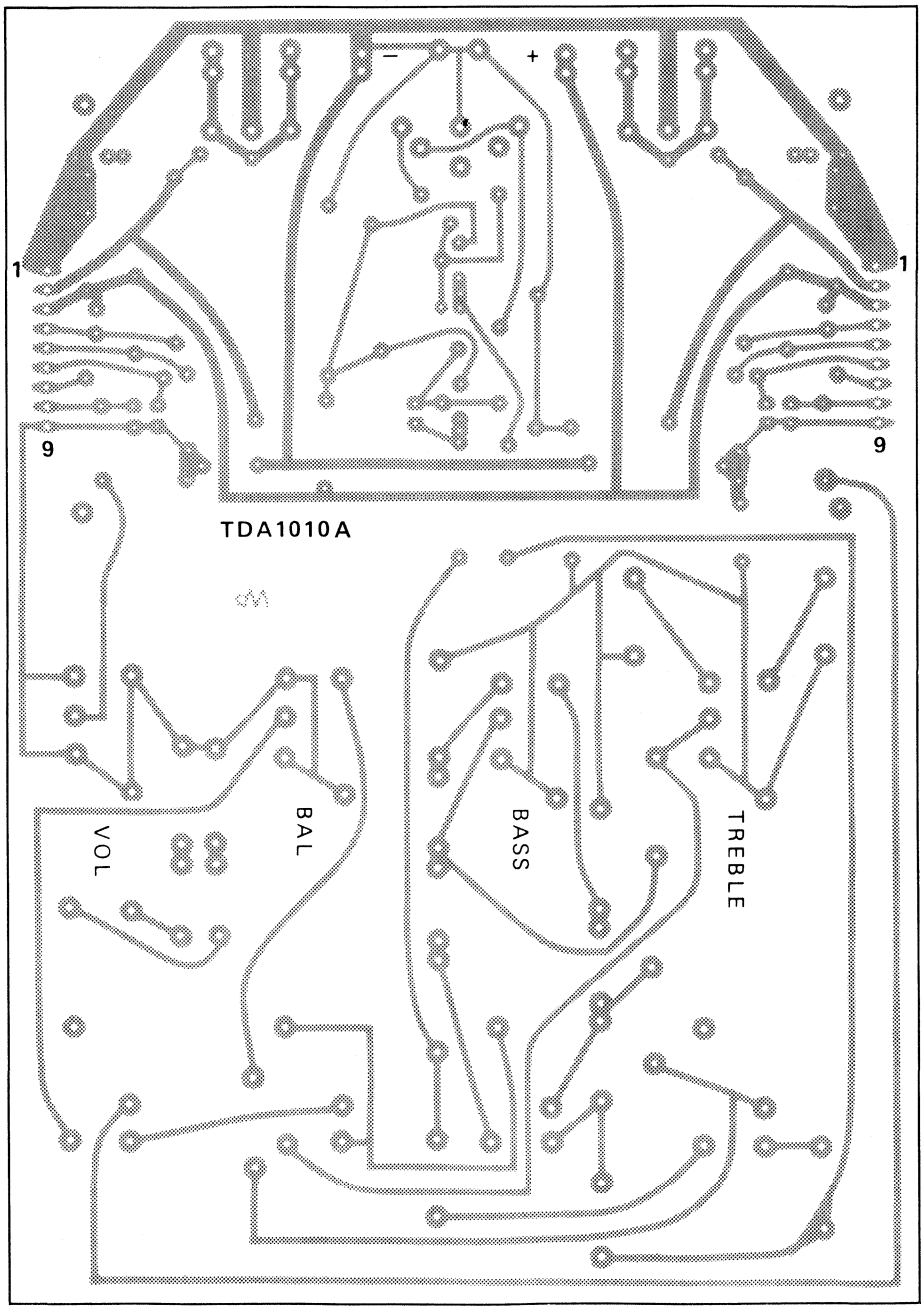


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Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

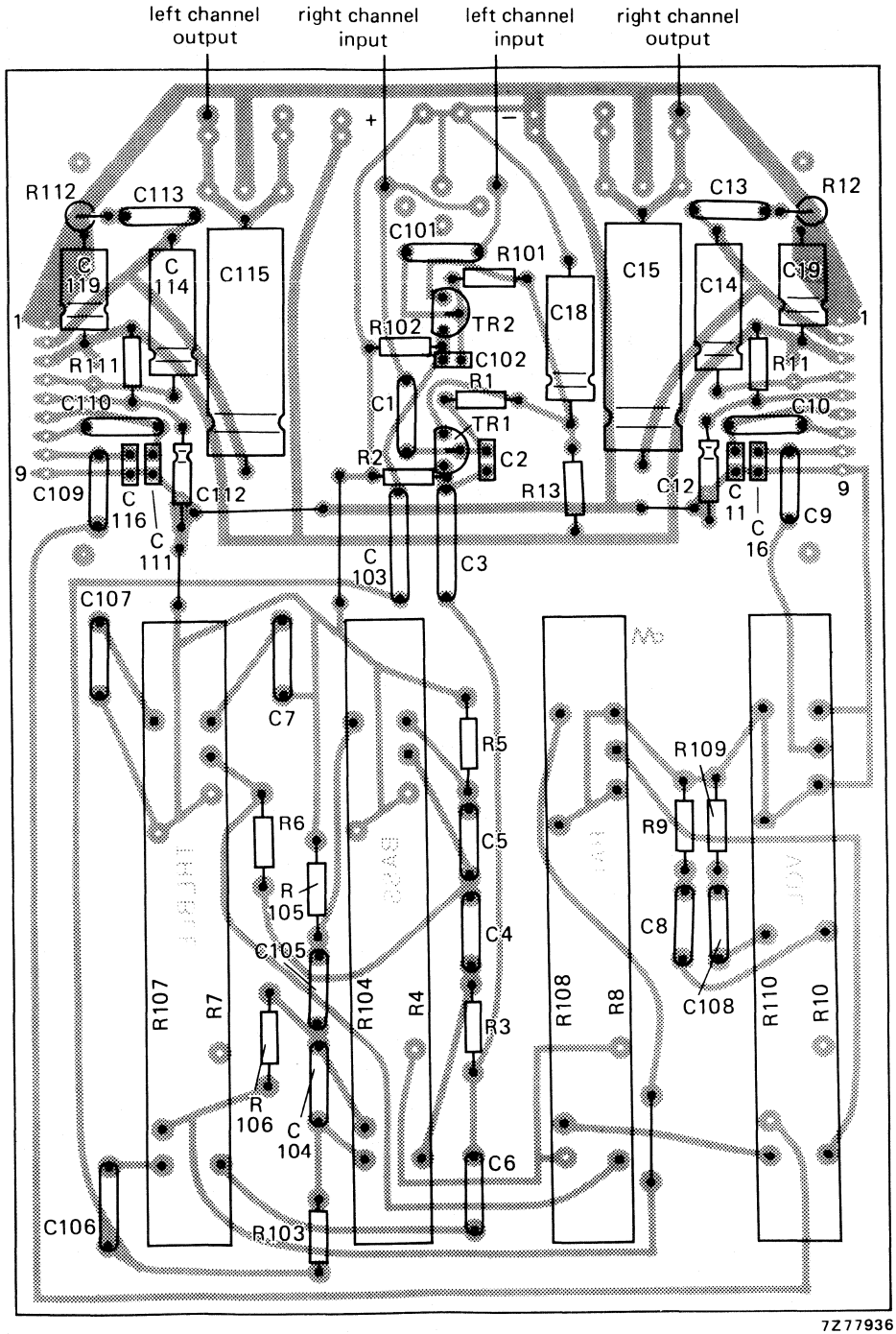


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

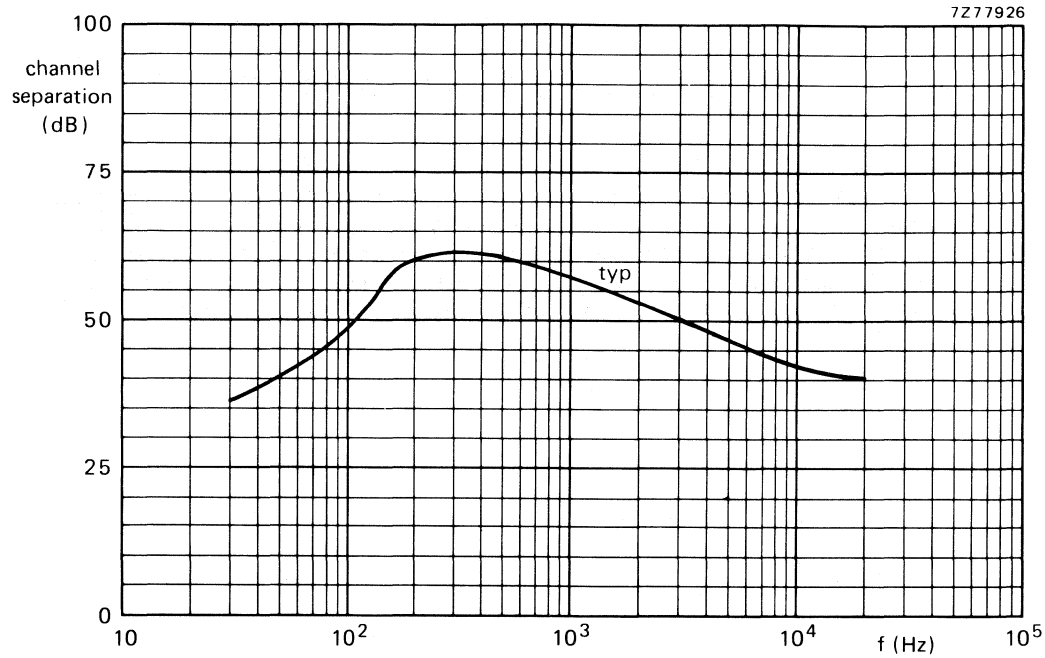


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 20	V
Peak output current	I_{OM}	max. 3	A
Output power at d_{tot} = 10%			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,2	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

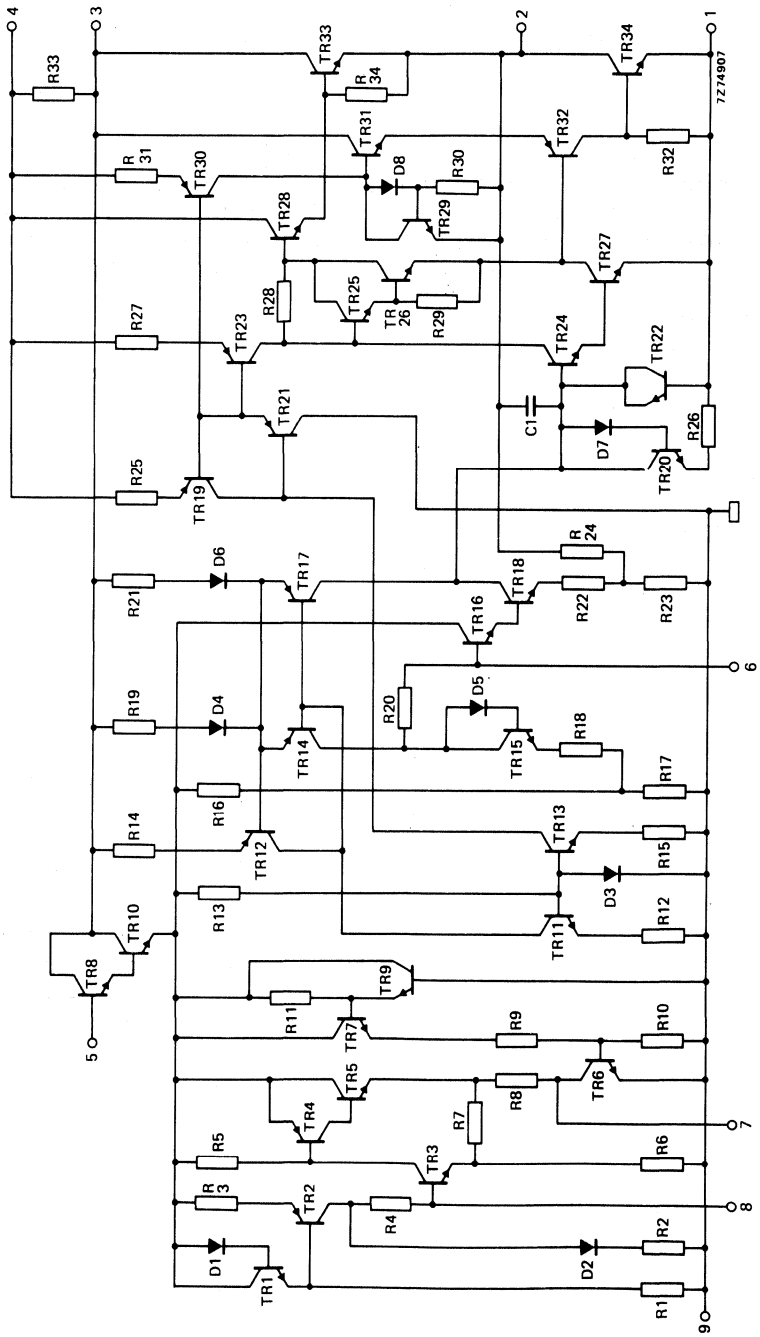


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

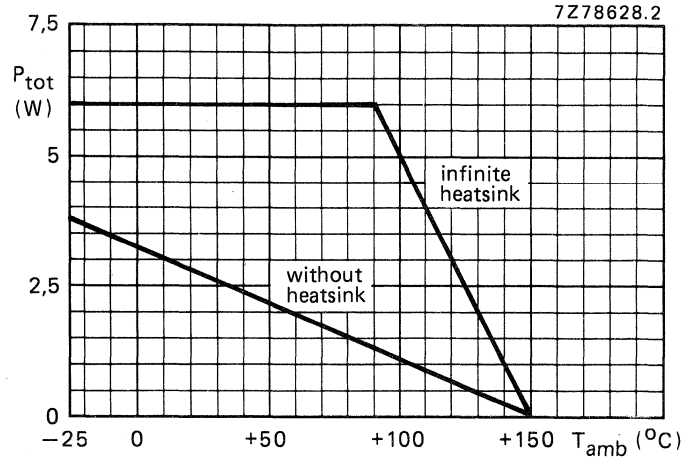


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{1{,}8} = 50\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 20	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 22	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	> 3,6 typ. 4,2	W W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23 21 to 25	dB dB
power amplifier	G_{v2}	typ. 29 27 to 31	dB dB
total amplifier	$G_{v\,tot}$	typ. 52 50 to 54	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,6 < 1,4	mV mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 1 to 10 kHz	RR	typ. 42	dB
f = 100 Hz; C2 = 1 μF	RR	> 35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

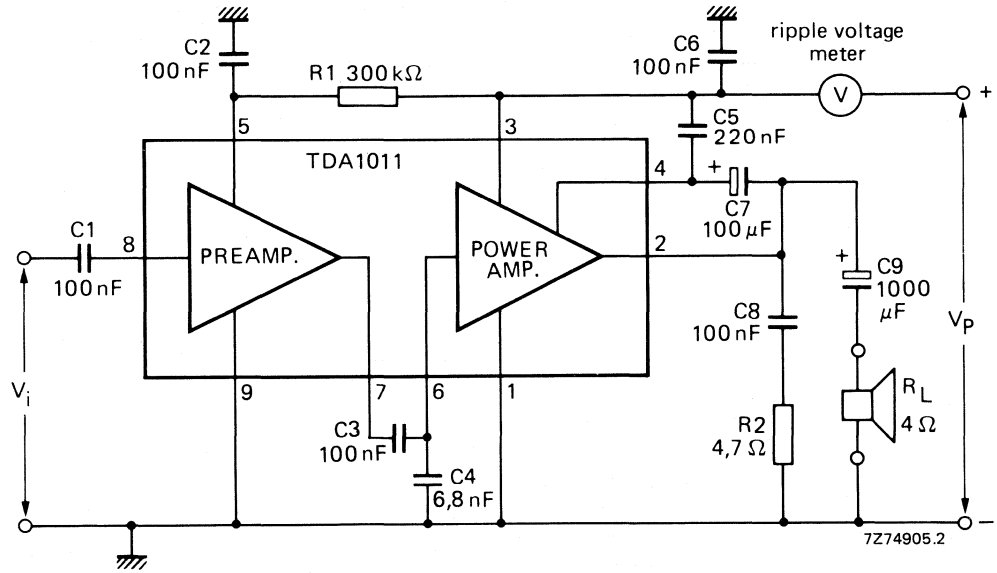


Fig. 3 Test circuit.

APPLICATION INFORMATION

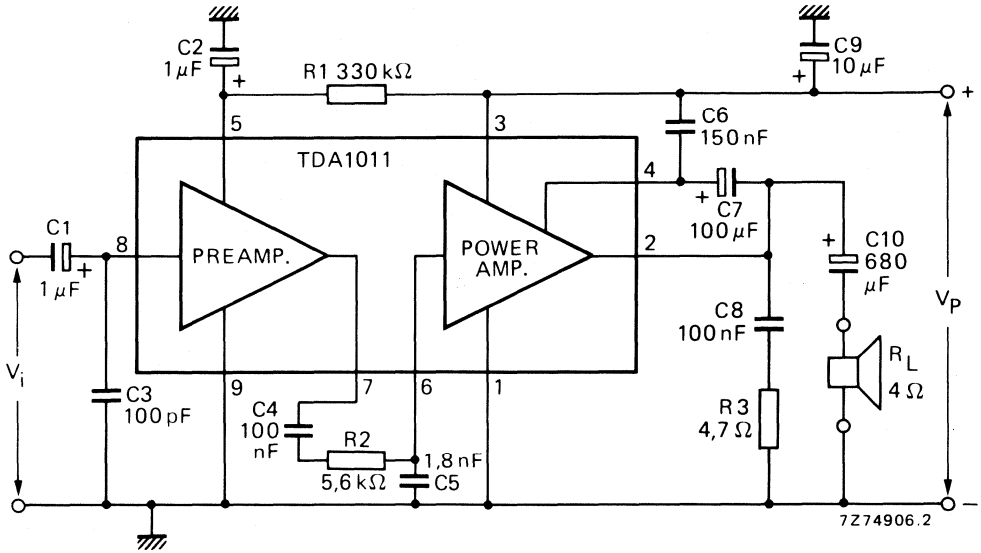


Fig. 4 Circuit diagram of a 4 W amplifier.

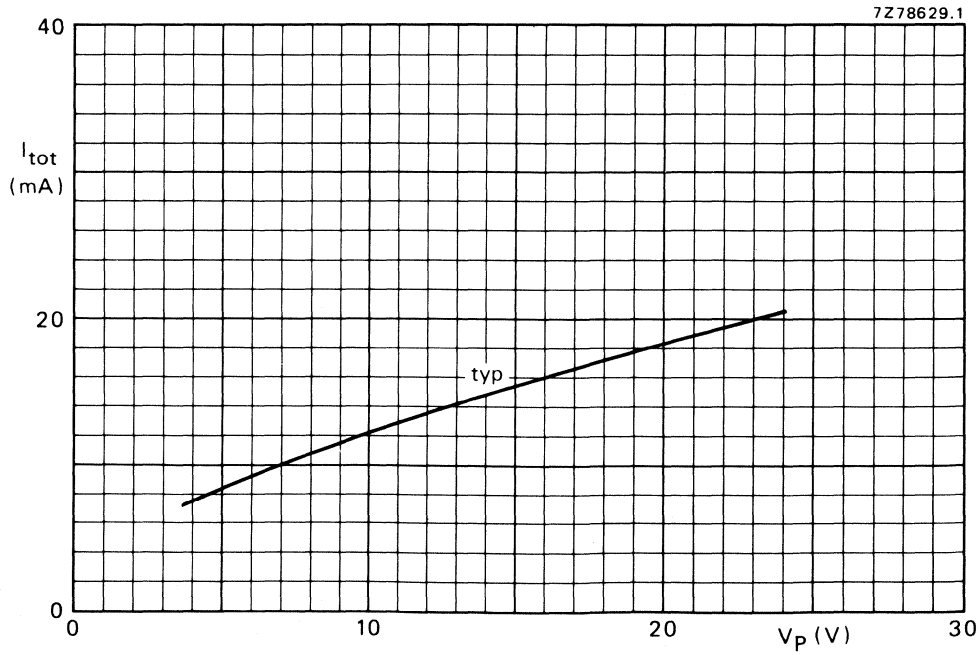


Fig. 5 Total quiescent current as a function of supply voltage.

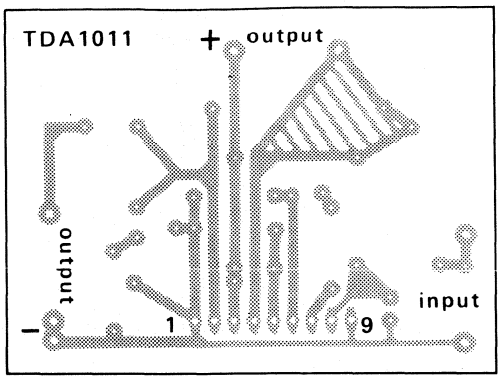


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

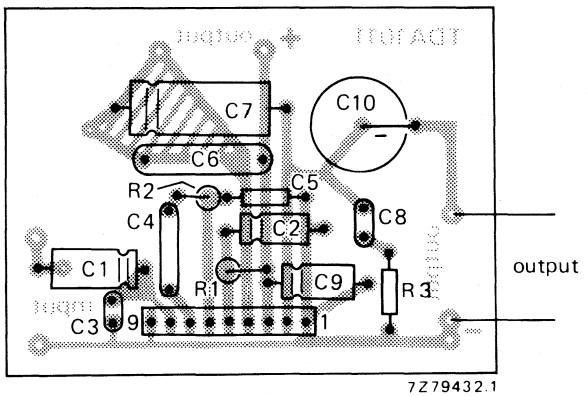


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

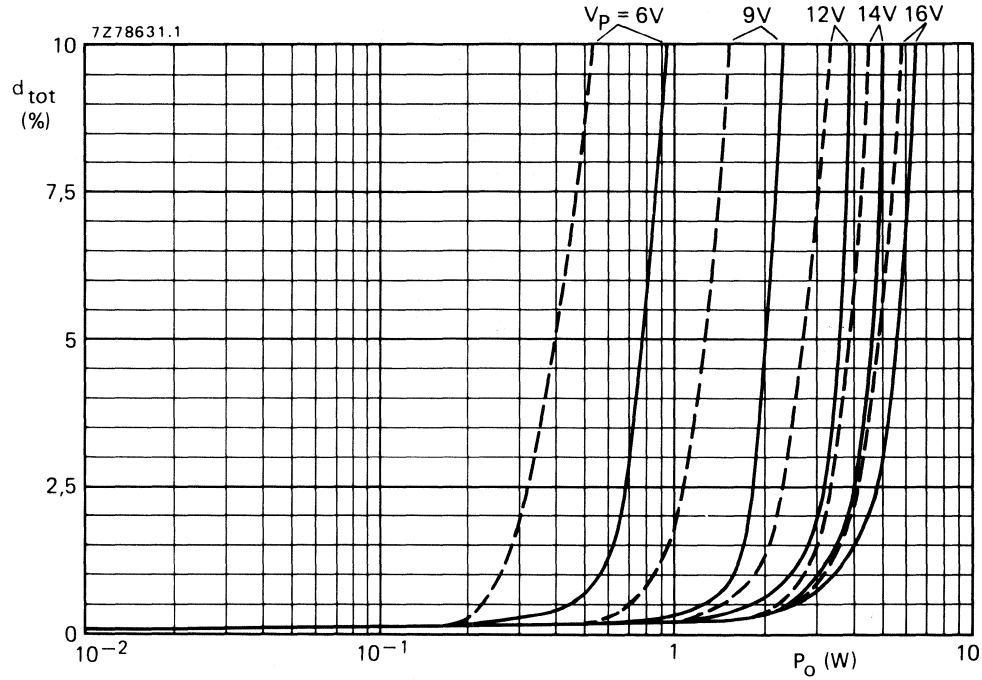


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; — — — without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

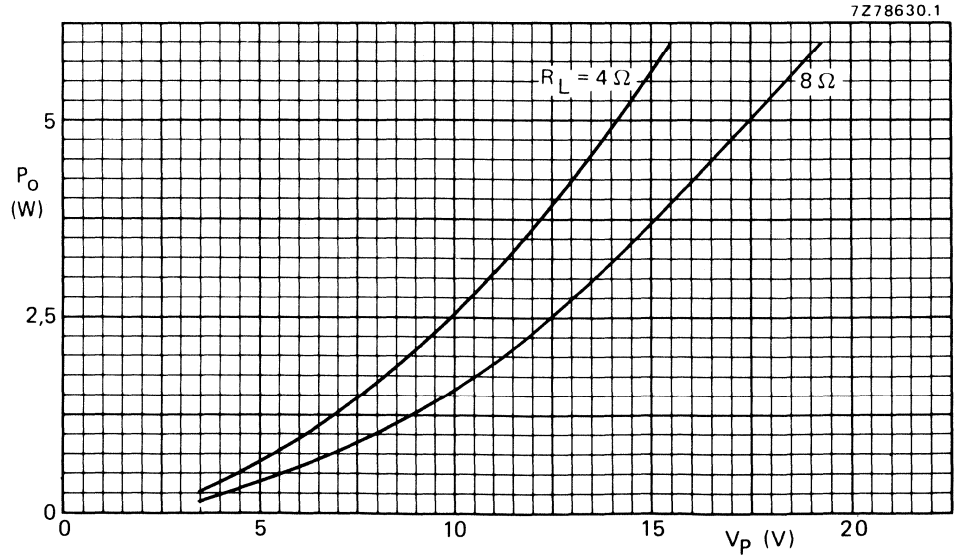


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

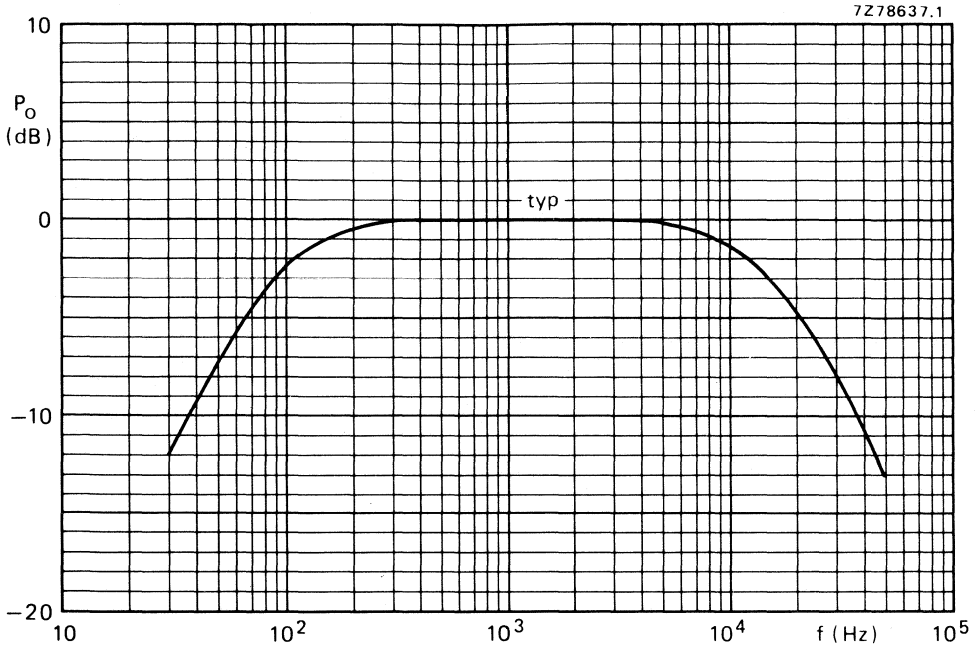


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

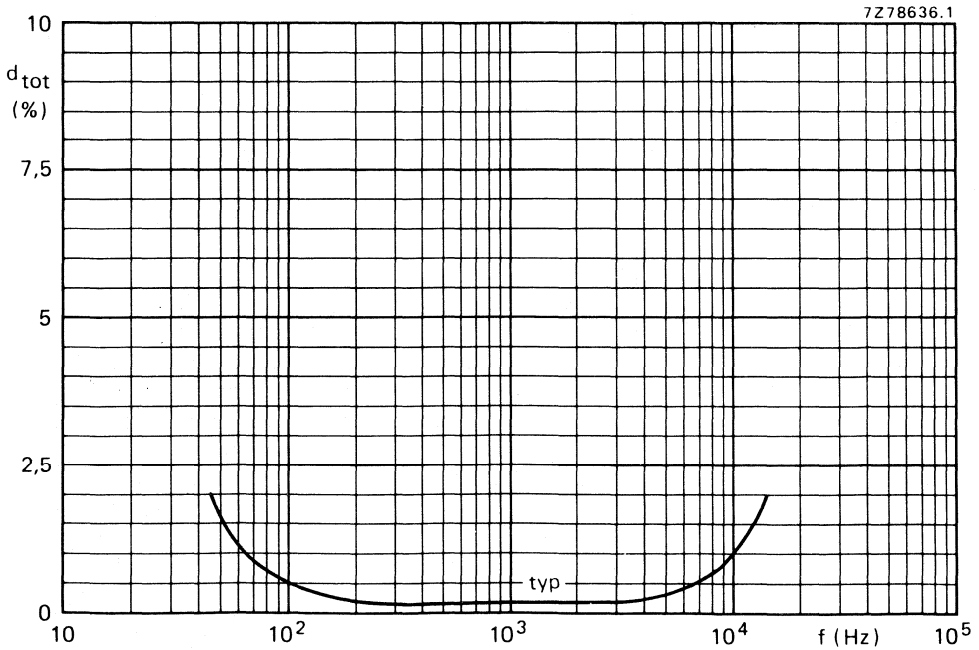


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

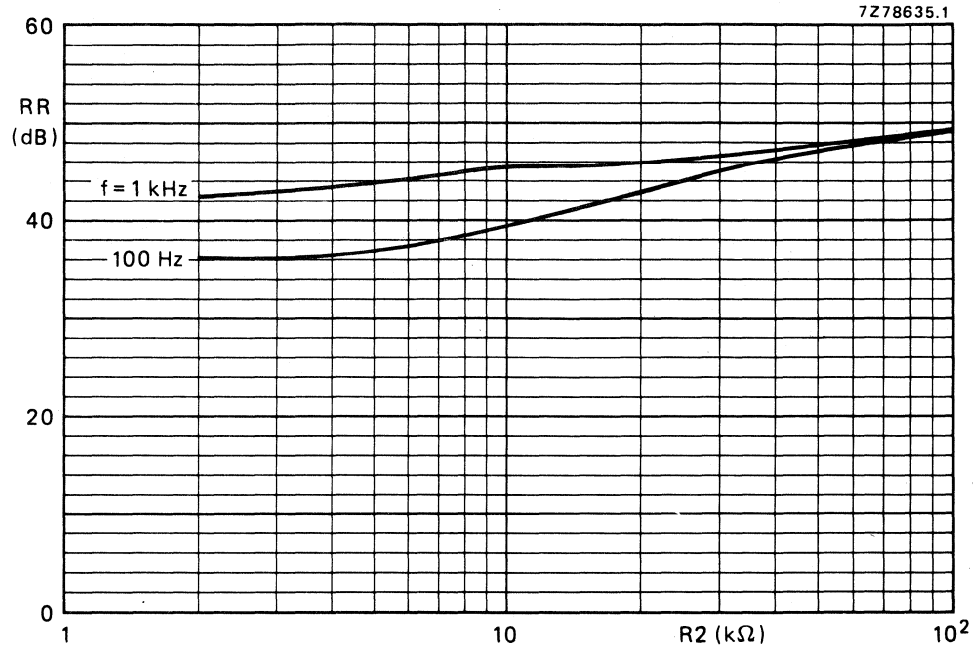


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

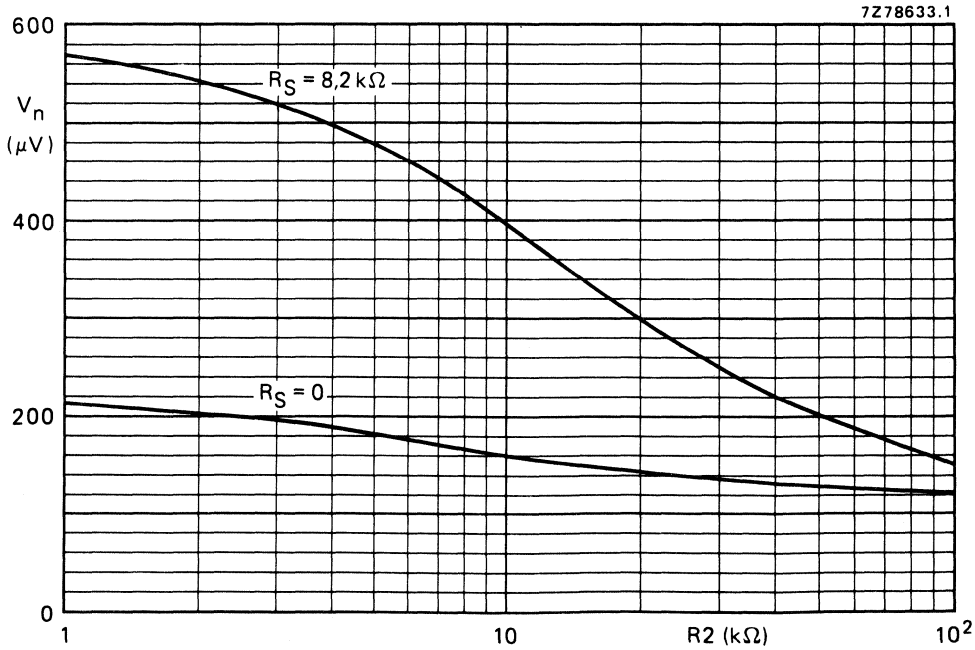


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

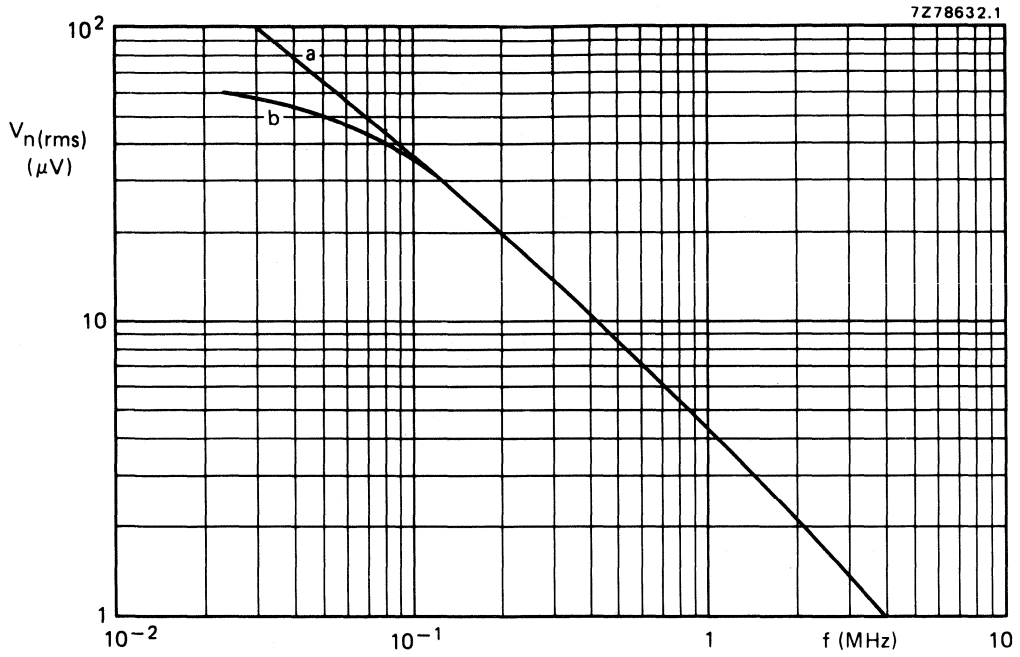


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

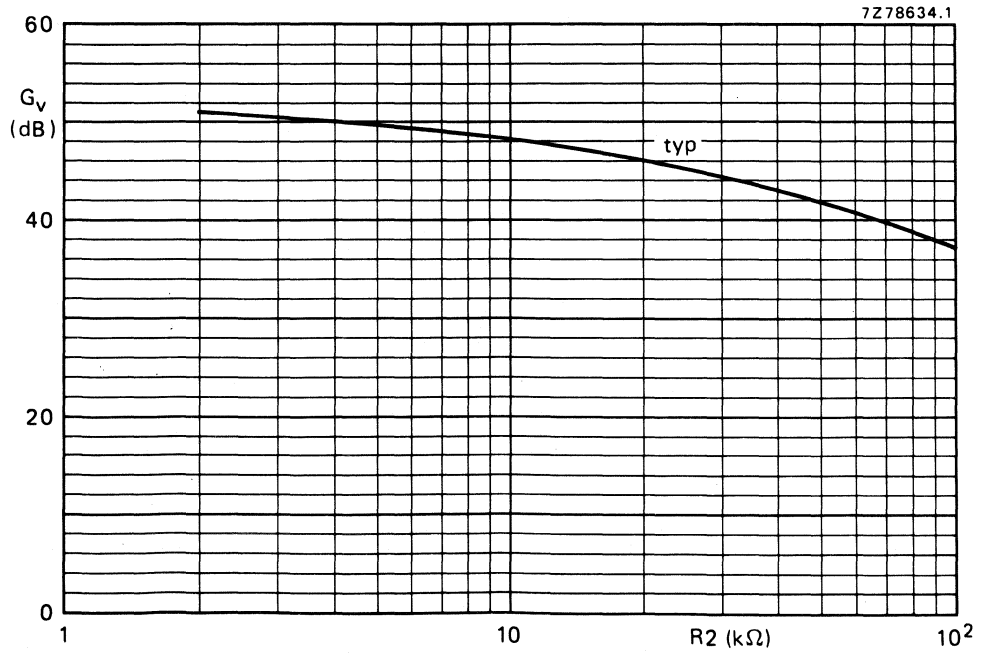


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

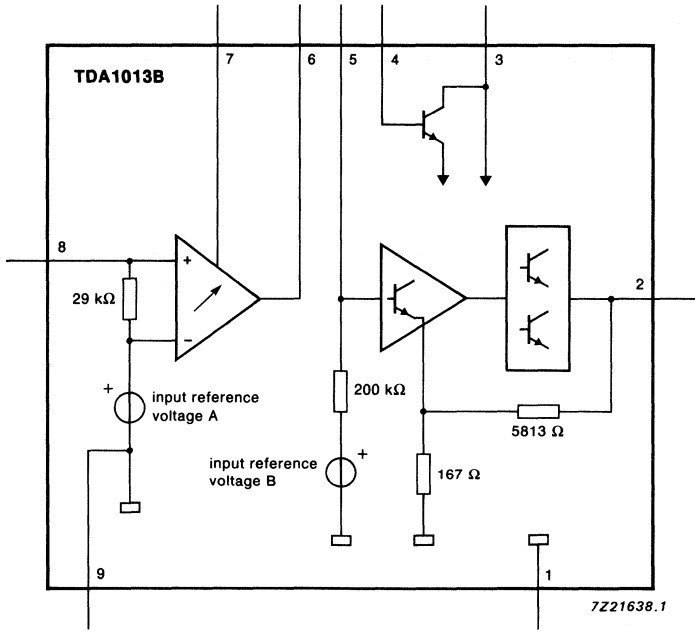


Fig.1 Block diagram.

PINNING

1 signal ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 power ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–55	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

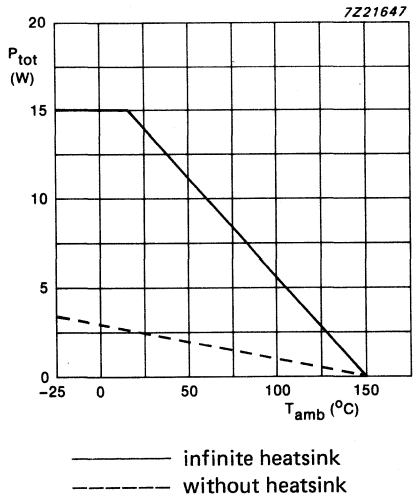


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

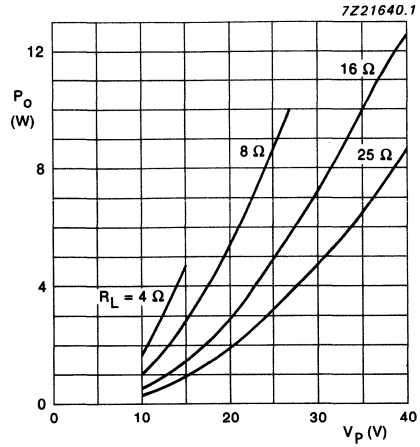


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

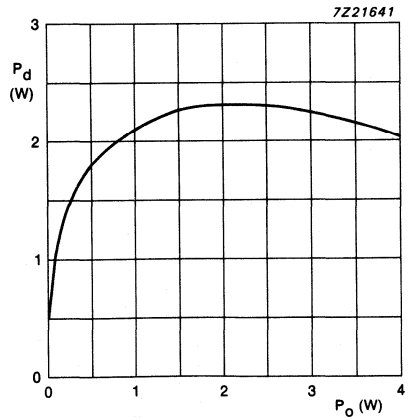


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

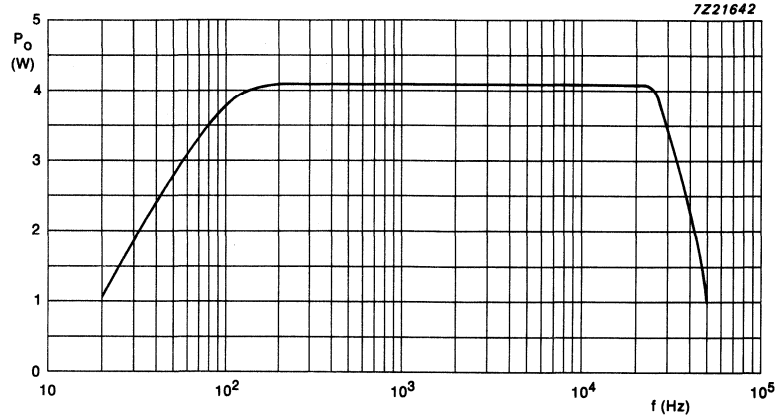


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω; THD = 10% and control voltage (V_7) = 6.5 V.

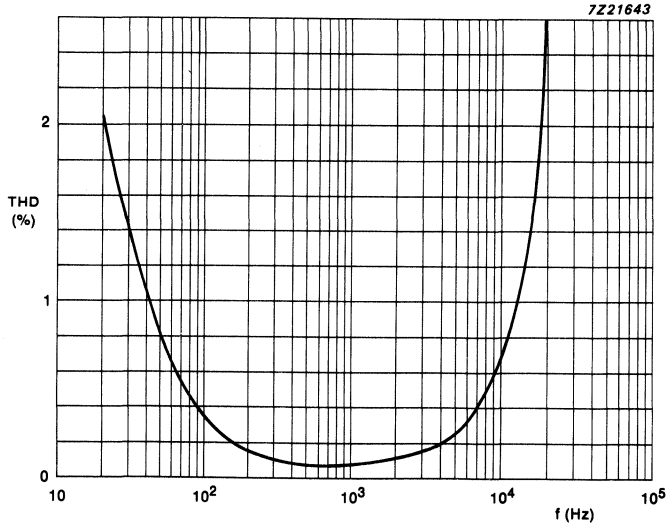


Fig.6 Total harmonic distortion as a function of frequency; V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

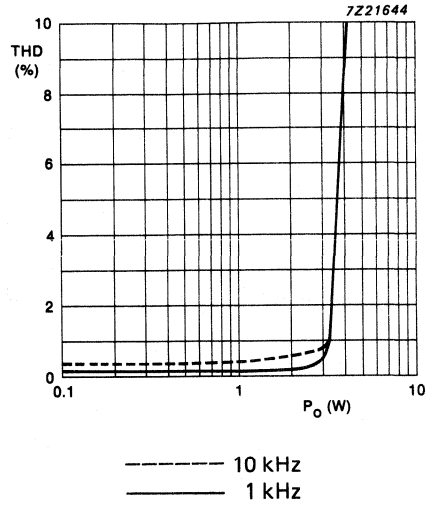


Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

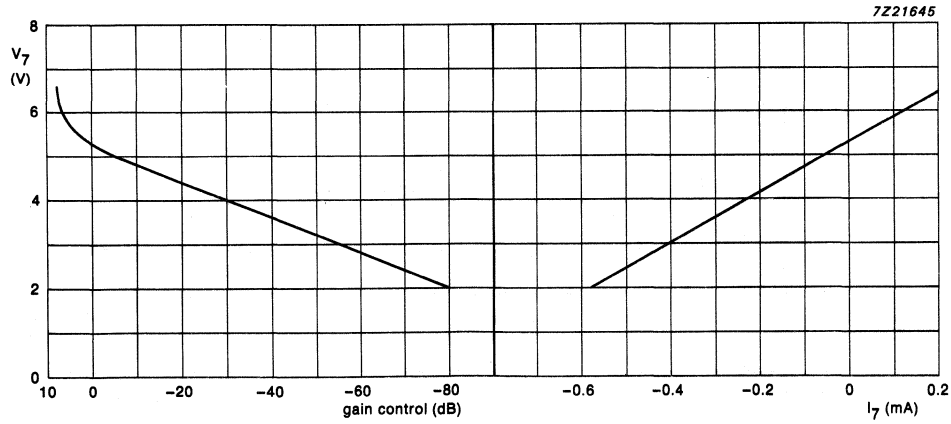


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

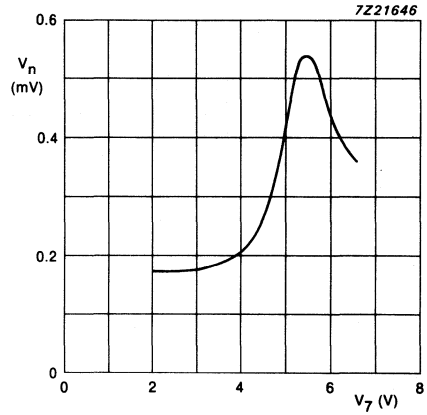
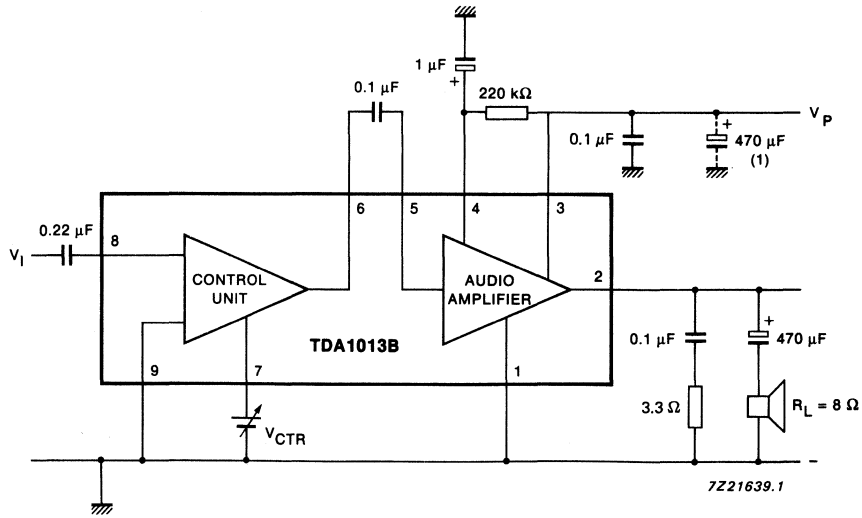


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	> 100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

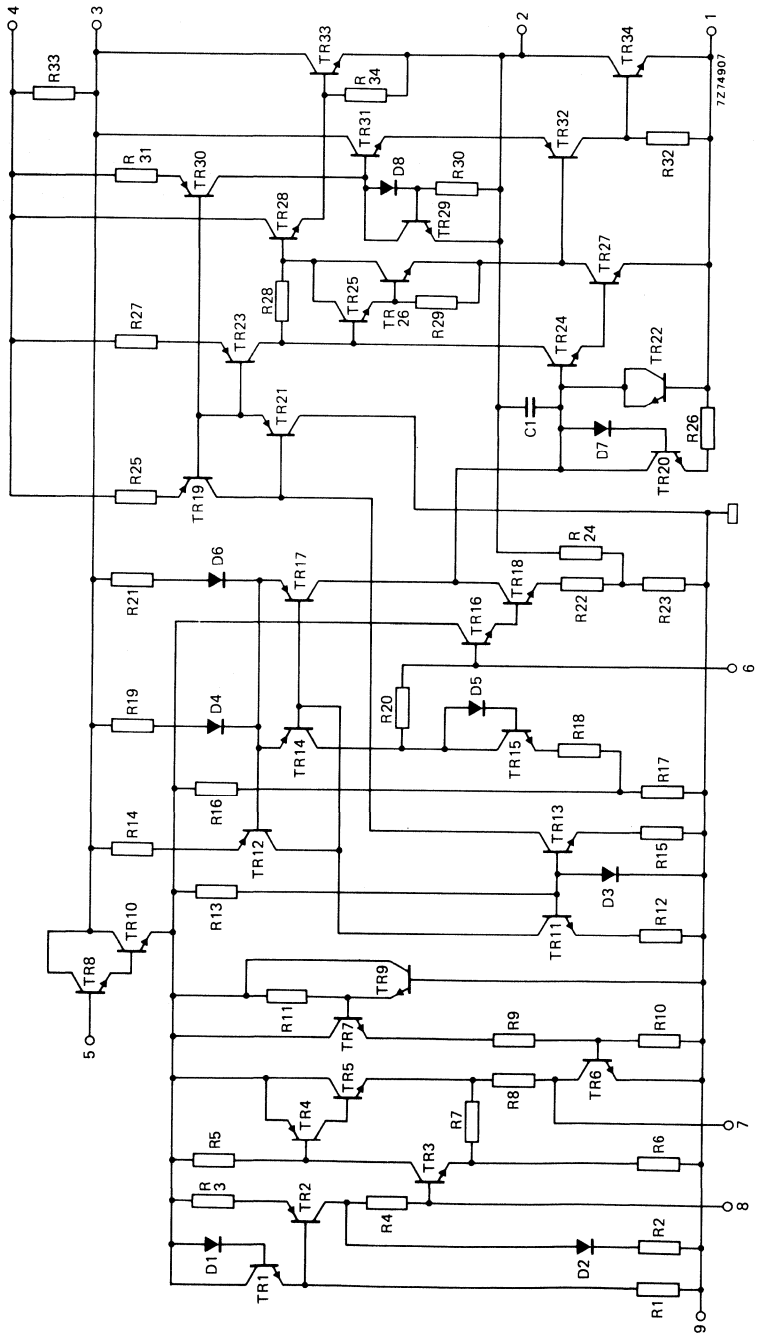


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Peak output current	I_{OM}	max.	2,5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

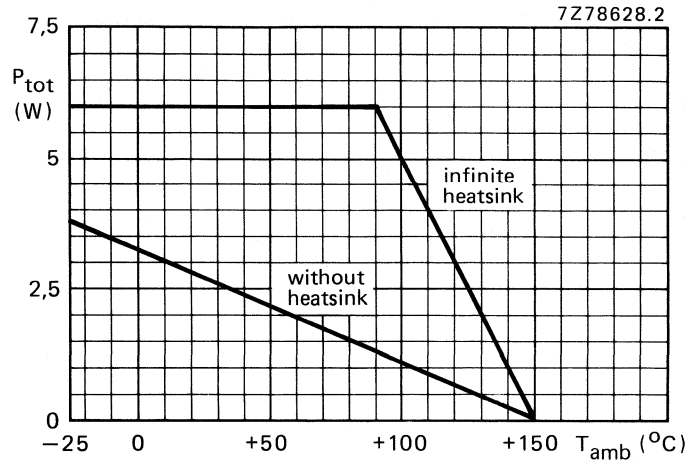


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1,8} = 58\ K/W.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

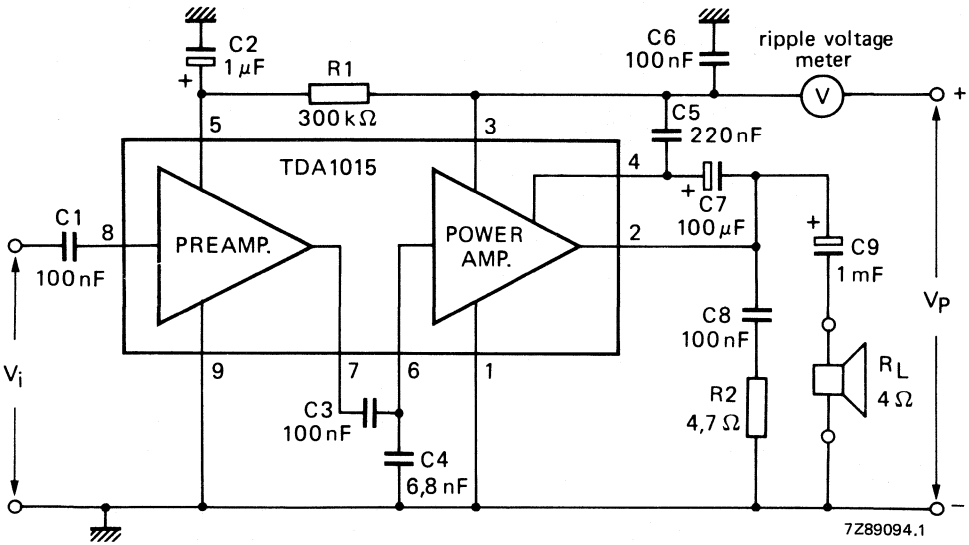


Fig. 3 Test circuit.

APPLICATION INFORMATION

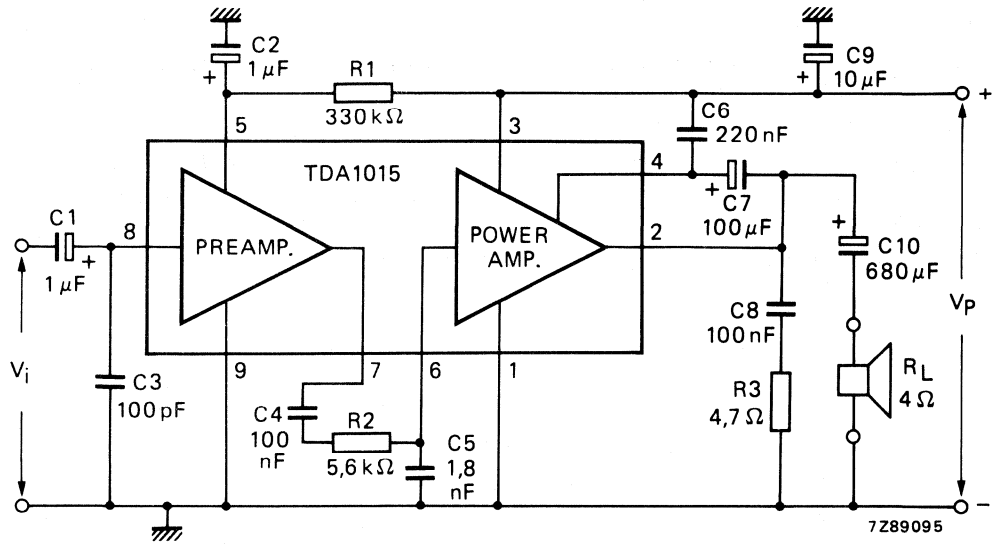


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

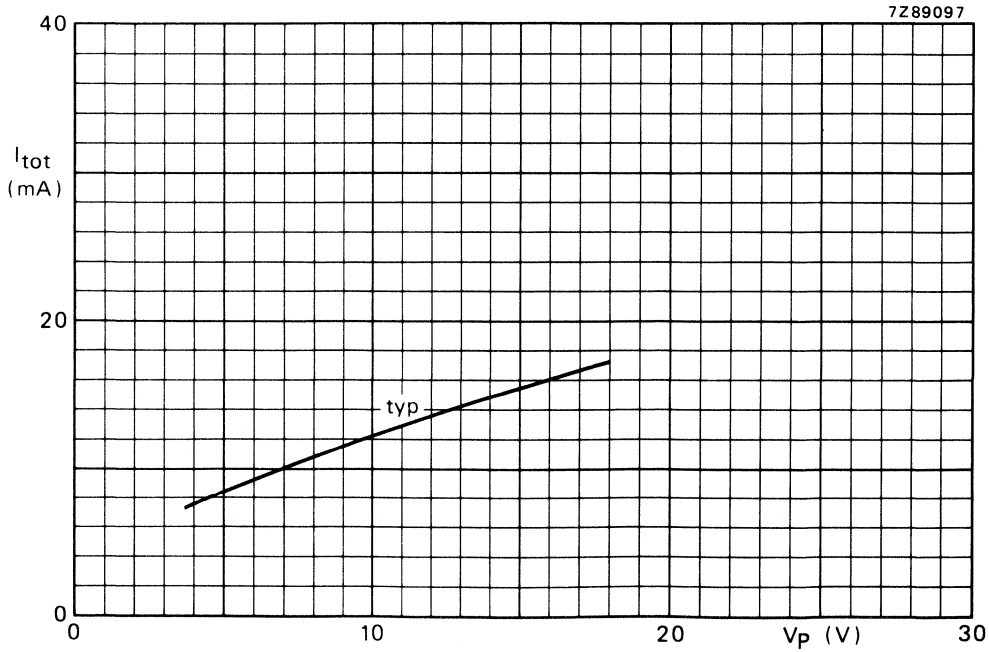


Fig. 5 Total quiescent current as a function of supply voltage.

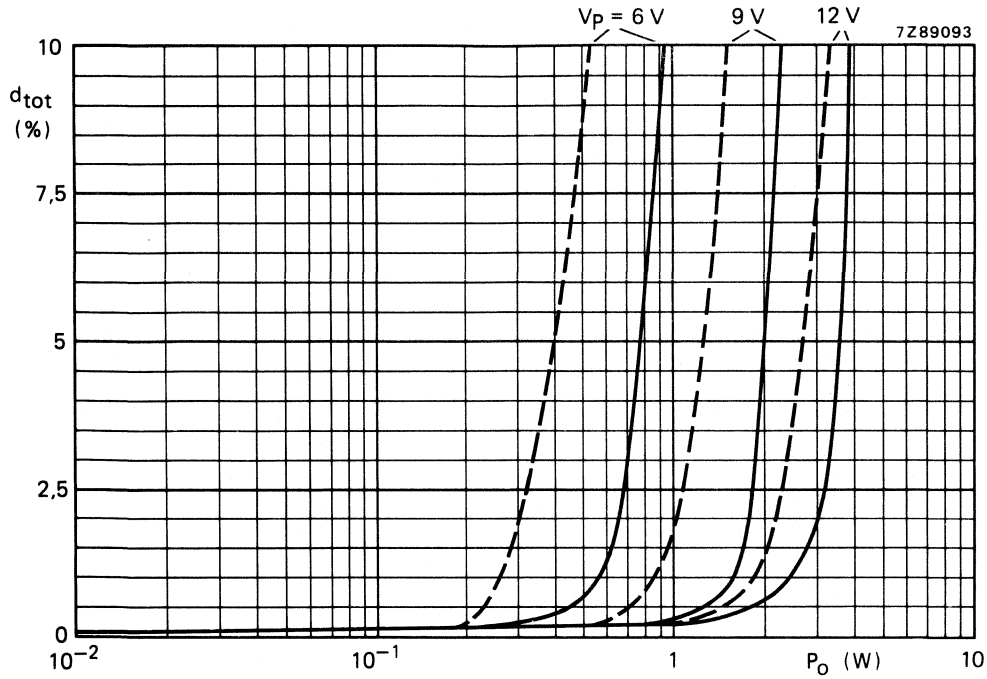


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; — — — without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

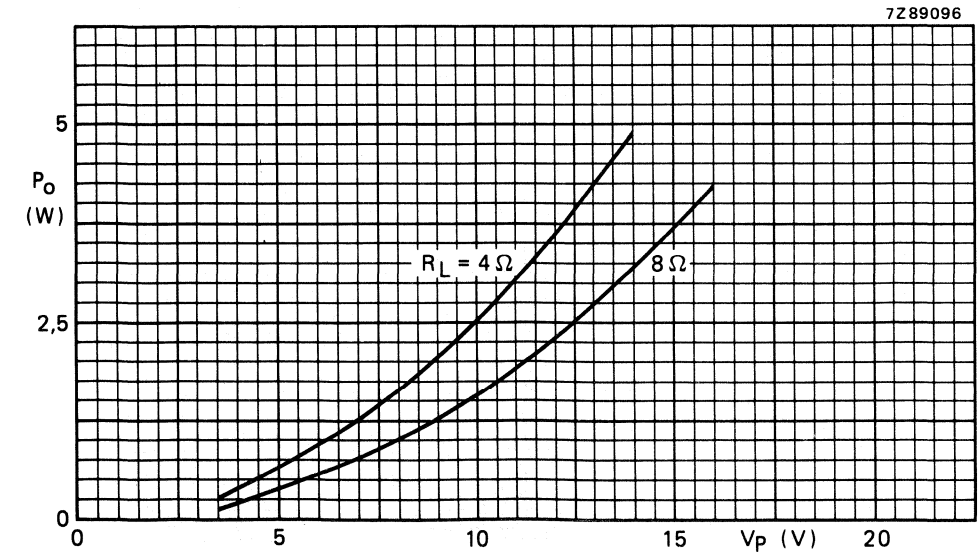


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

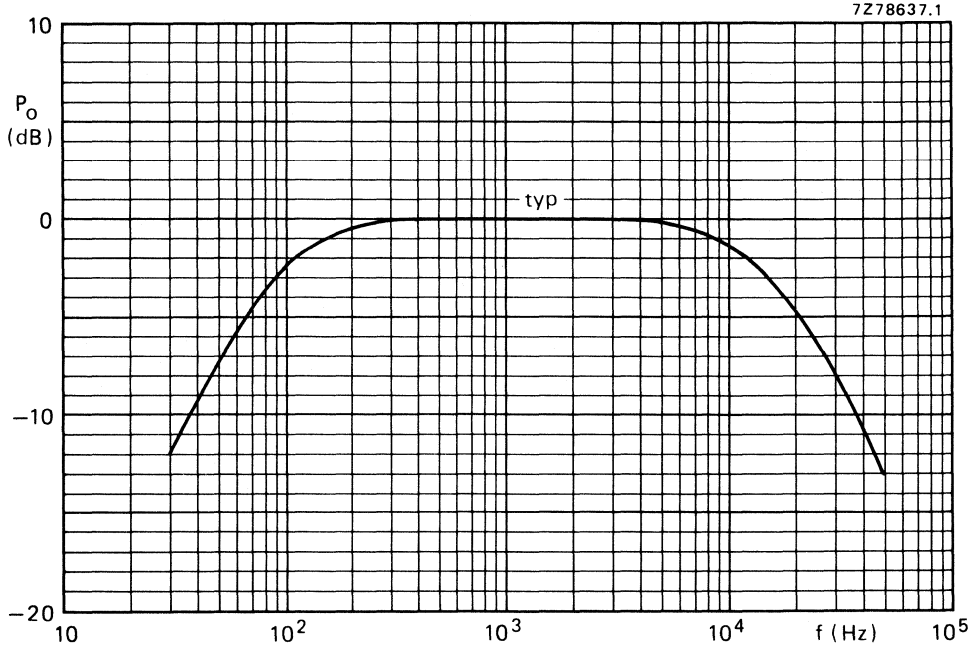


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

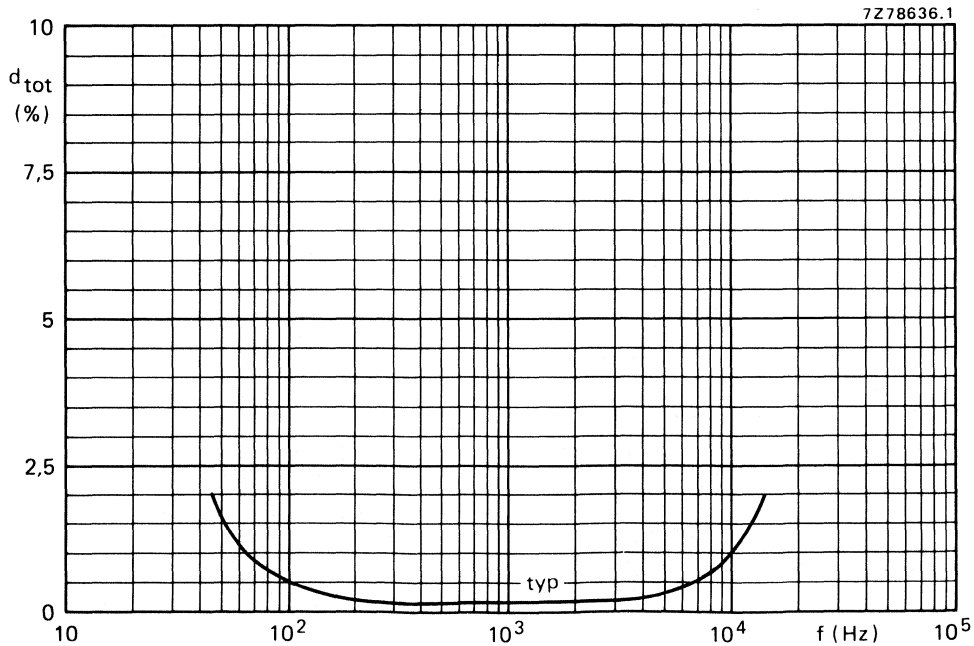


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

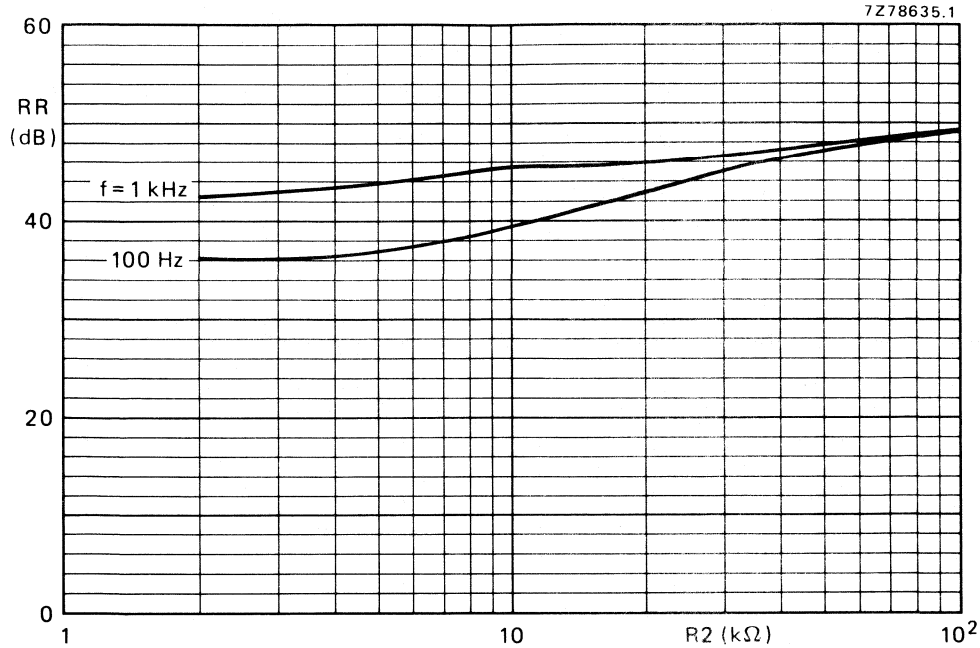


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

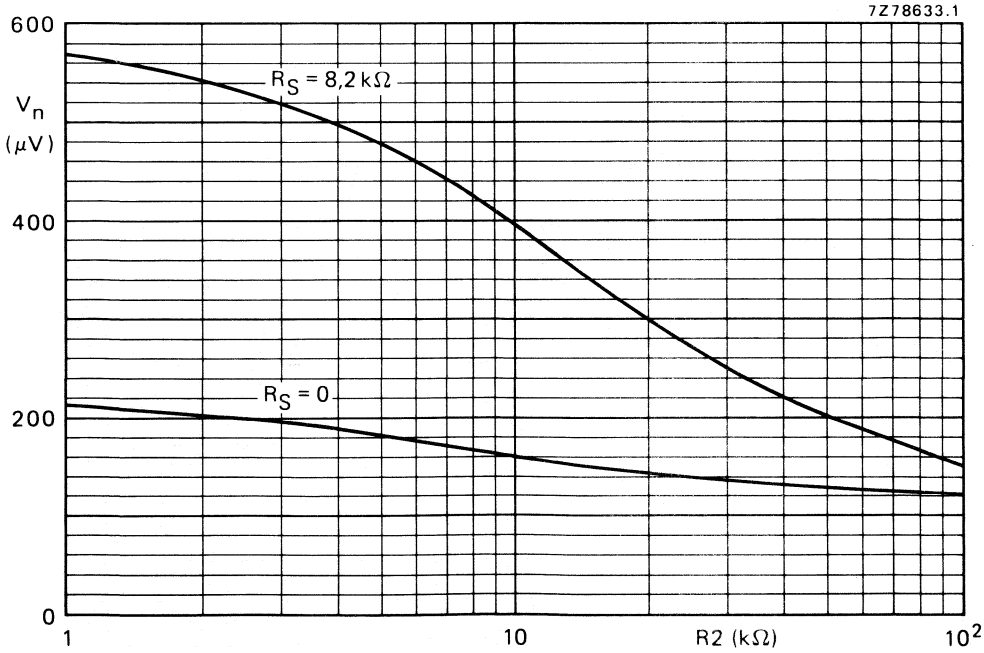


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

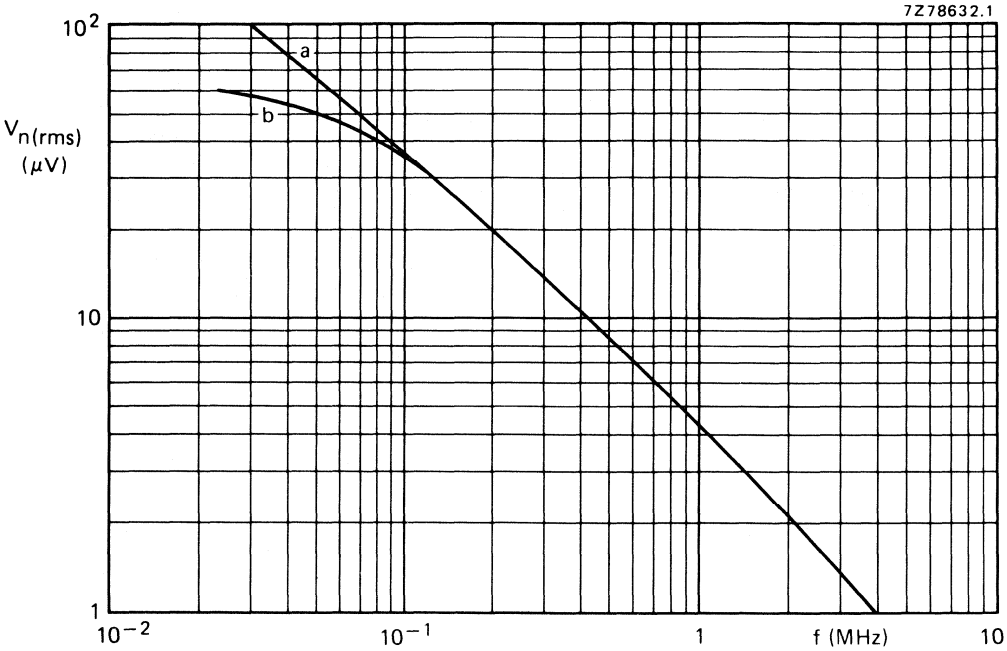


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

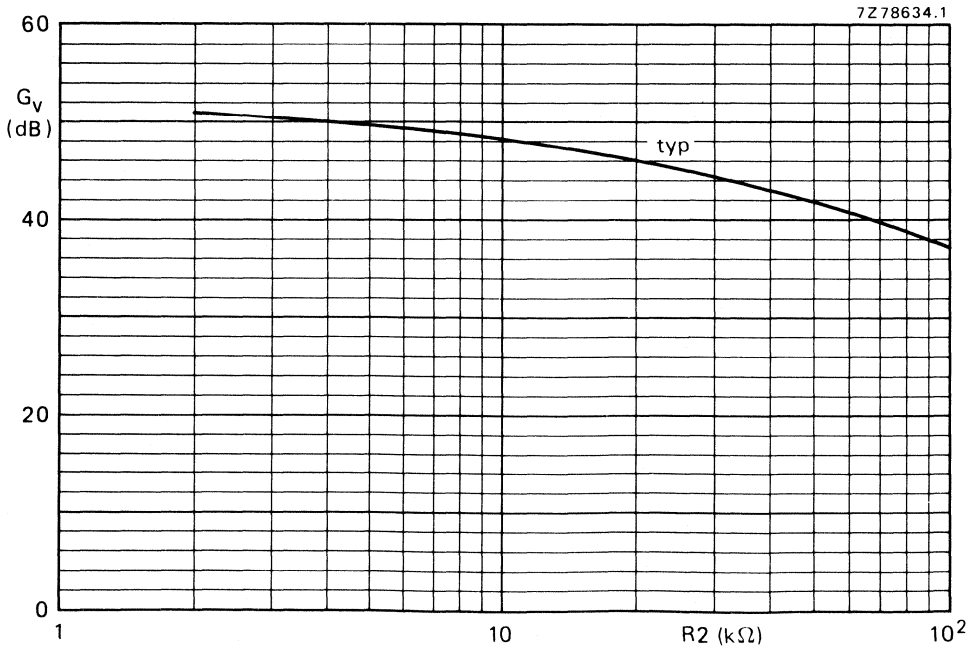


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

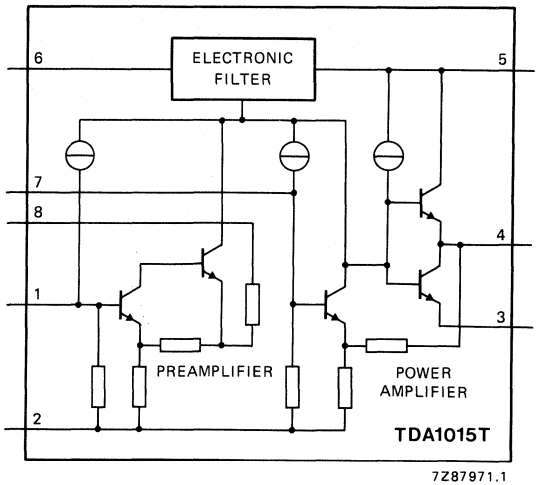


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

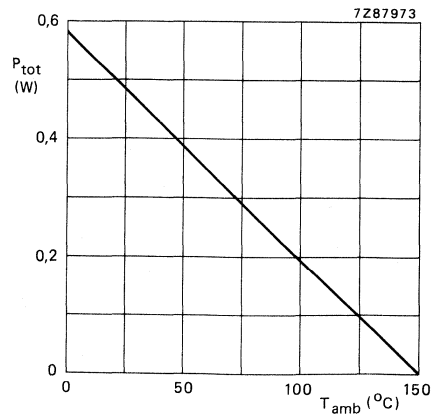


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

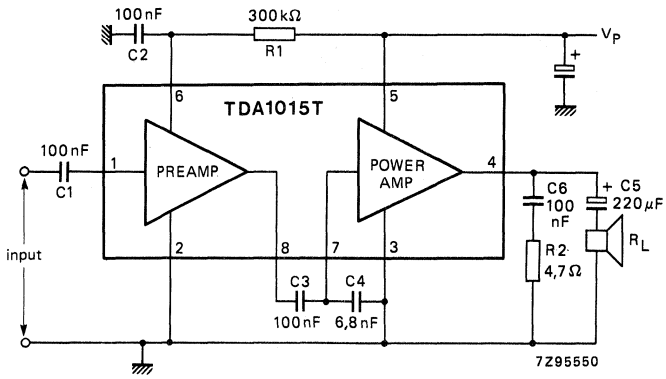


Fig. 3 Test circuit.

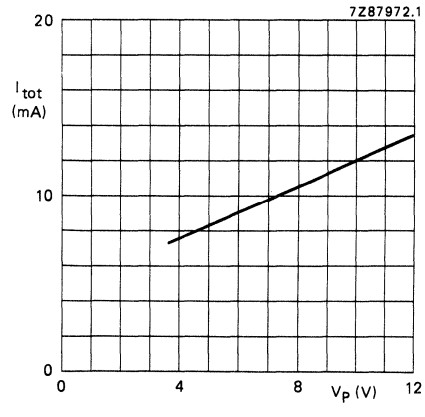


Fig. 4 Total quiescent current as a function of supply voltage.

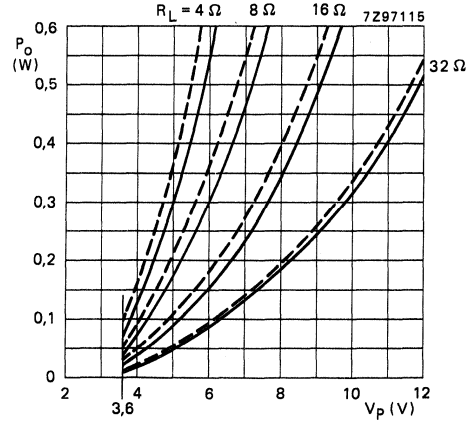


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

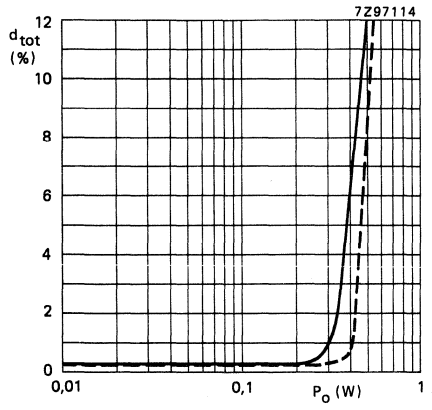


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

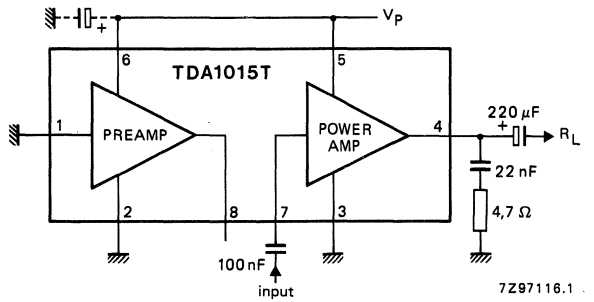


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

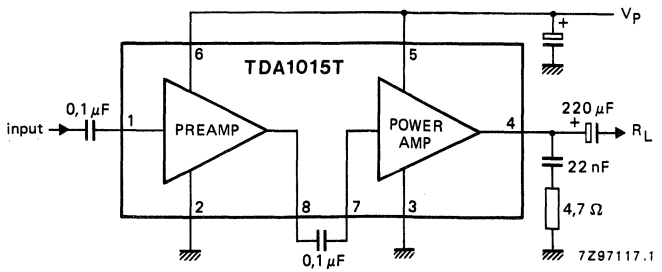


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\ tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

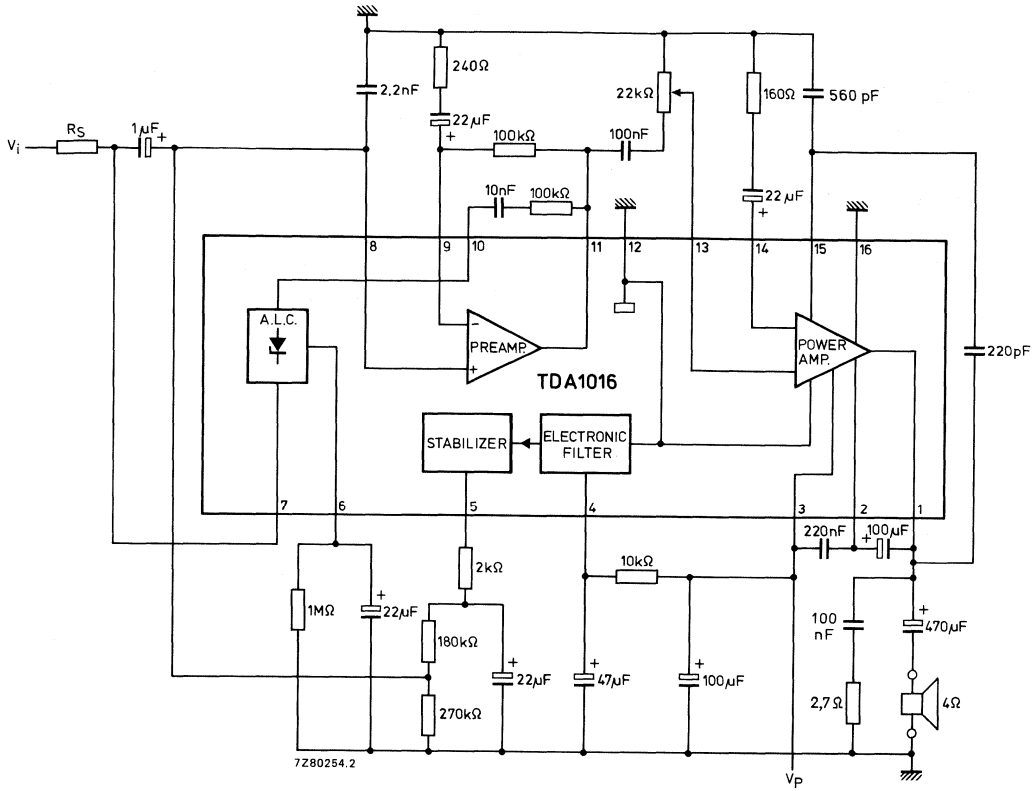


Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	V_P	max.	18	V
Repetitive peak output current	I_{ORM}	max.	1	A
Non-repetitive peak output current (pin 1)	I_{OSM}	max.	2	A
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sinewave drive; V_P = 12 V	t_{sc}	max.	100	hours
Crystal temperature	T_c	max.	150	°C
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−25 to +	150	°C

THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient	$R_{th\ j\text{-}a}$	=	55	K/W

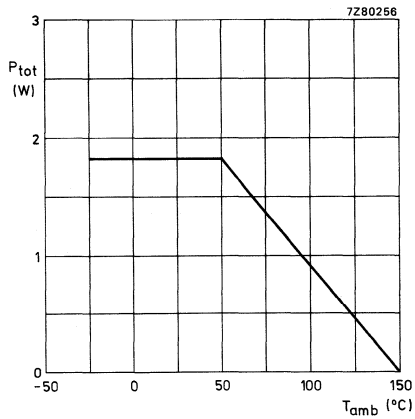


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	V_P	3,6	6	15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	–	10	–	mA
Power amplifier					
Output power at d_{tot} = 10%*					
V_P = 6 V	P_o	–	1	–	W
V_P = 9 V	P_o	–	2	–	W
Closed loop voltage gain	G_c	–	36	–	dB
Total harmonic distortion at P_o = 0,5 W	d_{tot}	–	–	1	%
Input impedance	$\|Z_i\|$	0,5	–	–	MΩ
Ripple rejection at f = 100 Hz (R_S = 0 Ω)	RR	40	50	–	dB
Noise output voltage (r.m.s. value) R_S = 0 Ω; B = 60 Hz to 15 kHz	$V_{n(rms)}$	–	90	200	μV
Noise output voltage at 500 kHz R_S = 0 Ω; B = 5 kHz	V_n	–	8	–	μV
Preamplifier					
Open loop voltage gain at f = 10 kHz	G_o	70	78	–	dB
Closed loop voltage gain	G_c	–	52	–	dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\,min}$	35	–	–	dB
Output voltage at d_{tot} = 1%	V_o	1	–	–	V
Output voltage with A.L.C. V_i = 2 mV	V_o	0,45	0,5	0,55	V
Total harmonic distortion with A.L.C.					
V_i = 2 mV	d_{tot}	–	–	1	%
V_i = 360 mV	d_{tot}	–	–	3	%
Signal-to-noise ratio related to V_i = 1,2 mV; R_S = 1 kΩ; B = 60 Hz to 15 kHz	S/N	–	60	–	dB
Input impedance	$\|Z_i\|$	100	–	–	kΩ
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	50	54	–	dB
Output impedance **	$\|Z_o\|$	–	–	50	Ω

* Measured with an ideal coupling capacitor connected to the speaker load.

** I_P (effective value) must not exceed 1 mA.

parameter	symbol	min.	typ.	max.	unit
Automatic Level Control (A.L.C.) (see Fig. 3)**					
Gain variation for ΔV_i = 45 dB	ΔG_v	–	2	3	dB
Limiting time*	t_l	–	–	50	ms
Level setting time*	t_s	–	–	50	ms
Recovery time* ▲	t_r	–	100	–	s
Voltage stabilizer					
Output voltage	$V_{11\text{-}15}$	–	2,6	–	V
Load current	I_{11}	–	–	1,5	mA
Ripple rejection at f = 100 Hz	RR	40	–	–	dB

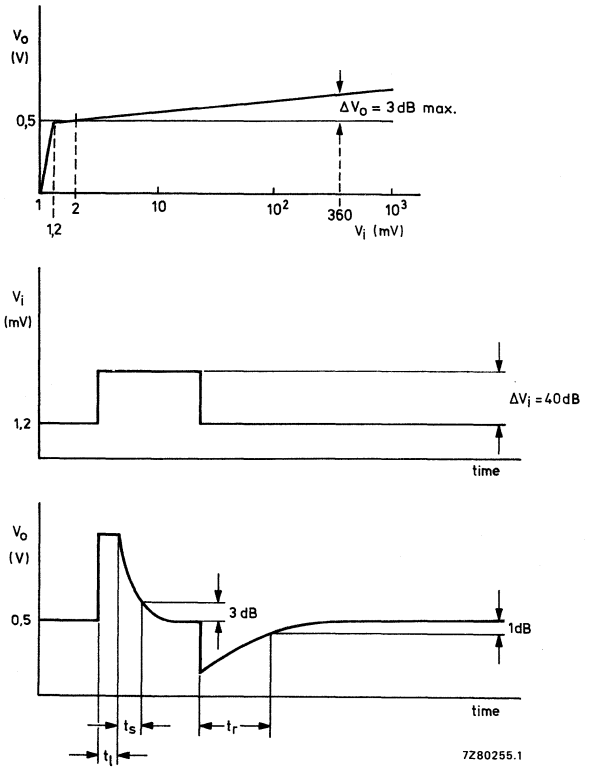


Fig. 3 Typical A.L.C. curve with R_S = 10 kΩ.

* At ΔV_i = 40 dB with respect to V_i = 1,2 mV.

** The A.L.C. tracking in stereo has a typical spread of 1 dB if pins 6 of both ICs are connected to the same RC network.

▲ Without a shunt resistor across A.L.C.
With 1 MΩ or 2,2 MΩ across A.L.C. recovery time becomes 22 or 50 seconds.

12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Output power at d_{tot} = 10% (with bootstrap)				
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10	W
		typ.	12	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5	W
Output power at d_{tot} = 10% (without bootstrap)				
V_P = 14,4 V; R_L = 4 Ω	P_o	>	4,5	W
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	typ.	40	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	40	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	30	mA
Stand-by current	I_{sb}	<	1	mA
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

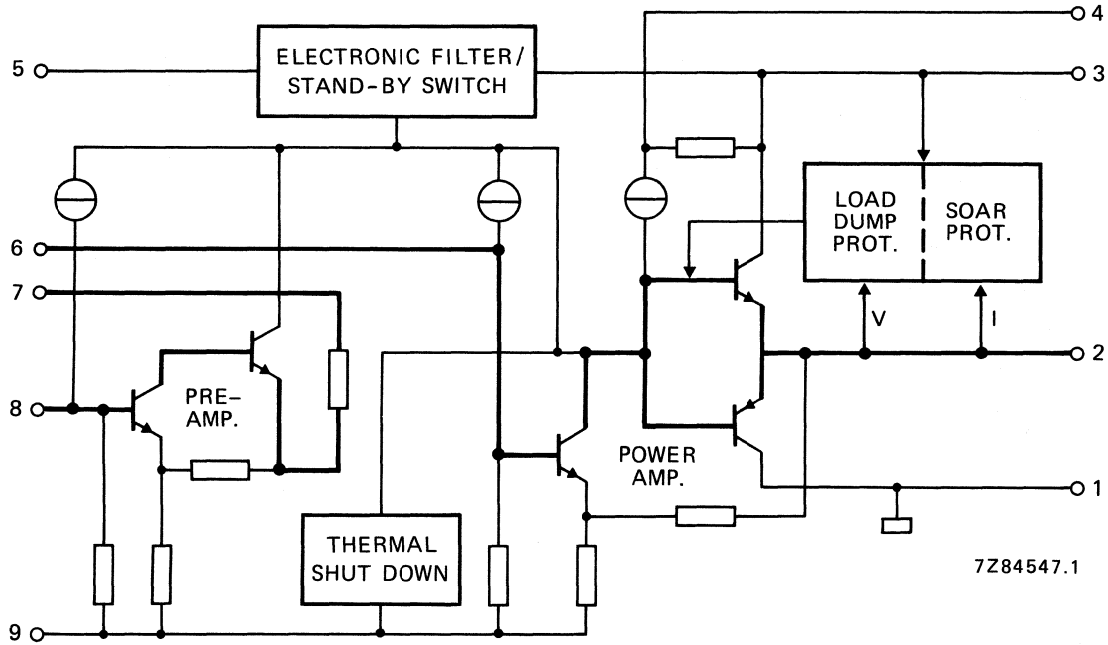


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; load dump	V_P	max.	45 V
Non-repetitive peak output current	I_{OSM}	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100 hours

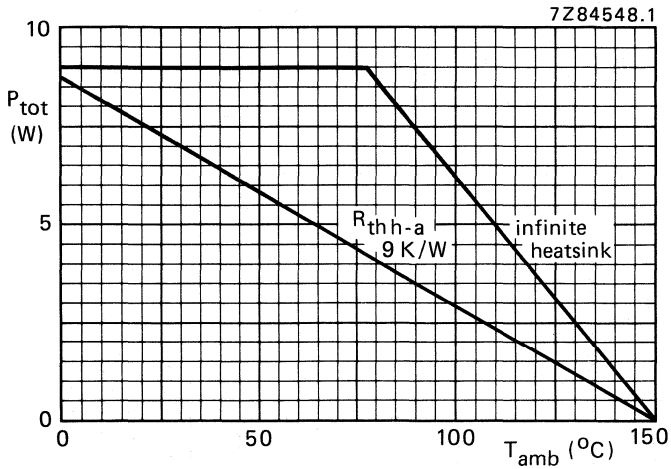


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{5,2} = 17,3\ K/W$$

Since $R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} = 8$ K/W, $R_{th\ h\text{-}a} = 17,3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current			
at V_P = 14,4 V	I_{tot}	typ.	30 mA
at V_P = 18 V	I_{tot}	typ.	40 mA

A.C. CHARACTERISTICS

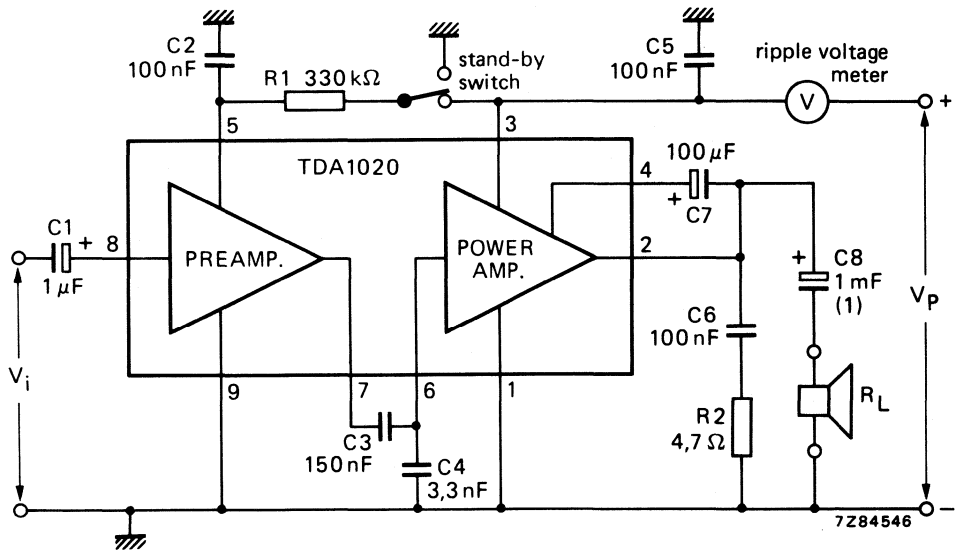
T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

Output power at d_{tot} = 10%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5 W
Output power at d_{tot} = 1%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,5 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3 W
Output voltage (r.m.s. value)			
R_L = 1 kΩ; d_{tot} = 0,5%	$V_{o(rms)}$	typ.	5 V
Output power at d_{tot} = 10%; without bootstrap	P_o	>	4,5 W
Voltage gain			
preamplifier (note 2)	G_{v1}	typ.	17,7 dB
			16,7 to 18,7 dB
power amplifier	G_{v2}	typ.	29,5 dB
			28,5 to 30,5 dB
total amplifier	$G_{v\,tot}$	typ.	47 dB
			46,2 to 48,2 dB
Input impedance			
preamplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
power amplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
Output impedance			
preamplifier	$\|Z_o\|$	typ.	2,0 kΩ
			1,4 to 2,6 kΩ
power amplifier	$\|Z_o\|$	typ.	50 mΩ
Output voltage (r.m.s. value) at d_{tot} = 1%			
preamplifier (note 2)	$V_{o(rms)}$	>	1 V
		typ.	1,5 V
Frequency response	B		50 Hz to 25 kHz
Noise output voltage (r.m.s. value; note 3)			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3 mV
		<	0,5 mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,5 mV
		<	1,0 mV

Ripple rejection (note 4)			
at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	>	48 dB
		typ.	54 dB
Bootstrap current at onset of clipping (pin 4)			
R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

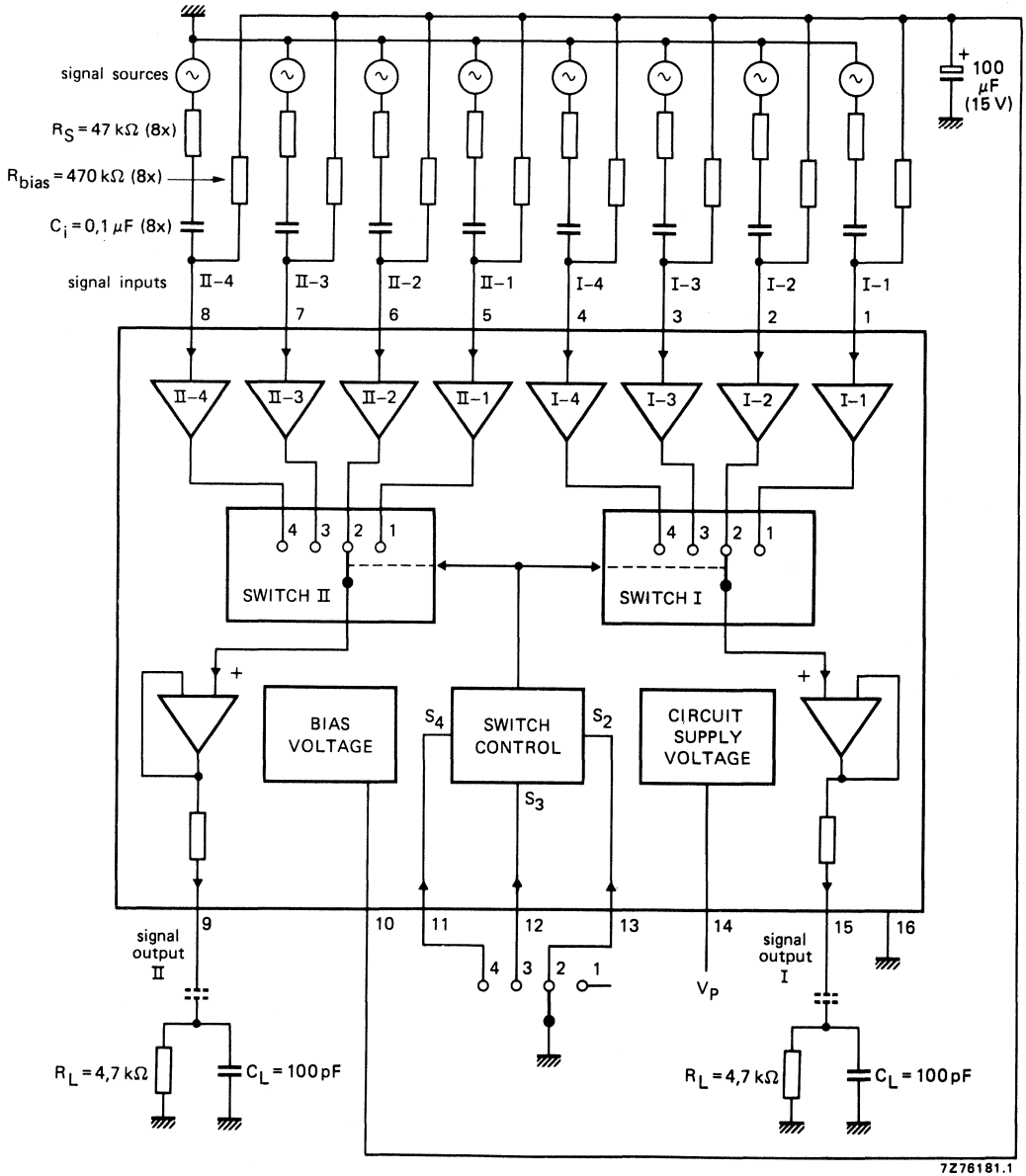


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_g = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage R_S = 0; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

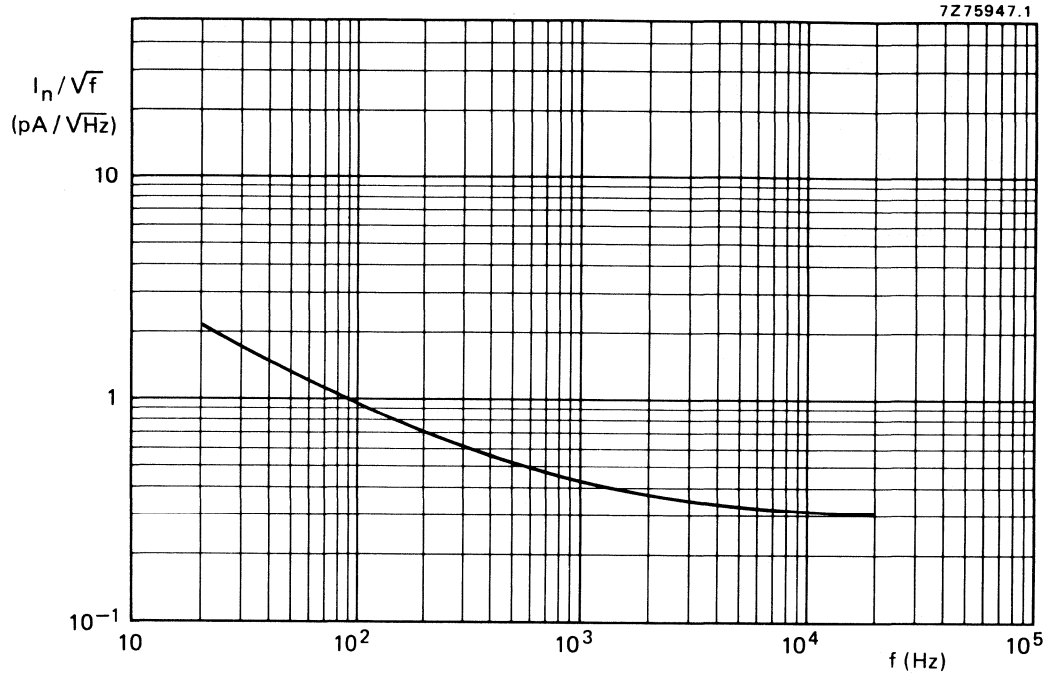


Fig. 2 Equivalent input noise current.

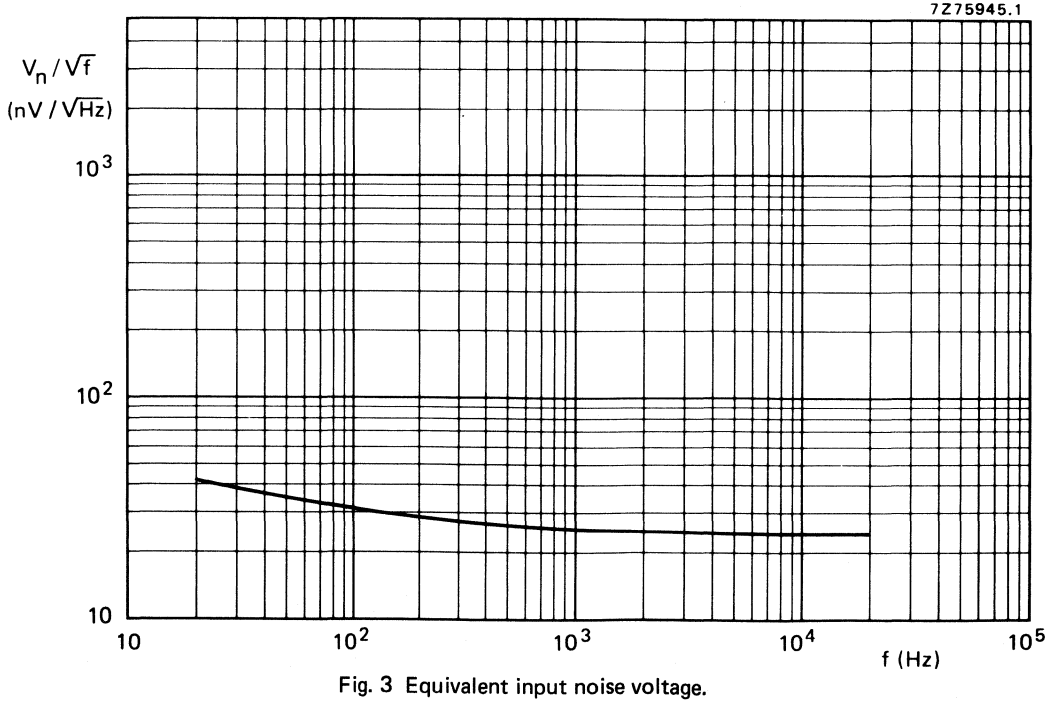


Fig. 3 Equivalent input noise voltage.

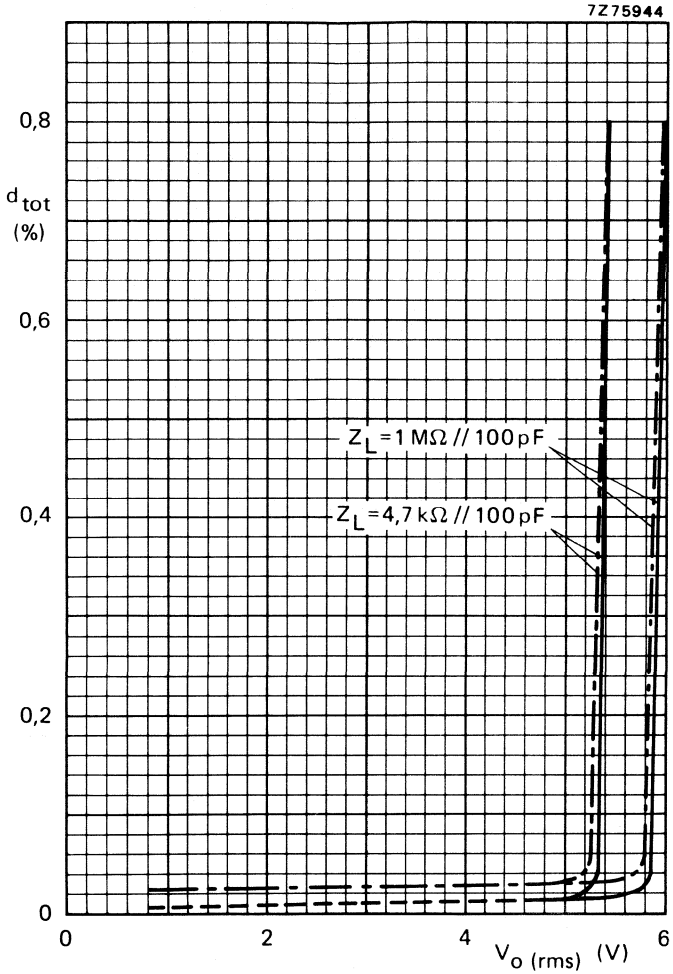


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

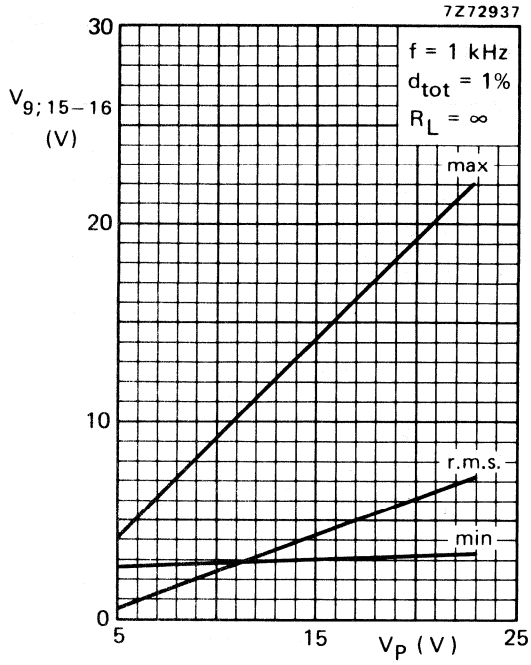


Fig. 5 Output voltage as a function of supply voltage.

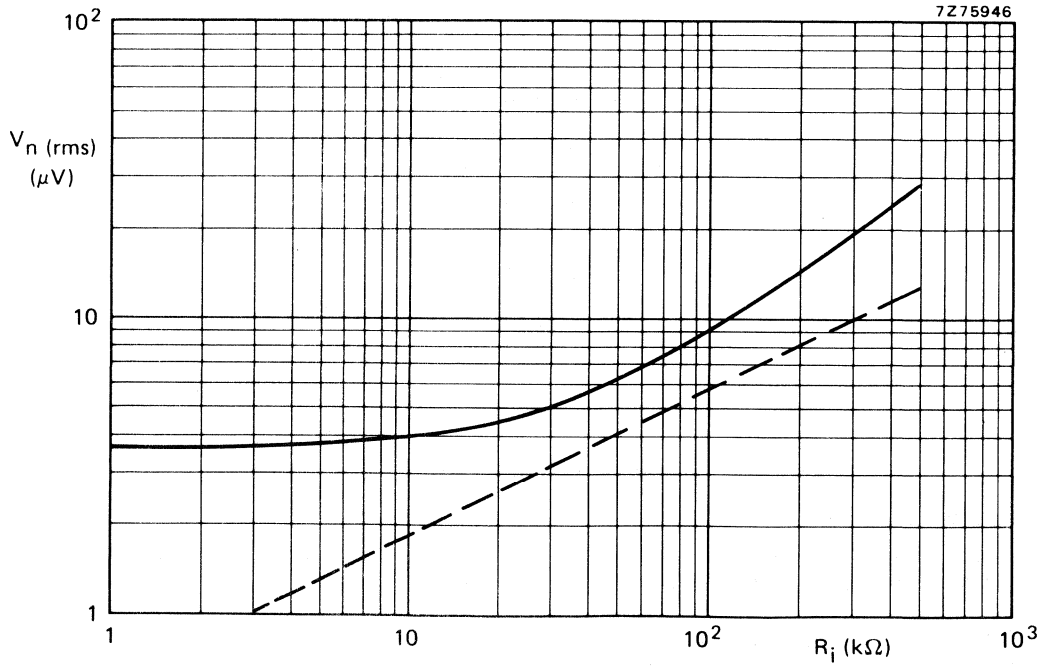


Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

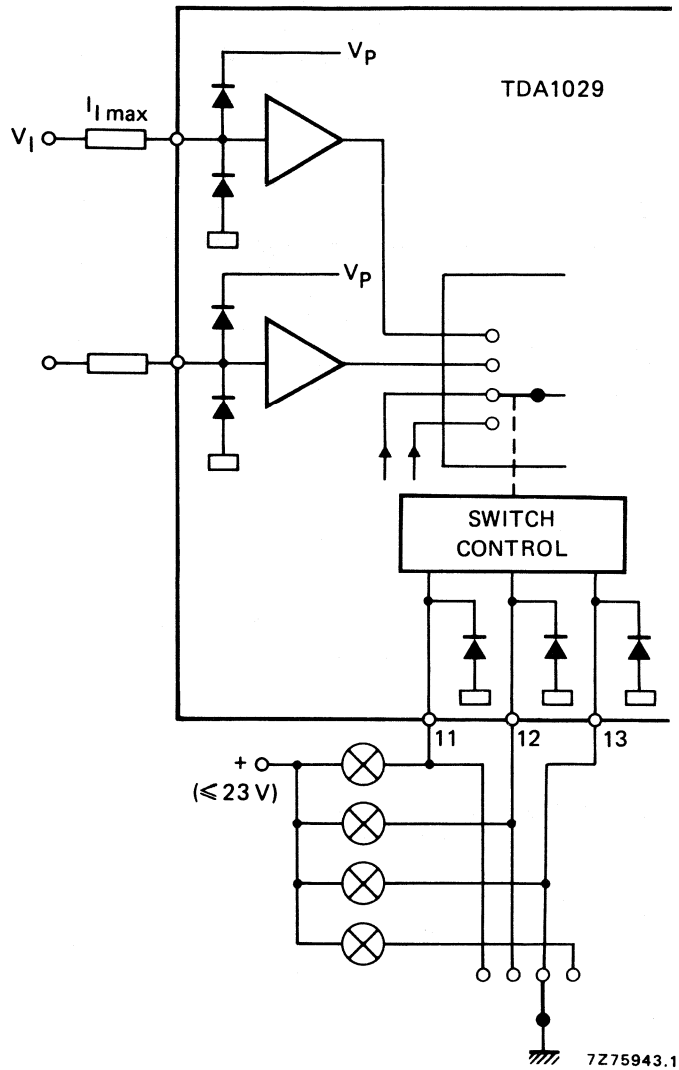


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

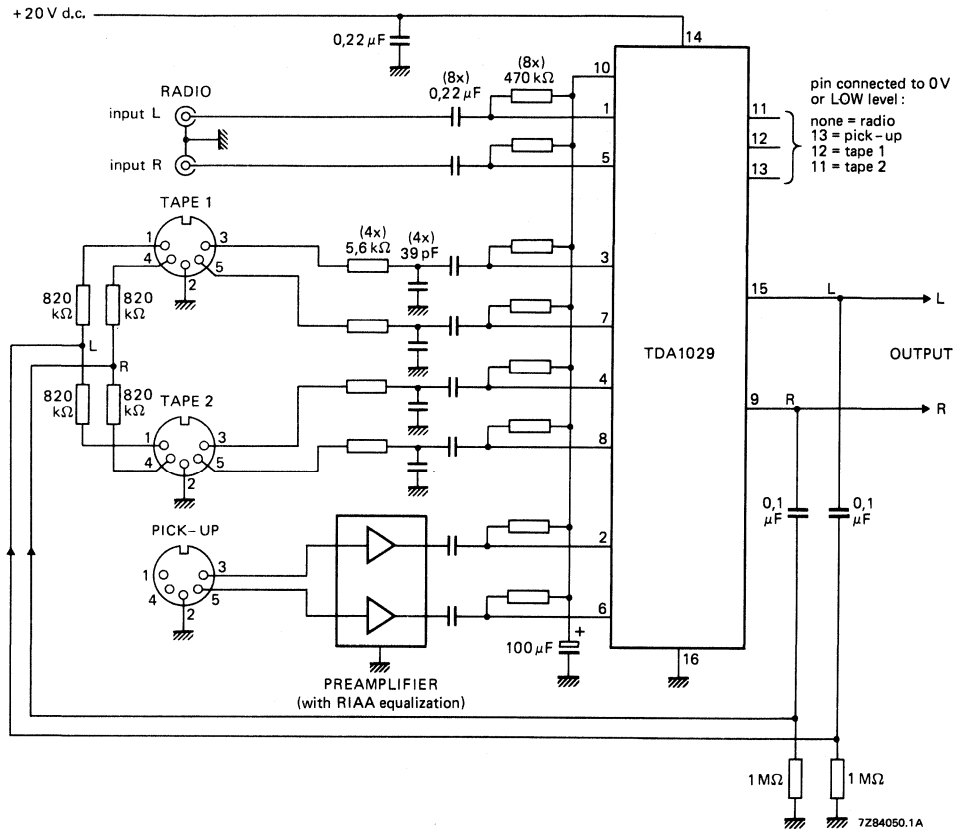


Fig. 8 TDA1029 connected as a four input stereo source selector.

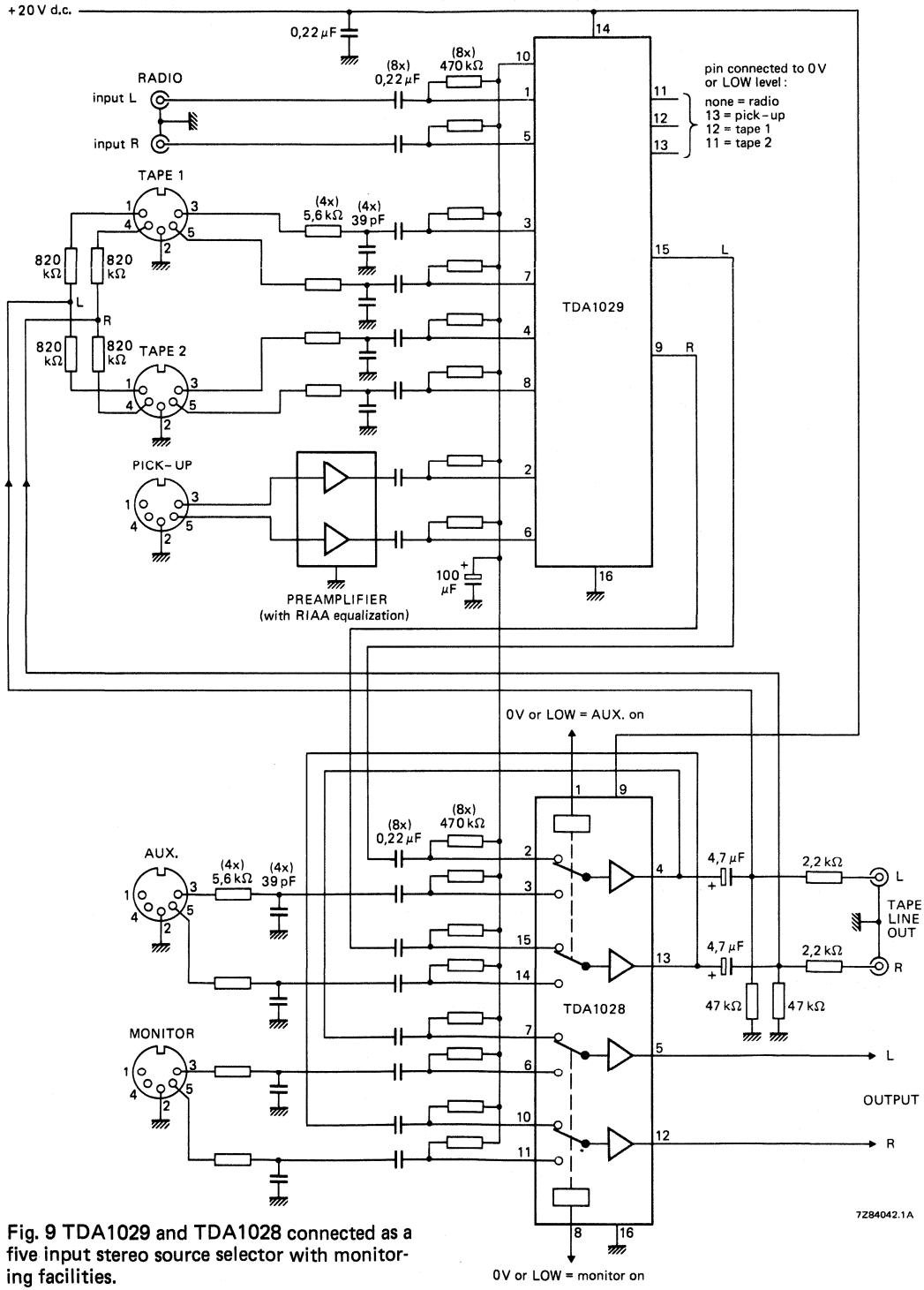


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

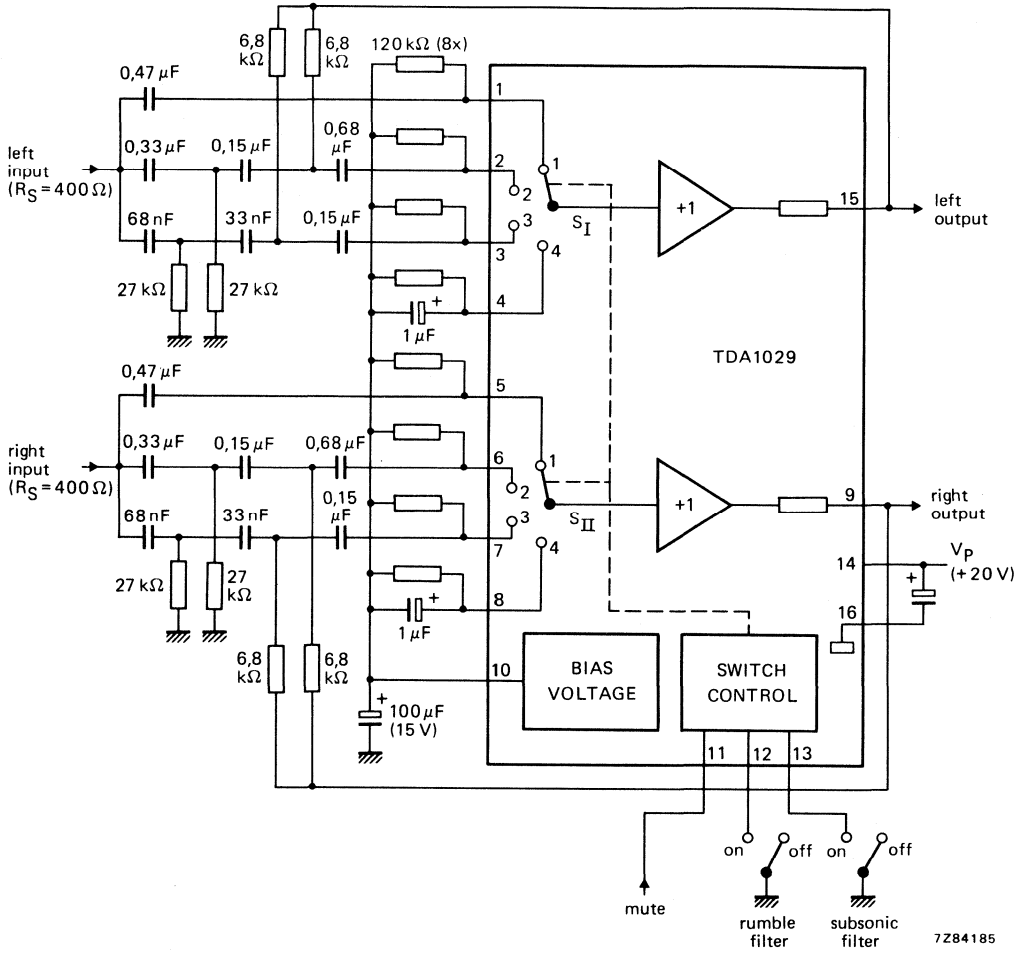


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

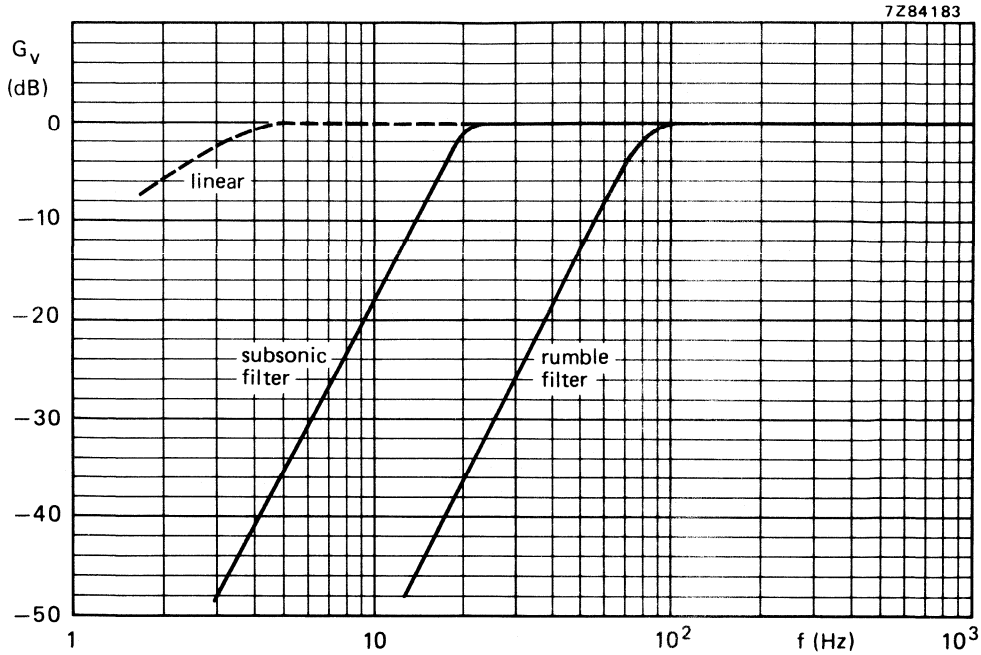


Fig. 11 Frequency response curves for the circuit of Fig. 10.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

Features

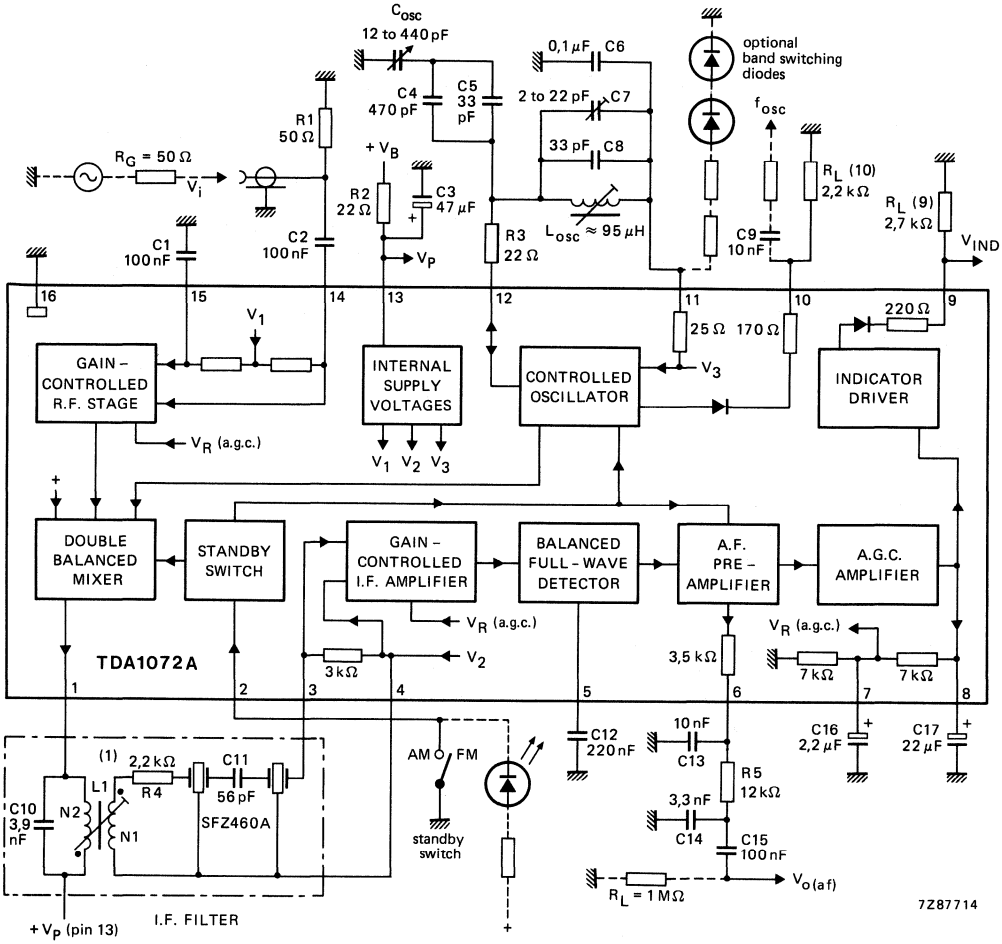
- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

QUICK REFERENCE DATA

Supply voltage range	V_P	7,5 to 18	V
Supply current range	I_P	15 to 30	mA
R.F. input voltage for S + N/N = 6 dB at m = 30%	V_i	typ. 1,5	μV
R.F. input voltage for 3% total harmonic distortion (THD) at m = 80%	V_i	typ. 500	mV
A.F. output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30% and f_m = 400 Hz	$V_{o(af)}$	typ. 310	mV
A.G.C. range: change of V_i for 1 dB change of $V_{o(af)}$		typ. 86	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	V_{IND}	typ. 2,8	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at $R_{3\text{-}4}$ = 3 kΩ; Z_I = 4,8 kΩ.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage	$V_P = V_{13-16}$	max.	20	V
Total power dissipation	P_{tot}	max.	875	mW
Input voltage	$\|V_{14-15}\|$	max.	12	V
	$-V_{14-16}$, $-V_{15-16}$	max.	0,6	V
	V_{14-16}, V_{15-16}	max.	V_P	V
Input current	$\|I_{14}\|$, $\|I_{15}\|$	max.	200	mA
Operating ambient temperature range	T_{amb}	−40 to	+80	°C
Storage temperature range	T_{stg}	−55 to	+150	°C
Junction temperature	T_j	max.	+125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	80	K/W

DEVICE CHARACTERISTICS

$V_P = V_{13-16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_{13-16}$	7,5	8,5	18	V
Supply current	$I_P = I_{13}$	15	23	30	mA
R.F. stage and mixer					
Input voltage (d.c. value)	V_{14-16}, V_{15-16}	–	$V_P/2$	–	V
R.F. input impedance at $V_i < 300\ \mu V$	R_{14-16}, R_{15-16}	–	5,5	–	kΩ
	C_{14-16}, C_{15-16}	–	25	–	pF
R.F. input impedance at $V_i > 10$ mV	R_{14-16}, R_{15-16}	–	8	–	kΩ
	C_{14-16}, C_{15-16}	–	22	–	pF
I.F. output impedance	R_{1-16}	500	–	–	kΩ
	C_{1-16}	–	6	–	pF
Conversion transconductance before start of a.g.c.	I_1/V_i	–	6,5	–	mA/V
Maximum i.f. output voltage, inductive coupling to pin 1	$V_{1-13(p-p)}$	–	5	–	V
D.C. value of output current (pin 1) at $V_i = 0$ V	I_1	–	1,2	–	mA
A.G.C. range of input stage		–	30	–	dB
R.F. signal handling capability: input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,6	–	60	MHz
Oscillator amplitude (pins 11 to 12)	$V_{11\text{-}12}$	–	130	150	mV
External load impedance	$R_{12\text{-}11(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation	$R_{12\text{-}11(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log[V_{13\text{-}16}/V_{11\text{-}16}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE})	$V_{11\text{-}16}$	–	4,2	–	V
D.C. output current (for switching diodes)	$-I_{11}$	0	–	20	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)	$\Delta V_{11\text{-}16}$	–	0,5	–	V
Buffered oscillator output					
D.C. output voltage	$V_{10\text{-}16}$	–	0,7	–	V
Output signal amplitude	$V_{10\text{-}16(p\text{-}p)}$	–	320	–	mV
Output impedance	R_{10}	–	170	–	Ω
Output current	$-I_{10(peak)}$	–	–	3	mA
I.F., a.g.c. and a.f. stages					
D.C. input voltage	$V_{3\text{-}16}$, $V_{4\text{-}16}$	–	2,0	–	V
I.F. input impedance	$R_{3\text{-}4}$	2,4	3	3,9	kΩ
	$C_{3\text{-}4}$	–	7	–	pF
I.F. input voltage for THD = 3% at m = 80%	$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of a.g.c.	$V_{3\text{-}4}/V_{6\text{-}16}$	–	68	–	dB
A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV	$\Delta V_{3\text{-}4}$	–	55	–	dB
A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV	$V_{o(af)}$	–	310	–	mV
A.F. output impedance (pin 6)	$\lvert Z_o \rvert$	–	3,5	–	kΩ
Indicator driver					
Output voltage at V_i = 0 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	–	20	150	mV
Output voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	2,5	2,8	3,1	V
Load resistance	$R_{L(9)}$	1,5	–	–	kΩ

DEVICE CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Standby switch					
Switching threshold at V_P = 7,5 to 18 V; T_{amb} = −40 to + 80 °C					
on-voltage	$V_{2\text{-}16}$	0	–	2,0	V
off-voltage	$V_{2\text{-}16}$	3,5	–	20	V
on-current at $V_{2\text{-}16}$ = 0 V	$-I_2$	–	–	200	μA
off-current at $V_{2\text{-}16}$ = 20 V	$\|I_2\|$	–	–	10	μA

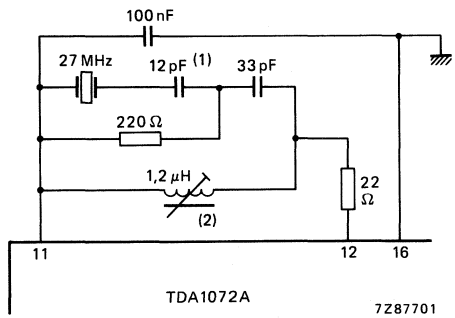
OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity					
R.F. input required for S + N/N = 6 dB	V_i	–	1,5	–	μV
R.F. input required for S + N/N = 26 dB	V_i	–	15	–	μV
R.F. input required for S + N/N = 46 dB	V_i	–	150	–	μV
R.F. input at start of a.g.c.	V_i	–	30	–	μV
R.F. large signal handling					
R.F. input at THD = 3%; m = 80%	V_i	–	500	–	mV
R.F. input at THD = 3%; m = 30%	V_i	–	700	–	mV
R.F. input at THD = 10%; m = 30%	V_i	–	900	–	mV
A.G.C. range					
Change of V_i for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
A.F. output voltage at V_i = 4 μV; m = 80%	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at V_i = 1 mV	$V_{o(af)}$	240	310	390	mV
THD at V_i = 1 mV; m = 80%	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV; m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio at V_i = 100 mV	(S + N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_P/V_{o(af)}]$)	RR	–	38	–	dB

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of i.f. whistles at V_i = 15 μV; m = 0% related to a.f. signal of m = 30%					
at $f_i \approx 2 \times f_{if}$	α_{2if}	–	37	–	dB
at $f_i \approx 3 \times f_{if}$	α_{3if}	–	44	–	dB
I.F. suppression at r.f. input					
for symmetrical input	α_{if}	–	40	–	dB
for asymmetrical input	α_{if}	–	40	–	dB
Residual oscillator signal at mixer output					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

APPLICATION INFORMATION (continued)

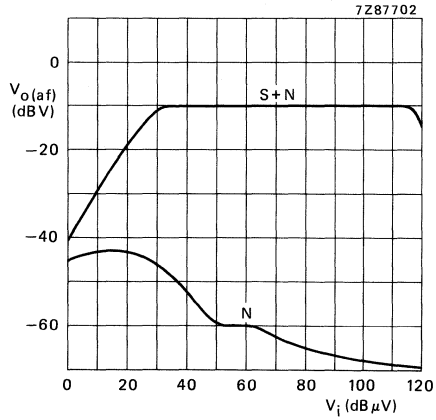


Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

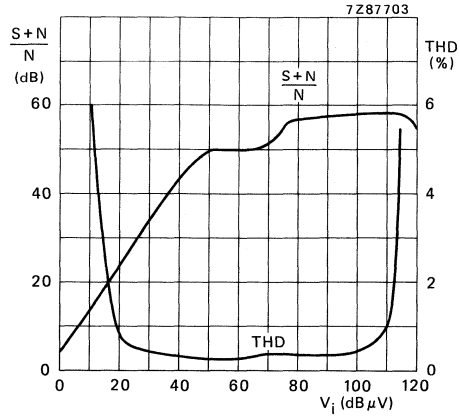


Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

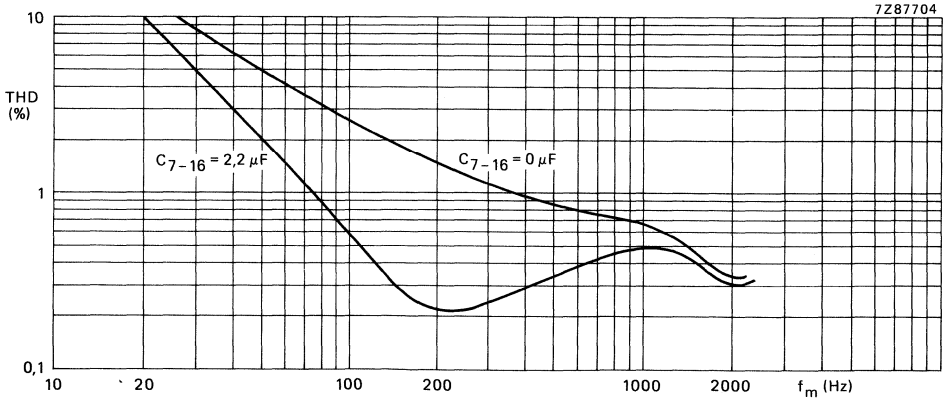


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2,2 μF.

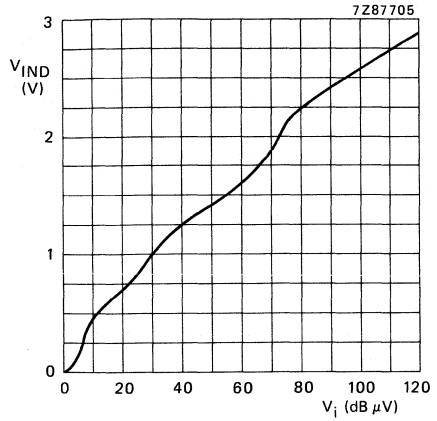


Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

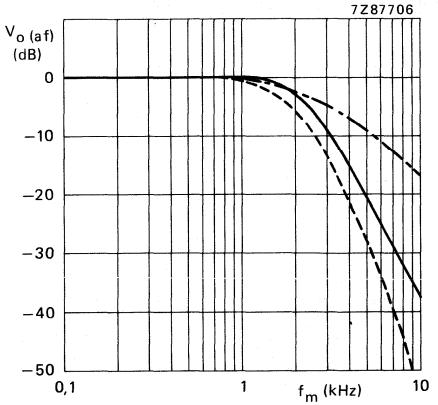


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:
——— with i.f. filter;
—·—·—·— with a.f. filter;
– – – – – – with i.f. and a.f. filters.

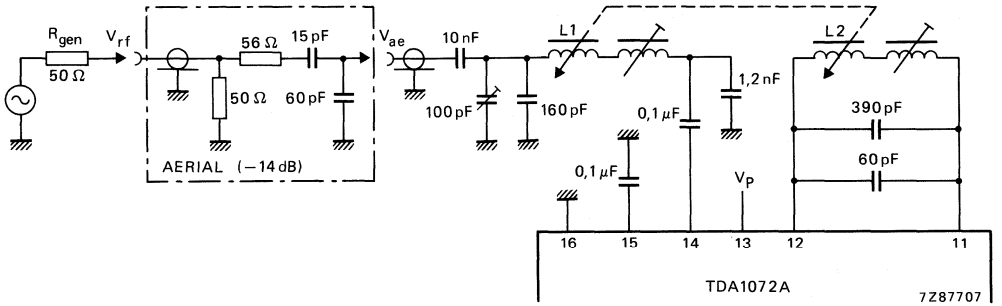


Fig. 8 Car radio application with inductive tuning.

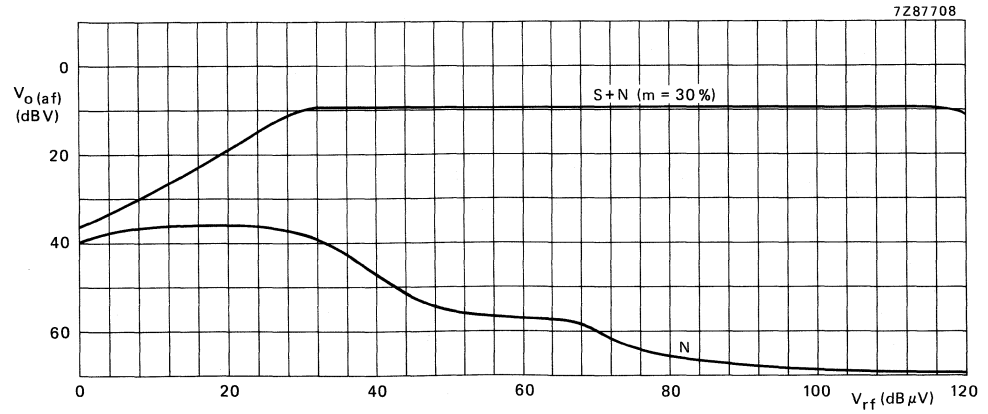


Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

APPLICATION INFORMATION (continued)

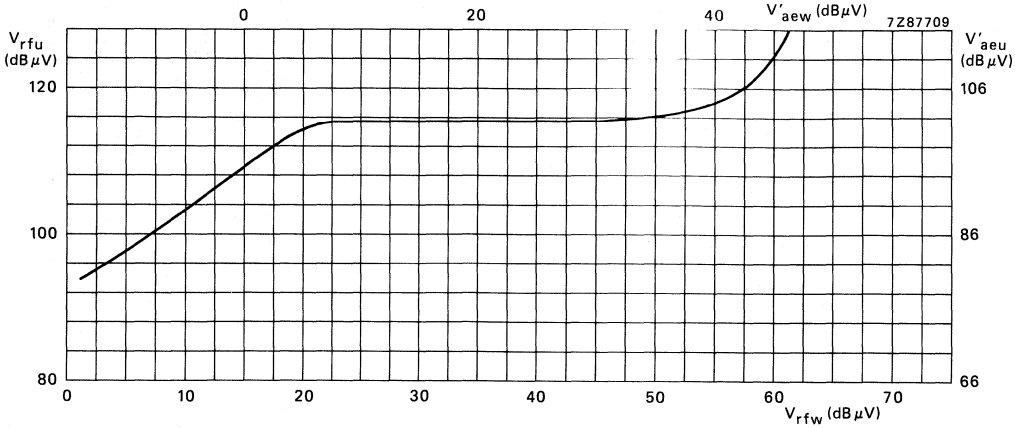


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

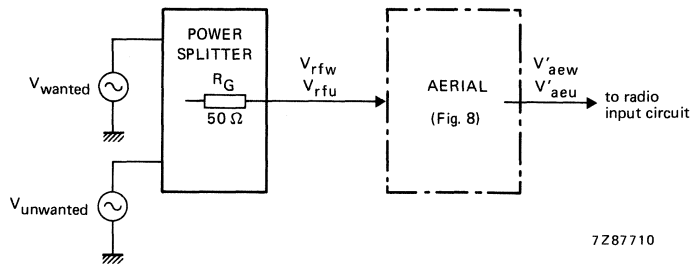


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

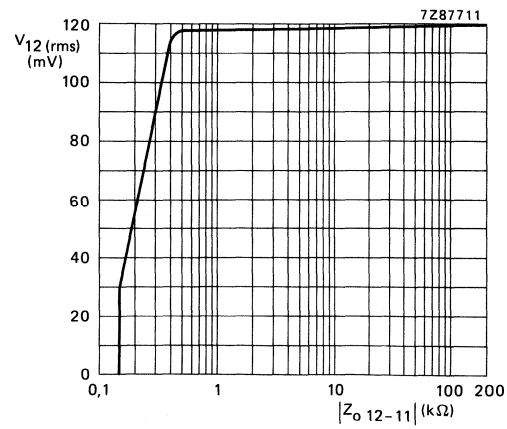


Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

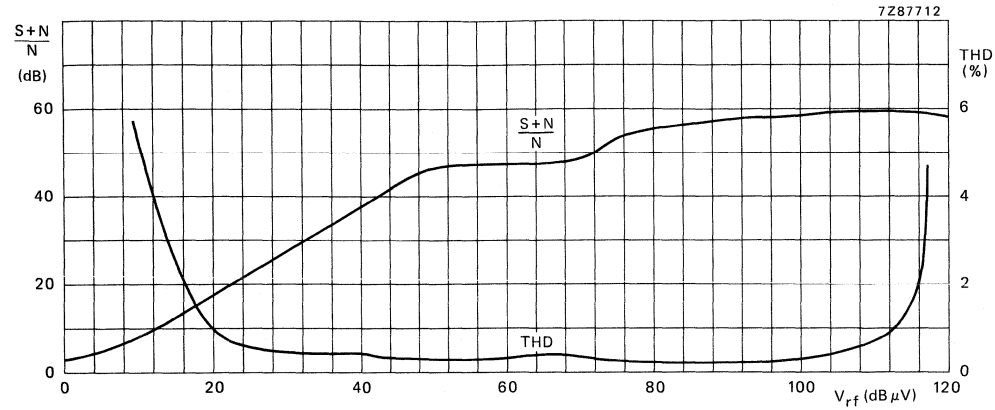


Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

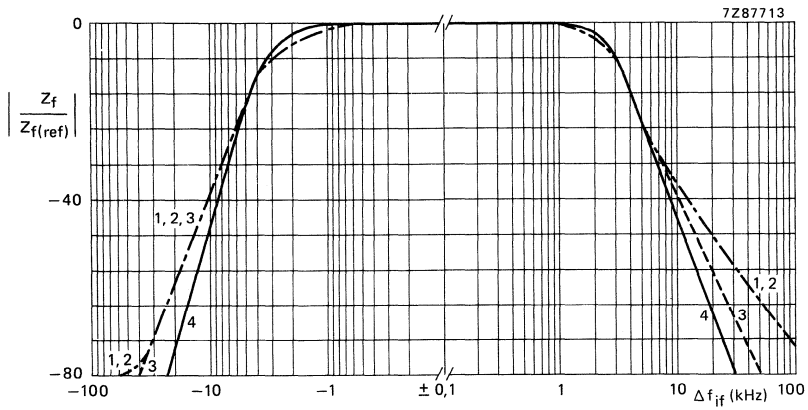


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

APPLICATION INFORMATION (continued)

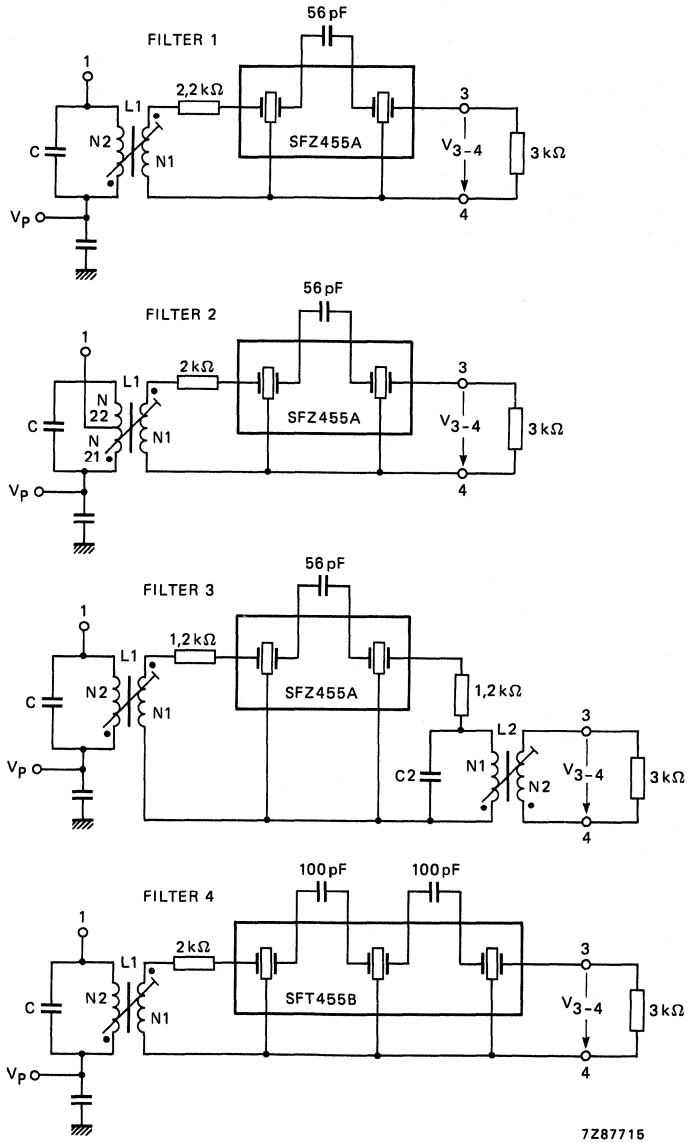
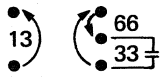
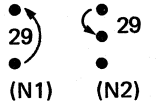


Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

Table 1 Data for I.F. filters shown in Fig. 15. Criterium for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

APPLICATION INFORMATION (continued)

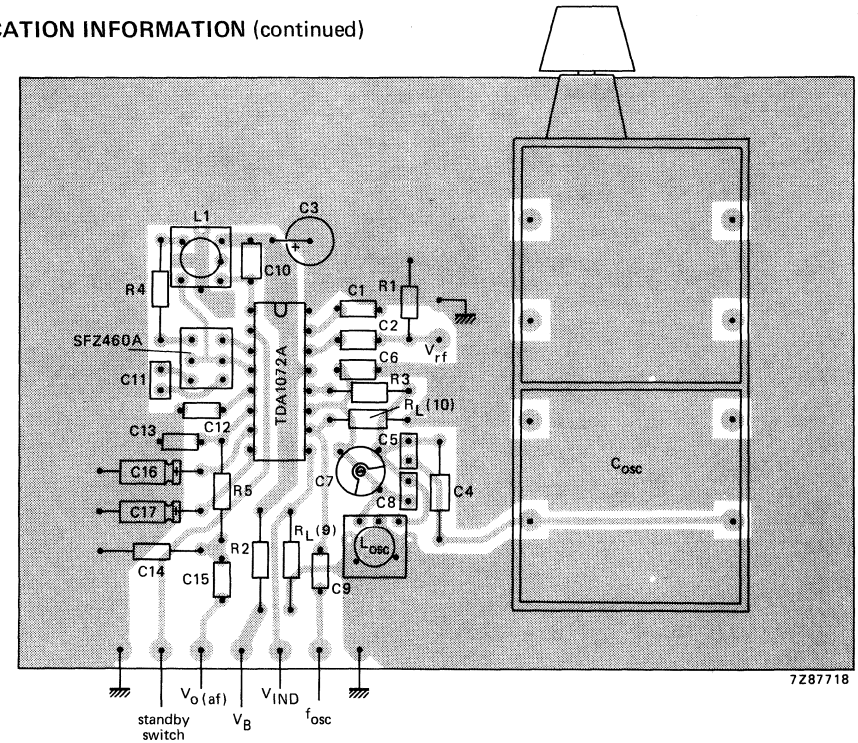


Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

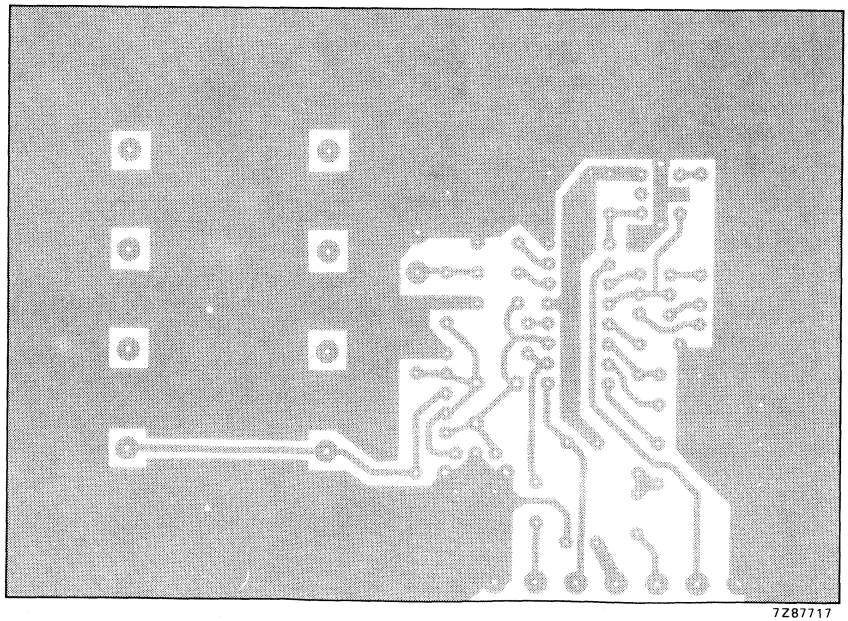
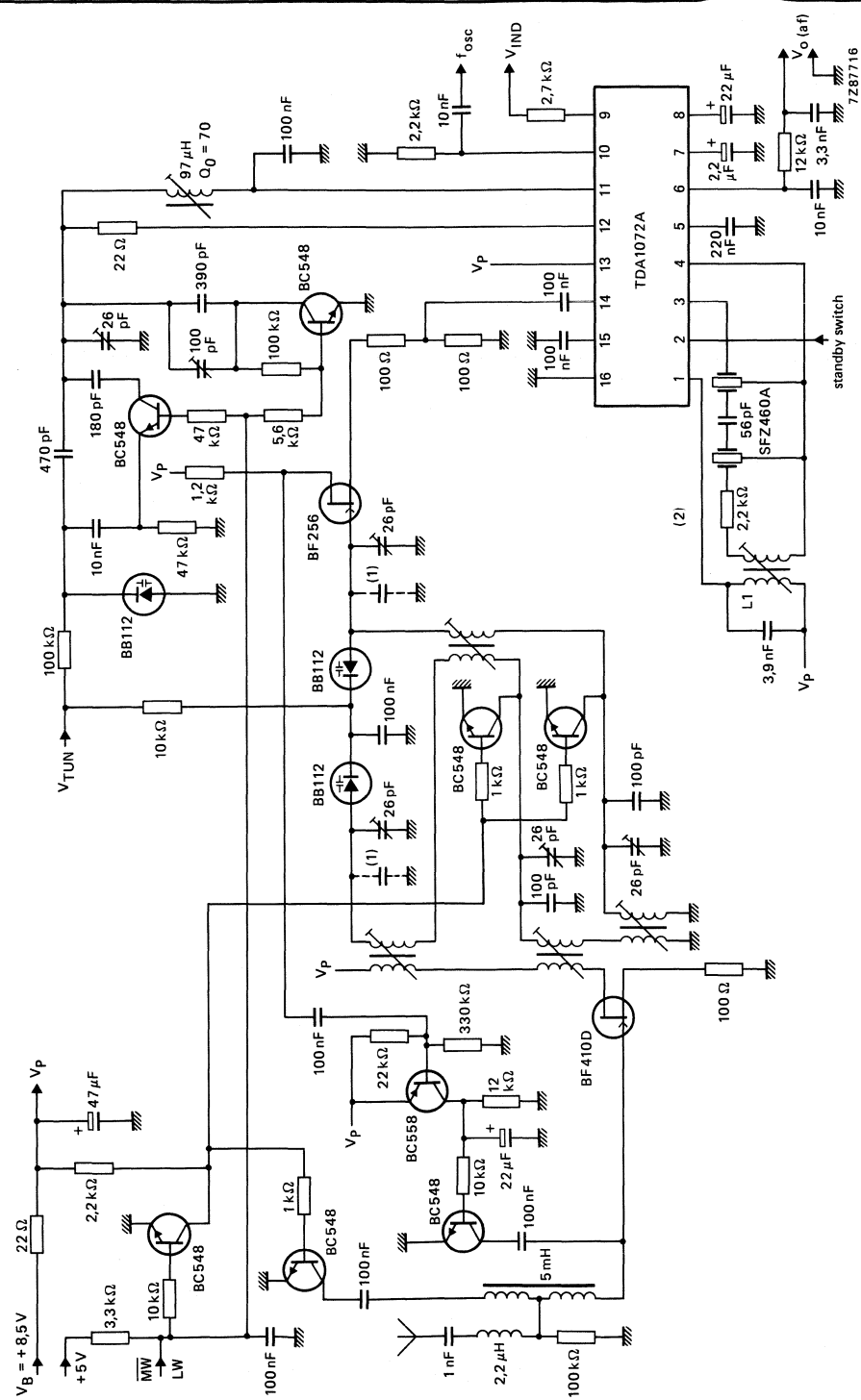


Fig. 17 Printed-circuit board showing track side.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072AT integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV. RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

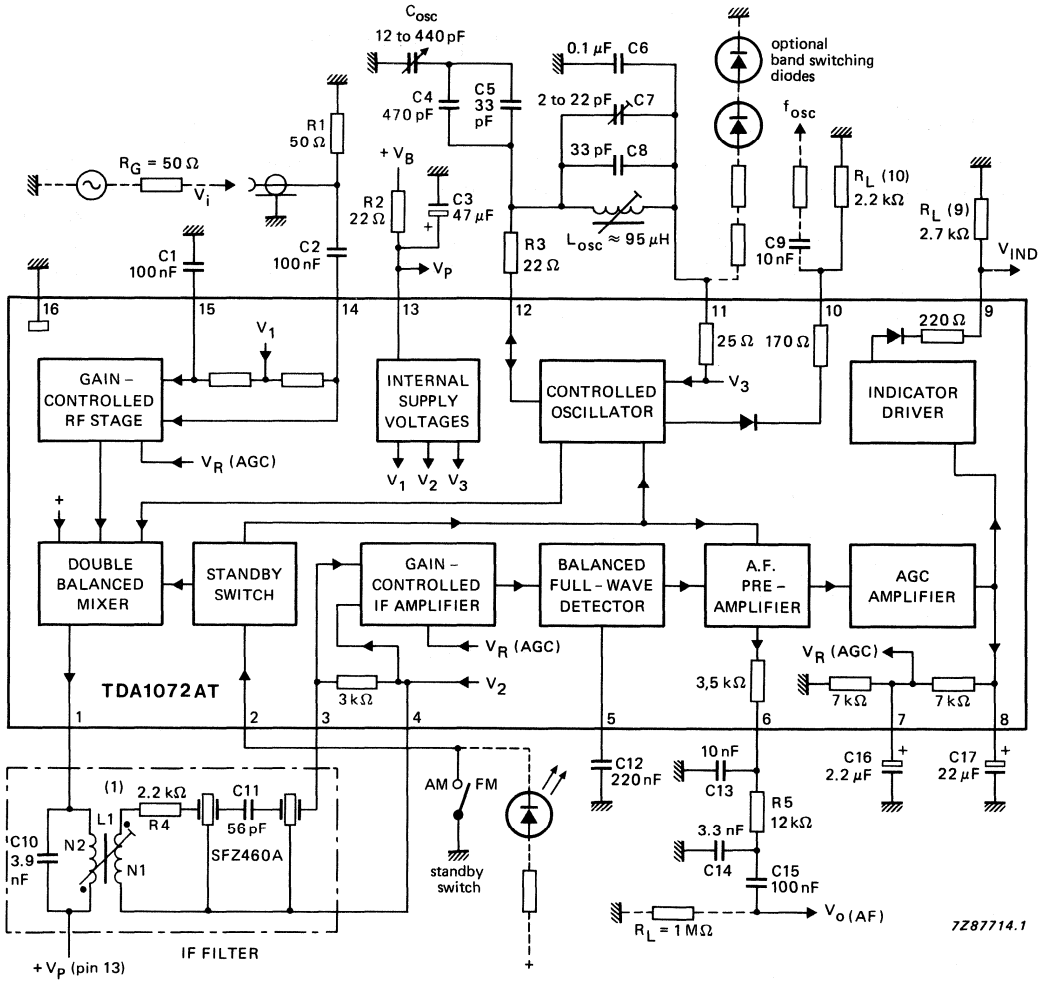
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	–	10	V
Supply current range		I_P	15	–	26	mA
RF input voltage for S+N/N = 6 dB at m = 30%		V_I	–	1.5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%		V_I	–	500	–	mV
AF output voltage with V_I = 2 mV; f_I = 1 MHz; m = 30% and f_m = 400 Hz		$V_{O(AF)}$	–	310	–	mV
AGC range: change of V_I for 1 dB change of $V_{O(AF)}$			–	86	–	dB
Field strength indicator voltage at V_I = 500 mV; $R_{L(9)}$ = 2.7 kΩ		V_{IND}	–	2.8	–	V

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1: N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_1 = 4.8 kΩ.

Fig.1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is also improved. Low noise working is achieved in the differential amplifier by using transistors with a low base resistance.

A double balanced mixer provides the IF output to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. The residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output. The amplifier output stage uses an emitter follower with a series resistor which, together with an external capacitor, provides the required low-pass filtering for AF signals.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives a fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter. The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If field strength information is not needed, $R_{L(9)}$ can be omitted.

FUNCTIONAL DESCRIPTION (continued)

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and demodulator are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	$V_P = V_{13-16}$	V_{13}	–	12	V
Input voltage					
pins 14-15		V_{14-15}	–	10	V
pins 14-16		V_{14-16}	–	V_P	V
pins 15-16		V_{15-16}	–	V_P	V
pins 14-16		V_{14-16}	–	–0.6	V
pins 15-16		V_{15-16}	–	–0.6	V
Input current (pins 14 and 15)		I_{14-15}	–	200	mA
Total power dissipation*		P_{tot}	–	300	mW
Operating ambient temperature range		T_{amb}	–40	+ 80	°C
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	300	K/W
		160	K/W*

* Mounted on epoxiprint

CHARACTERISTICS

$V_P = V_{13-16} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig.1; all measurements are with respect to ground (pin 16); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_{13}	7.5	8.5	10	V
Supply current (pin 13)		I_{13}	15	23	27	mA
RF stage and mixer						
Input voltage (DC value)		V_{14-15}	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$		R_{14-15}	–	5.5	–	kΩ
		C_{14-15}	–	25	–	pF
RF input impedance at $V_I > 10$ mV		R_{14-15}	–	8	–	kΩ
		C_{14-15}	–	22	–	pF
IF output impedance		R_1	500	0	0	kΩ
		C_1	–	6	–	pF
Conversion transconductance before start of AGC		I_1/V_I	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1, (peak-to-peak value)		$V_{1(p-p)}$	–	5	–	V
DC value of output current (pin 1) at $V_I = 0$ V		I_1	–	1.2	–	mA
AGC range of input stage			–	30	–	dB
RF signal handling capability: input voltage for THD = 3% at m = 80% (RMS value)		$V_{I(rms)}$	–	500	–	mV
Oscillator						
Frequency range		Δf	0.6	–	60	MHz
Oscillator amplitude (pins 11 to 12) (peak-to-peak value)		$V_{11-12(p-p)}$	–	130	150	mV
External load impedance		$R_{11-12(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation		$R_{11-12(ext)}$	–	–	60	Ω

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection at V_P = 100 mV (RMS value); f_p = 100 Hz ($RR = 20 \log [V_{13}/V_{11}]$)						
Source voltage for switching diodes (6 x V_{BE})		V_{11}	–	4.2	–	V
DC output current (for switching diodes)	$V_P = V_{13} \leqslant 9$ V	I_{11}	0	–	5	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)		ΔV_{11}	–	0.5	–	V
Buffered oscillator output						
DC output voltage		V_{10}	–	0.7	–	V
Output signal amplitude (peak-to-peak value)		$V_{10(p\text{-}p)}$	–	320	–	mV
Output impedance		R_{10}	–	170	–	Ω
Output current		$I_{10(peak)}$	–	–	–3	mA
IF, AGC and AF stages						
DC input voltage		$V_{3\text{-}4}$	–	2	–	V
IF input impedance		$R_{3\text{-}4}$	2.4	3.0	3.9	kΩ
		$C_{3\text{-}4}$	–	7	–	pF
IF input voltage for THD = 3% at m = 80%		$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of AGC		$V_{3\text{-}4}/V_6$	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{O(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV		$\Delta V_{3\text{-}4}$	–	55	–	dB
AF output voltage at $V_{3\text{-}4(IF)}$ = 50 μV		$V_{O(AF)}$	–	130	–	mV
AF output voltage at $V_{3\text{-}4(IF)}$ = 1 mV		$V_{O(AF)}$	–	310	–	mV
AF output impedance (pin 6)		$\lvert Z_O \rvert$	–	3.5	–	kΩ

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator driver						
Output voltage at V_I = 0 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	–	20	150	mV
Output voltage at V_I = 500 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	2.5	2.8	3.1	V
Load resistance		$R_{L(9)}$	2.7	–	–	kΩ
Standby switch						
Switching threshold at V_P = 7.5 to 18 V; T_{amb} = −40 to + 80 °C						
ON-voltage		V_2	0	–	2	V
OFF-voltage		V_2	3.5	–	20	V
ON-current	V_2 = 0 V	I_2	–	–	−200	μA
OFF-current	V_2 = 20 V	I_2	–	–	10	μA

OPERATING CHARACTERISTICS

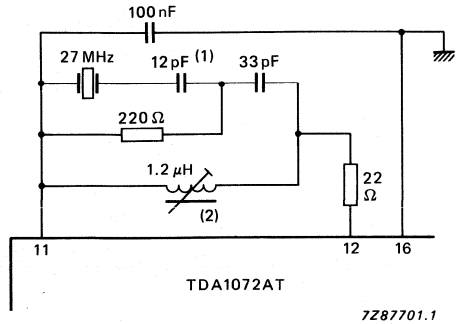
V_P = 8.5 V; f_I = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input required for						
S+N/N = 6 dB		V_I	–	1.5	–	μV
S+N/N = 26 dB		V_I	–	15	–	μV
S+N/N = 46 dB		V_I	–	150	–	μV
RF input at start of AGC		V_I	–	30	–	μV
RF large signal handling						
RF input at						
THD = 3%; m = 80%		V_I	–	500	–	mV
THD = 3%; m = 30%		V_I	–	700	–	mV
THD = 10%; m = 30%		V_I	–	900	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AGC range						
Change of V_I for						
1 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	86	–	dB
6 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	91	–	dB
Output signal						
AF output voltage at						
V_I = 4 μV	m = 80%	$V_{O(AF)}$	–	130	–	mV
V_I = 1 mV		$V_{O(AF)}$	240	310	390	mV
Total harmonic distortion at						
V_I = 1 mV	m = 80%	d_{tot}	–	0.5	–	%
V_I = 500 mV	m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio	V_I = 100 mV	S+N/N	–	58	–	dB
Ripple rejection at V_I = 2 mV V_P = 100 mV (RMS value) f_p = 100 Hz ($RR = 20 \log [V_P/V_{O(AF)}]$)		RR	–	38	–	dB
Unwanted signals						
Suppression of IF whistles at V_I = 15 μV; m = 0% related to AF signal of m = 30%						
at $f_I \approx 2 \times f_{IF}$		α_{2IF}	–	37	–	dB
at $f_I \approx 3 \times f_{IF}$		α_{3IF}	–	44	–	dB
IF suppression at RF input						
for symmetrical input		α_{IF}	–	40	–	dB
for asymmetrical input		α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output						
at f_{osc}		$I_{(osc)}$	–	1	–	μA
at 2 x f_{osc}		$I_{(2osc)}$	–	1.1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0.1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o = 80$.

Fig.2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

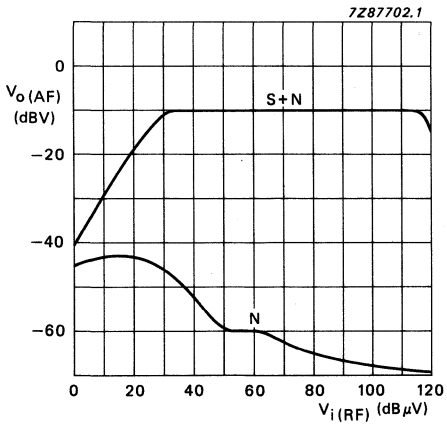


Fig.3 AF output as a function of RF input in the circuit of Fig.1; f_I = 1 MHz; f_m = 400 Hz; m = 30%.

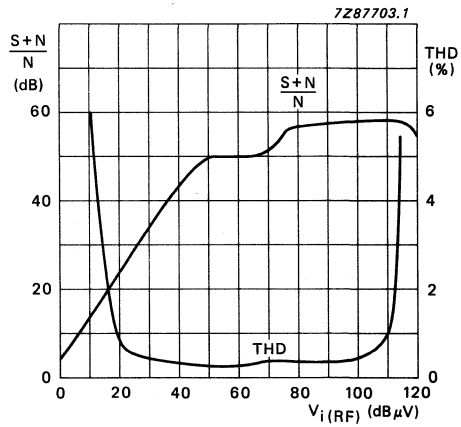


Fig.4 Total harmonic distortion and S+N/N as functions of RF input in the circuit of Fig.1; m = 30% for (S+N)/N curve and m = 80% for THD curve.

APPLICATION INFORMATION (continued)

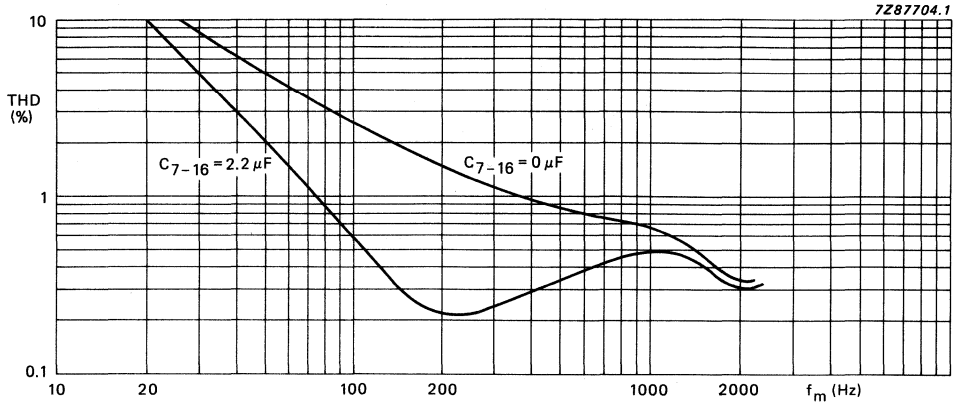


Fig.5 Total harmonic distortion as a function of modulation frequency at V_I = 5 mV; m = 80%; measured in the circuit of Fig.1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2.2 μF.

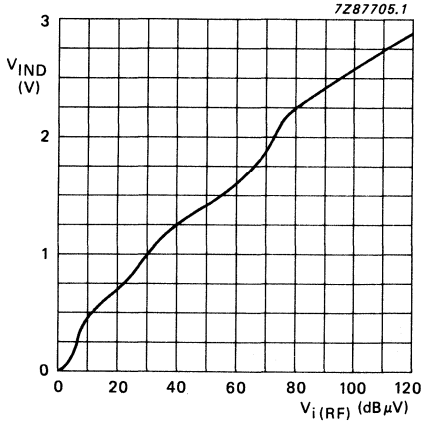
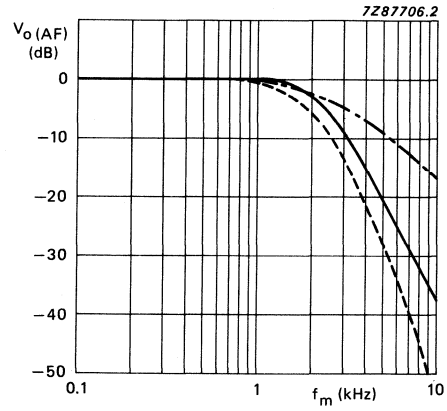


Fig.6 Indicator driver voltage as a function of RF input in the circuit of Fig.1.



—— with IF filter
—·—· with AF filter
------- with IF and AF filter

Fig.7 Typical frequency response curves from Fig.1 showing the effects of filtering.

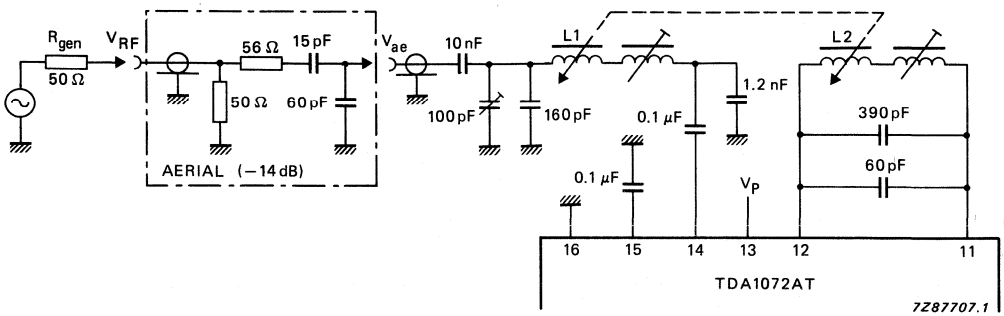


Fig.8 Car radio application with inductive tuning.

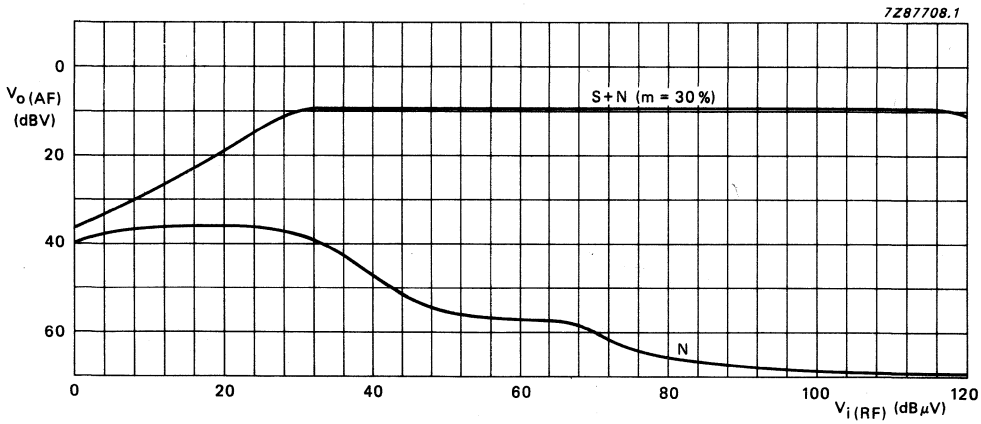


Fig.9 AF output as a function of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

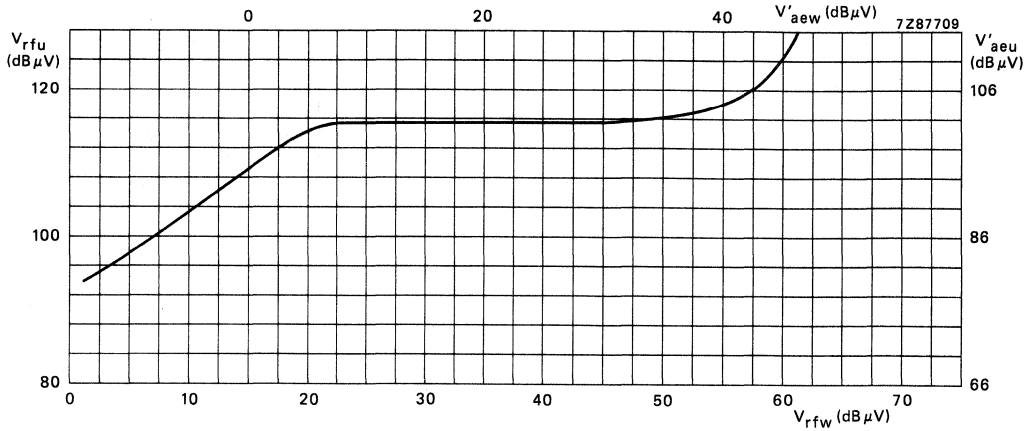


Fig.10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig.8 with the input circuit as shown in Fig.11. Curve is for wanted $V_{O(AF)}$/unwanted $V_{O(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

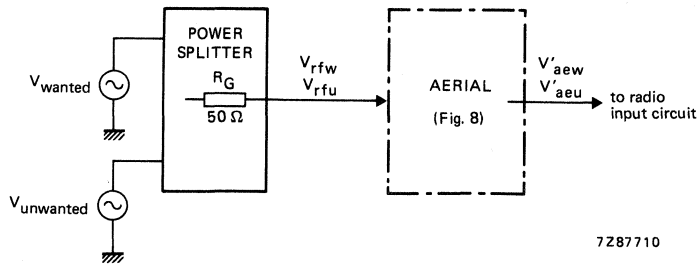


Fig.11 Input circuit to show cross-modulation suppression (see Fig.10).

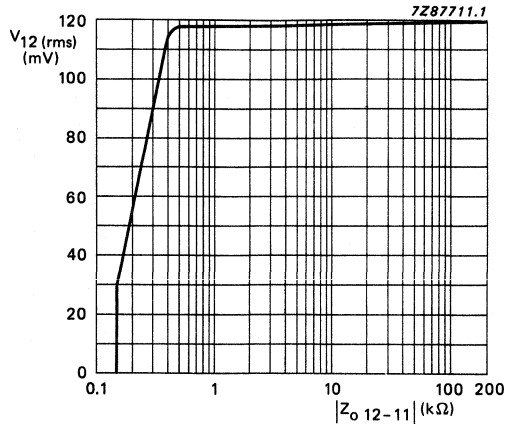


Fig.12 Oscillator amplitude as a function of the impedance at pins 11 and 12 in the circuit of Fig.8.

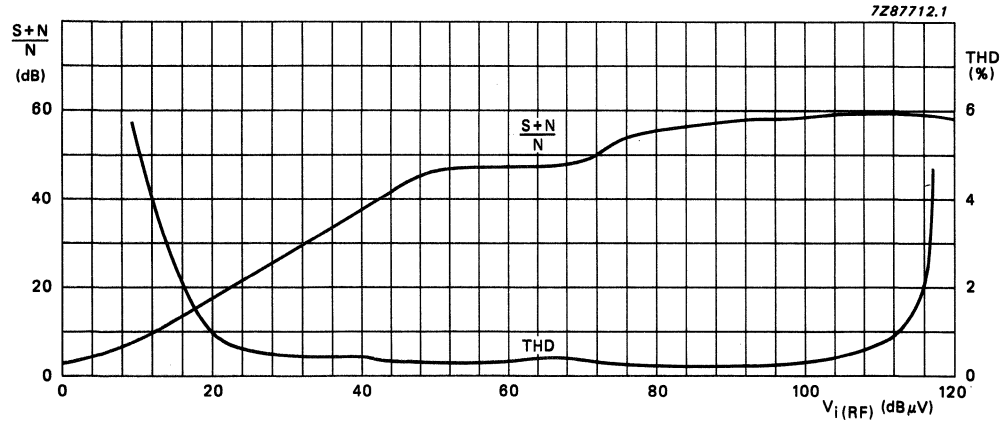


Fig.13 Total harmonic distortion and (S+N)/N as functions of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

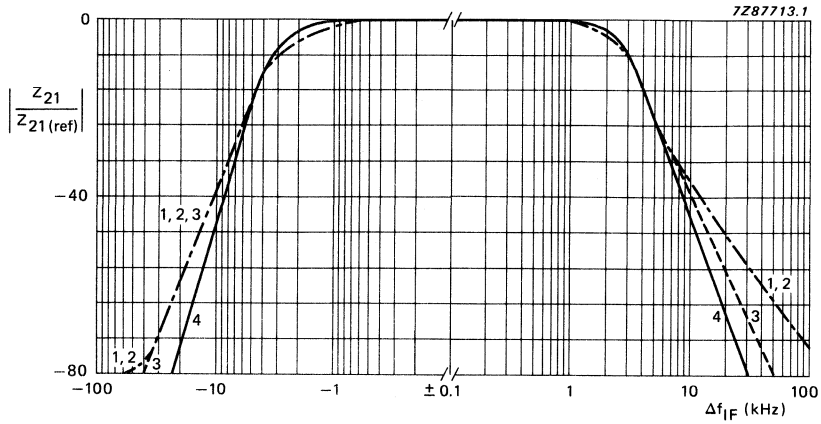


Fig.14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.14; centre frequency = 455 kHz.

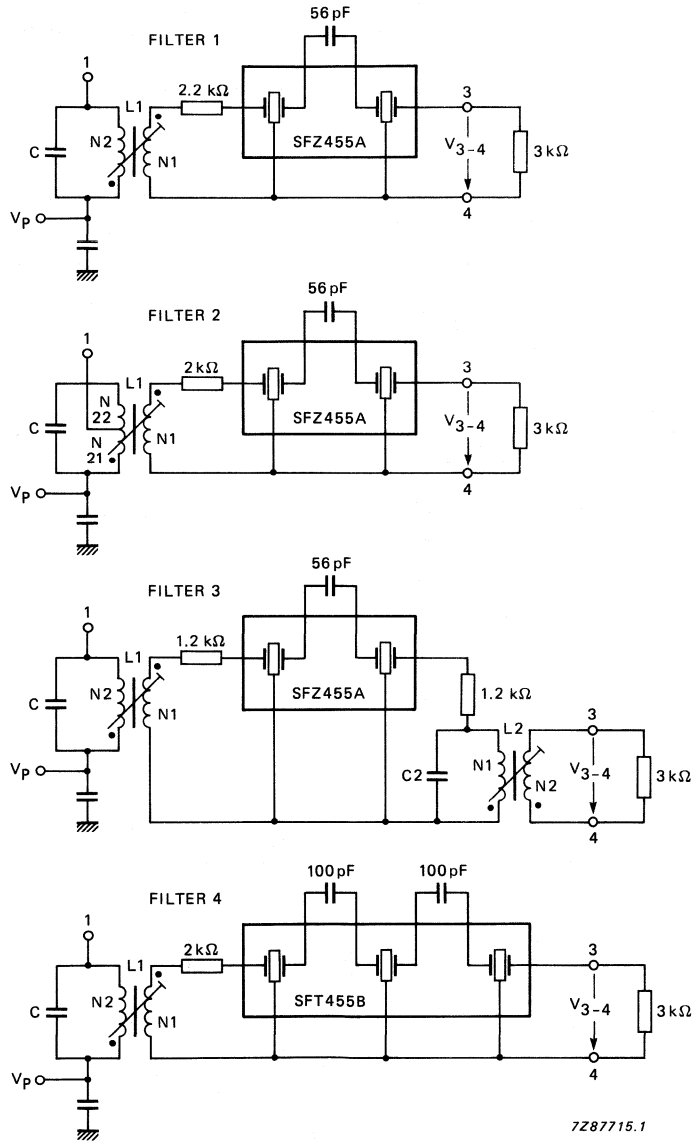


Fig.15 IF filter variants applied to the circuit of Fig.1; for filter data refer to Table 1.

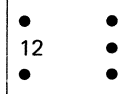
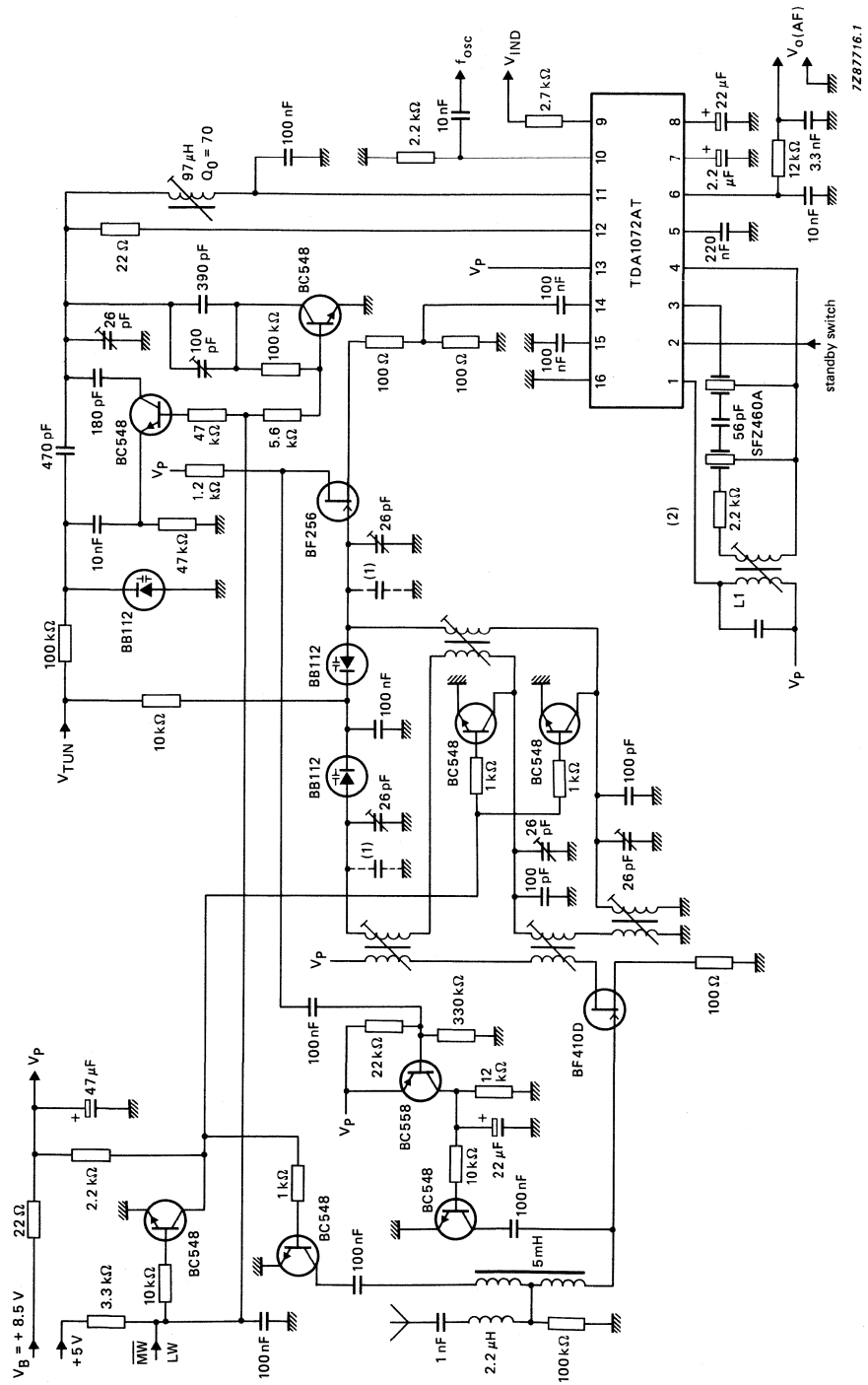
filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0.09	0.08	0.09	0.08	0.09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4.8	3.8	4.2		4.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0.70	0.67	0.68		0.68	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

Table 1 Data for IF filters shown in Fig.15. Criterium for adjustment is Z_F = maximum (optional selectivity curve at centre frequency f_o = 455 kHz). See also Fig.14.

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding. N2 the outer winding.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.

(2) For IF filter and coil data refer to Fig.1.

Fig.18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage AGC optimised for good large-signal handling.

DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20 V
Supply current (pin 11)	I_P	typ.	22 mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6 V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6 V
Total harmonic distortion	THD	typ.	0,05 %
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50 μV
Control range	$\Delta\alpha$	typ.	110 dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80 dB
Ripple rejection (100 Hz)	α_{100}	typ.	46 dB
Tracking of ganged potentiometers	ΔG_v	typ.	0,5 dB
Supply voltage range	V_P		7,5 to 23 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

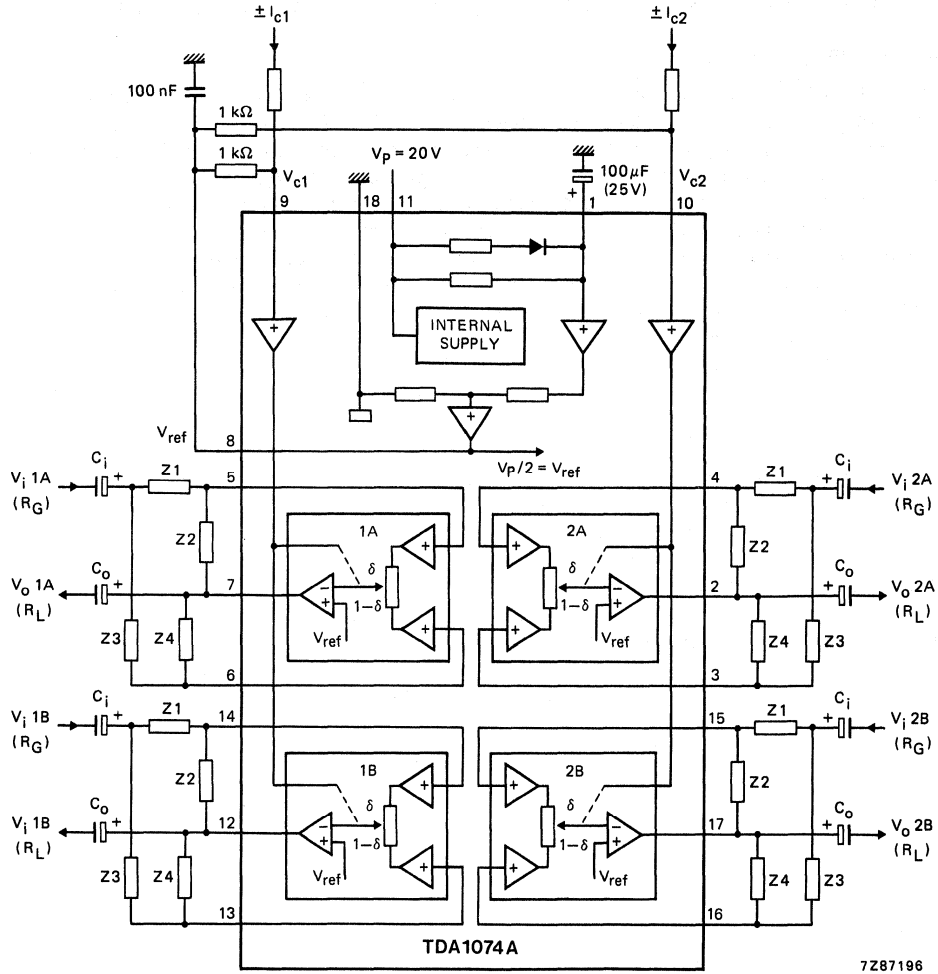


Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance R_G = 60 Ω; the output load resistance R_L = 4,7 kΩ; the coupling capacitors at the inputs and outputs are C_i = 2,2 µF and C_o = 10 µF respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23	V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1	V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i	0 to	V_P	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−30 to +	80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

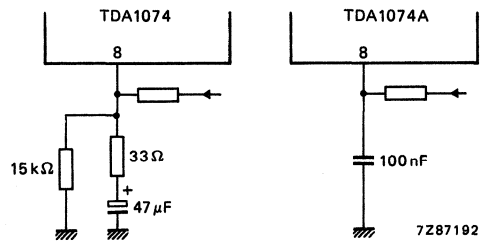


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; R_L > 4,7 kΩ; C_L < 30 pF; f = 1 kHz; with a linear frequency response ($V_{c1} = V_{c2}$ = 0 V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) $V_{c1} = V_{c2}$ = 0 V	f	10	–	20 000	Hz
Voltage gain at linear frequency response ($V_{c1} = V_{c2}$ = 0 V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at ± V_{c1} = ± V_{c2} = 120 mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) V_{c2} = 120 mV		–	17,5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2}$ = 120 mV		–	17,5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) V_{c1} = 120 mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1}$ = 120 mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)}$ = 300 mV f = 1 kHz (measured selectively)	THD	–	0,002	–	%
f = 20 Hz to 20 kHz	THD	–	0,005	–	%
at $V_{o(rms)}$ = 5 V f = 1 kHz	THD	–	0,015	0,1	%
f = 20 Hz to 20 kHz	THD	–	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i;o(rms)}$	5,5	6,2	–	V
Power bandwidth at reference level $V_{o(rms)}$ = 5 V (−3 dB); THD = 0,1%	B	–	40	–	kHz
Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	–	86	–	dB
f = 20 Hz to 20 kHz	α_{ct}	–	80	–	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	–	20	–	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	–	46	–	dB

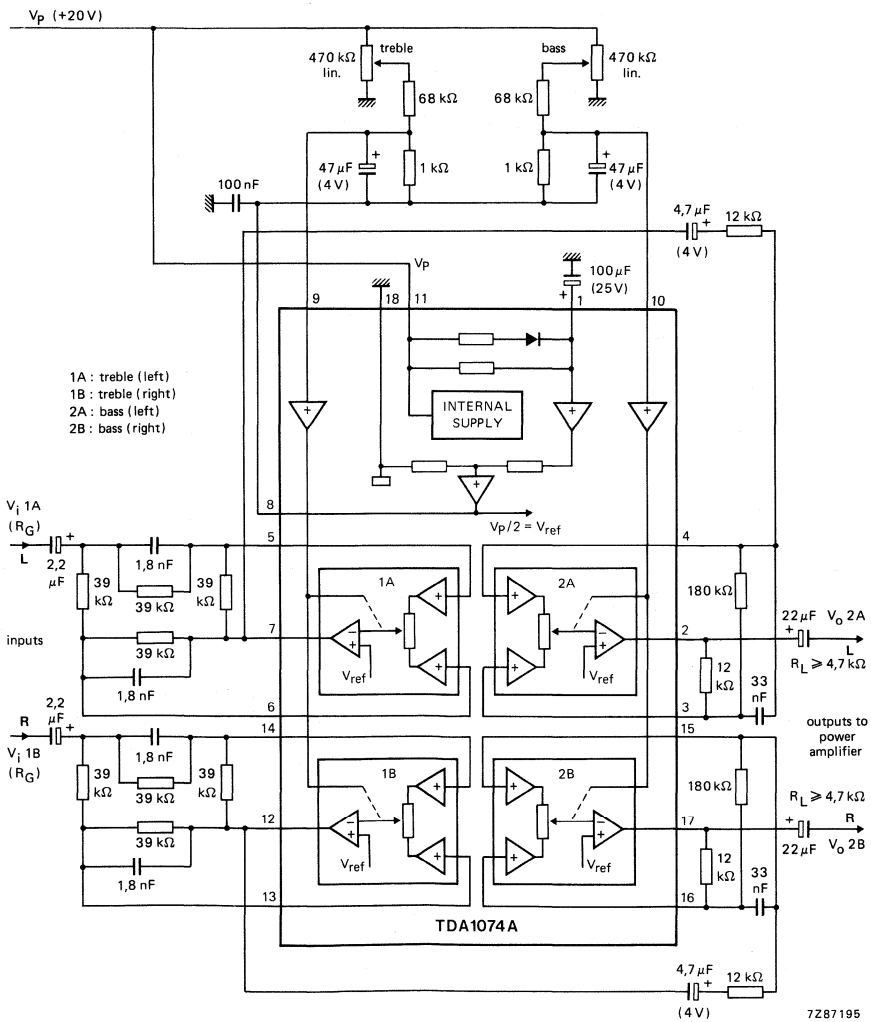


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

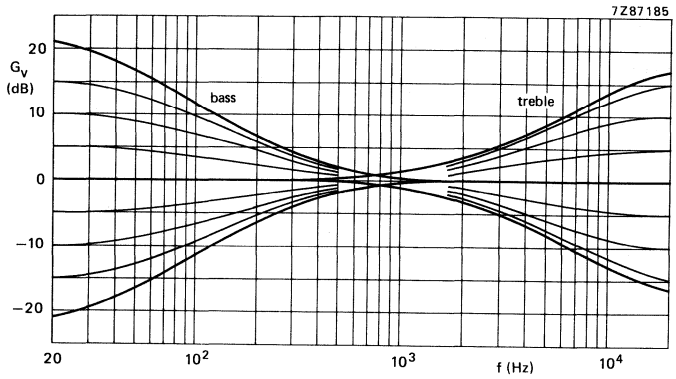


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

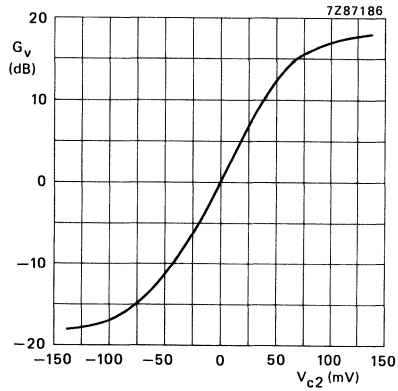


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

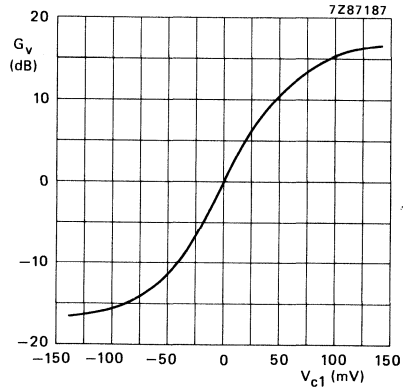
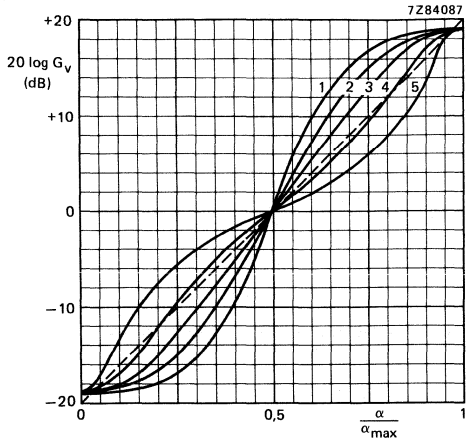


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

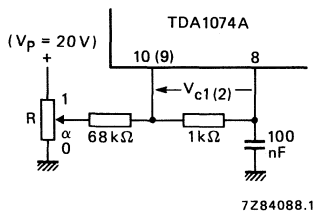


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

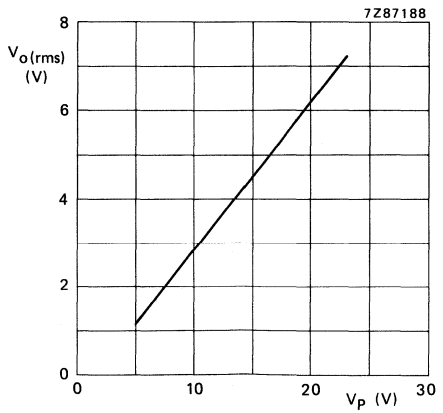


Fig. 9 Output signal level as a function of V_P; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

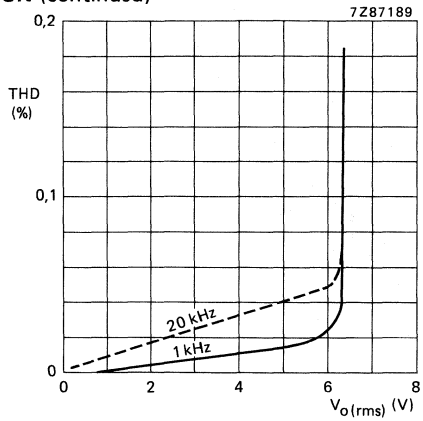


Fig. 10 Total harmonic distortion as a function of the output level; V_P = 20 V; R_L = 4,7 kΩ; $V_{c1} = V_{c2}$ = 0 V (linear, $G_{v\,tot}$ = 1). ——— f = 1 kHz; – – – – f = 20 kHz.

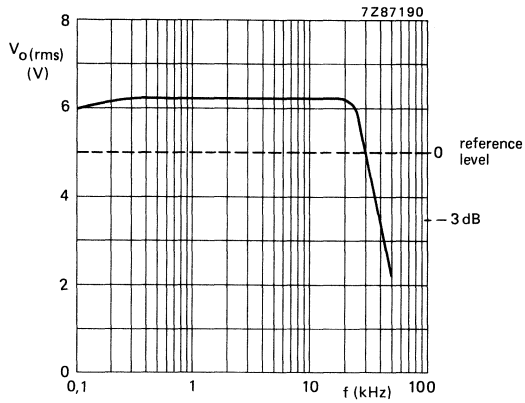


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

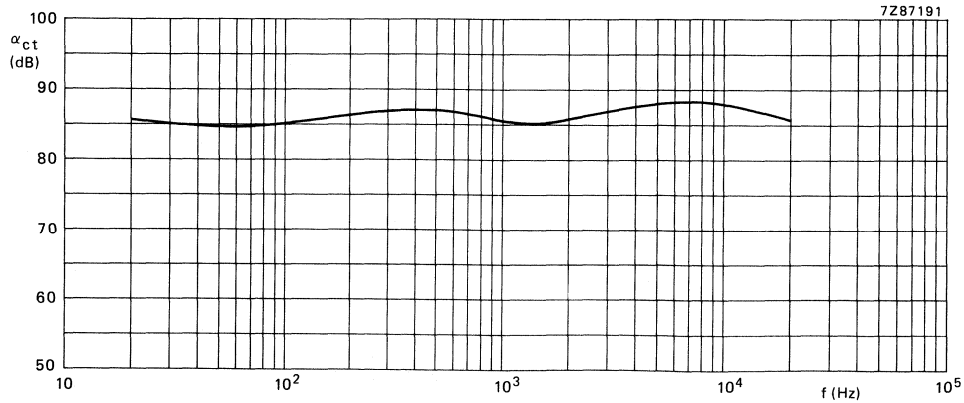
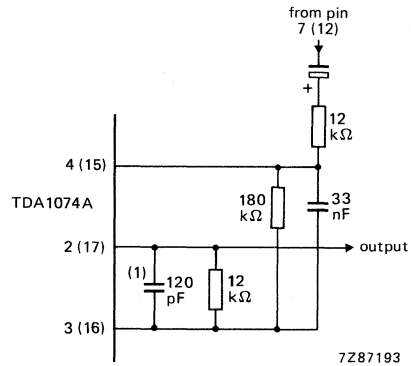


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1} = V_{c2}$ = 0 V); V_i = 5 V; R_G = 60 Ω; R_L = 4,7 kΩ.

Application recommendations

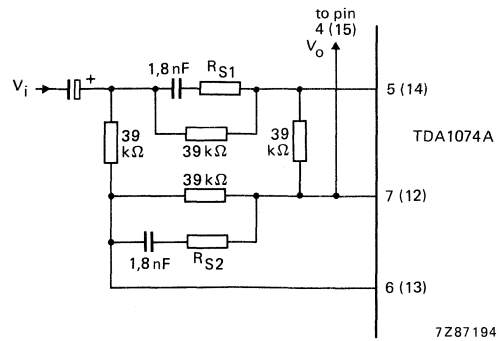
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8 (V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For $R_{S1} = R_{S2}$ = 3,3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

24 W BTL OR 2 × 12 W STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1510AQ is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6 Ω). With a supply voltage (V_P) of 14,4 V, an output power of 24 W can be delivered into a 4 Ω Bridge Tied Load (BTL), or when used as a stereo amplifier, 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Features

- Flexibility – stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range:						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	28,0	V
non-operating, load dump protection		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current		I_{so}	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$\|Z_I\|$	1	–	–	MΩ
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

TDA1510AQ: 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

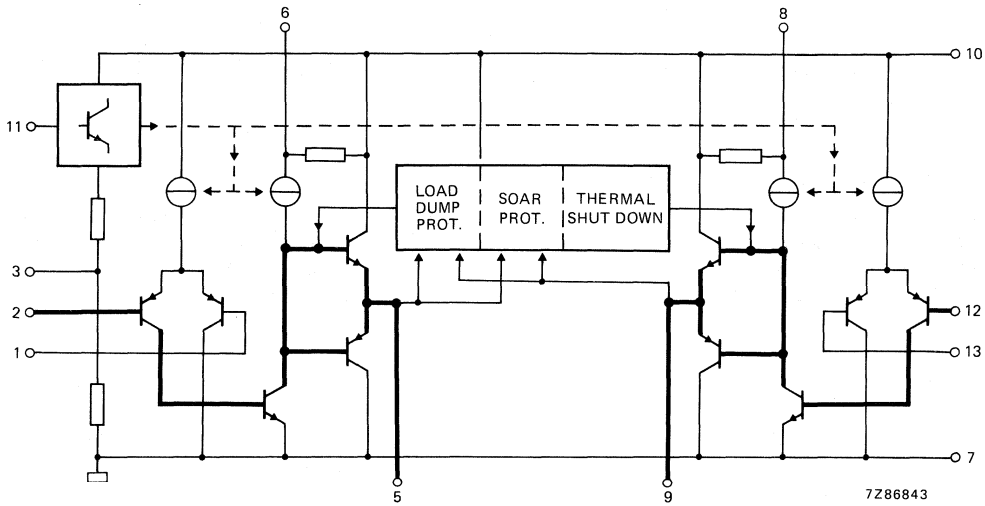


Fig. 1 Functional diagram; heavy lines indicate signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage:					
operating	pin 10	V_P	–	18	V
non-operating		V_P	–	28	V
non-operating, load dump protection	during 50 ms	V_P	–	45	V
Peak output current		I_{OM}	–	6	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Crystal temperature		T_c	–	+ 150	°C

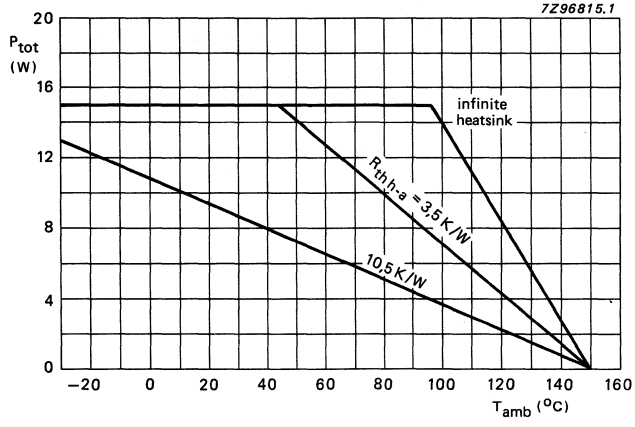


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

$(R_{th\ j\text{-}mb}) = 3{,}5$ K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3{,}5 = 3{,}5\ K/W$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3{,}5 = 10{,}5\ K/W$$

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	6,0	14,4	18,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current	$V_{11} \leqslant V_{10}$; note 1	I_{so}	0,15	0,35	0,80	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

parameter	parameter	symbol	min.	typ.	max.	unit
Bridge Tied Load application (BTL)						
Output power with bootstrap	note 6; R_L = 4 Ω					
	V_P = 13,2 V					
	d_{tot} = 0,5%	P_o	–	15,0	–	W
	d_{tot} = 10%	P_o	–	20,0	–	W
	V_P = 14,4 V					
	d_{tot} = 0,5%	P_o	15,5	18,0	–	W
	d_{tot} = 10%	P_o	20,0	24,0	–	W
Open loop voltage gain		G_o	–	75	–	dB
Closed loop voltage gain	note 2	G_c	39,5	40,0	40,5	dB
Frequency response	at –3 dB; note 3	f_r	–	20 to > 20 k	–	Hz
Input impedance	note 4	$\|Z_i\|$	1	–	–	MΩ
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz					
	R_S = 0 Ω	$V_{n\ (rms)}$	–	0,2	–	mV
	R_S = 10 kΩ	$V_{n\ (rms)}$	–	0,35	0,8	mV
	R_S = 10 kΩ; according to IEC 179 curve A	$V_{n\ (rms)}$	–	0,25	–	mV
Supply voltage ripple rejection	f = 100 Hz; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$\|\Delta V_{5\text{-}9}\|$	–	2	50	mV
Power bandwidth	–1 dB; d_{tot} = 0,5%	B	–	30 to > 40 k	–	Hz

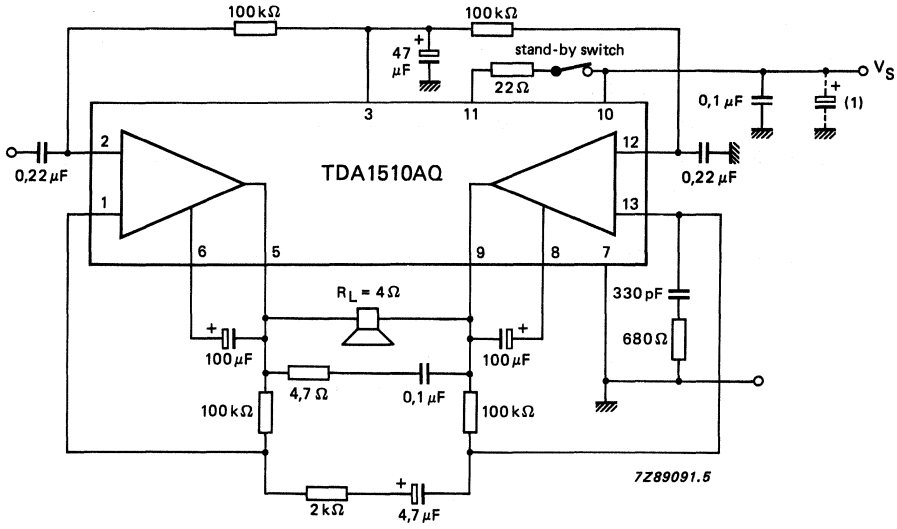
A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power; with bootstrap	note 6; $R_L = 4\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	4,5	–	W
	$d_{tot} = 10\%$	P_o	–	6,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	4,5	5,5	–	W
	$d_{tot} = 10\%$	P_o	6,0	7,0	–	W
	$R_L = 2\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	7,5	–	W
	$d_{tot} = 10\%$	P_o	–	10,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	7,75	9,0	–	W
	$d_{tot} = 10\%$	P_o	10,0	12,0	–	W
Output power; without bootstrap	notes 6, 8 and 9 $R_L = 4\ \Omega$ $V_P = 14{,}4$ V					
	$d_{tot} = 10\%$	P_o	–	6	–	W
Frequency response	notes 3 and 6					
	−3 dB	f_r	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	f = 1 kHz	SVRR	–	50	–	dB
Channel separation	$R_S = 10\ k\Omega$;					
	f = 1 kHz	α	40	50	–	dB
Closed loop voltage gain	note 7	G_c	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz;					
	$R_S = 0\ \Omega$	$V_{n(rms)}$	–	0,15	–	mV
	$R_S = 10\ k\Omega$	$V_{n(rms)}$	–	0,25	–	mV
	$R_S = 10\ k\Omega$; according to IEC179 curve A	$V_{n(rms)}$	–	0,2	–	mV

Notes to the characteristics

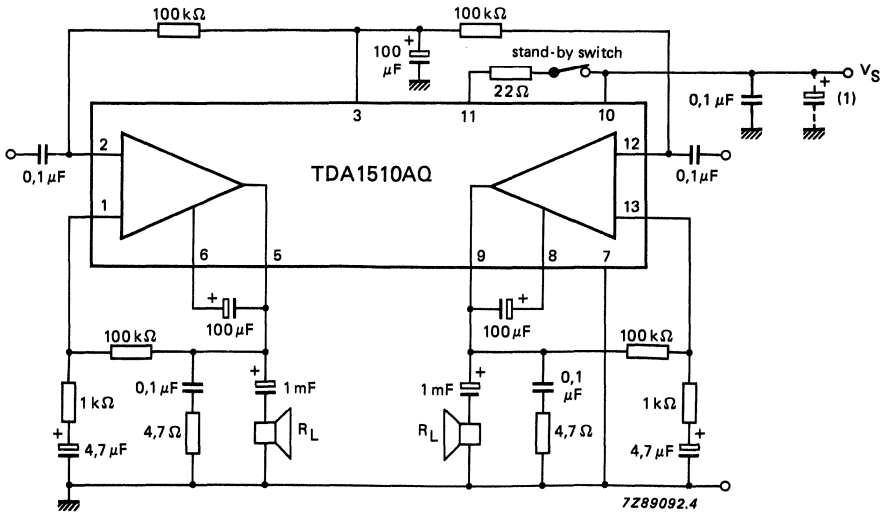
1. If $V_{11} > V_{10}$ then I_{11} must be < 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 and the 100 μF capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.

APPLICATION INFORMATION



(1) belongs to power supply

Fig. 3 Test and application circuit; Bridge Tied Load (BTL).



(1) belongs to power supply

Fig. 4 Test and application circuit; stereo mode.

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512A: 9-lead SIL; plastic power (SOT131).
TDA1512AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

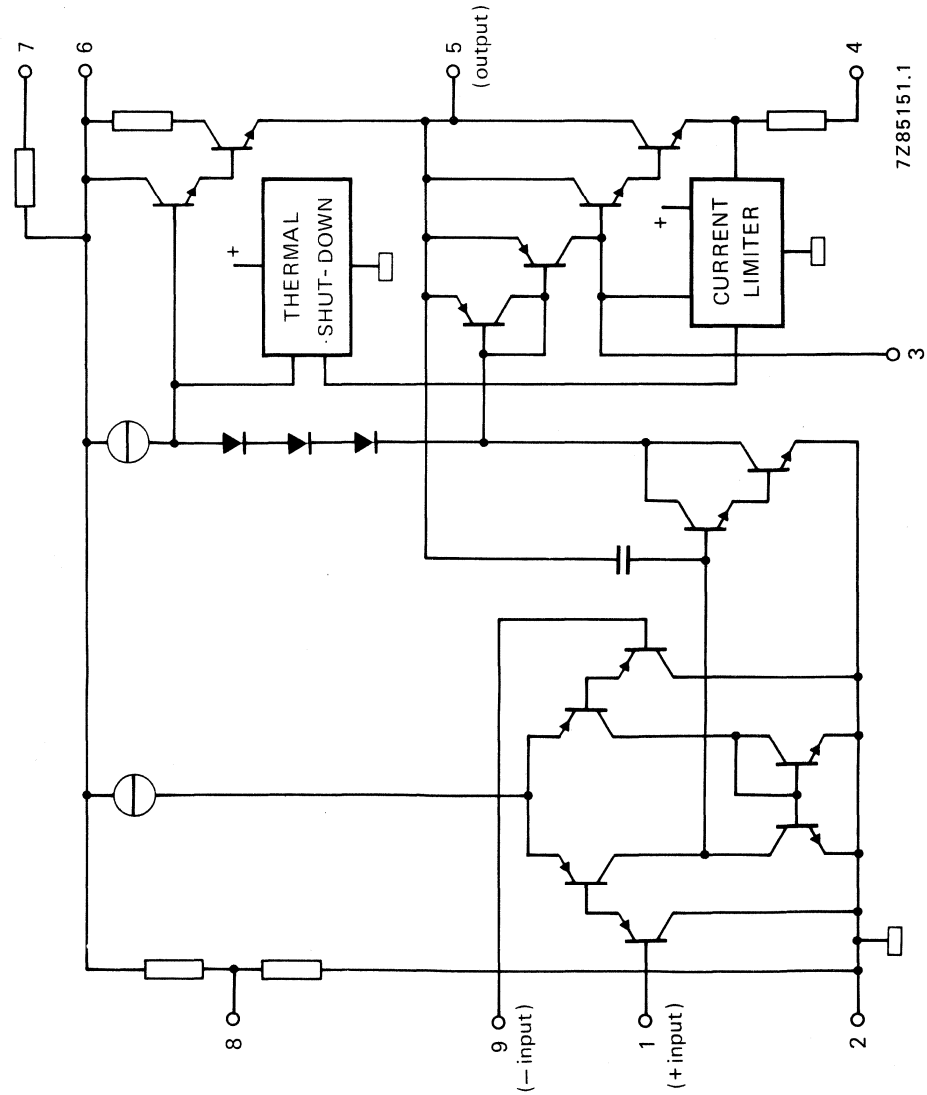


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

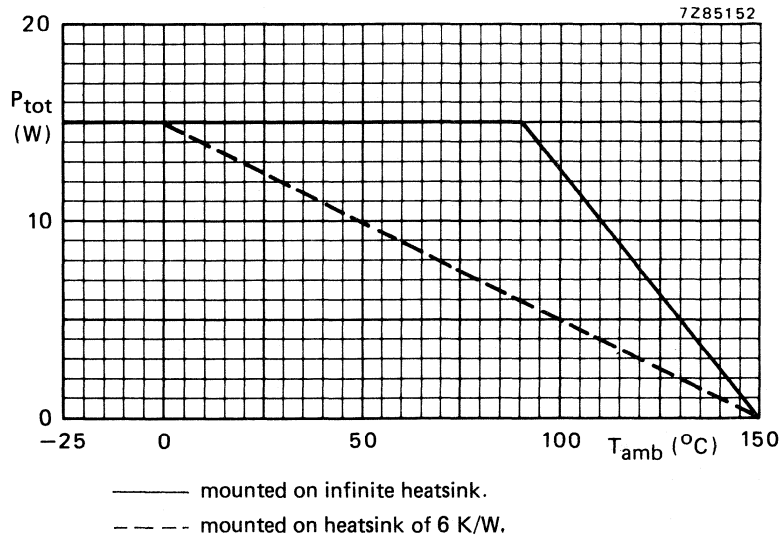


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

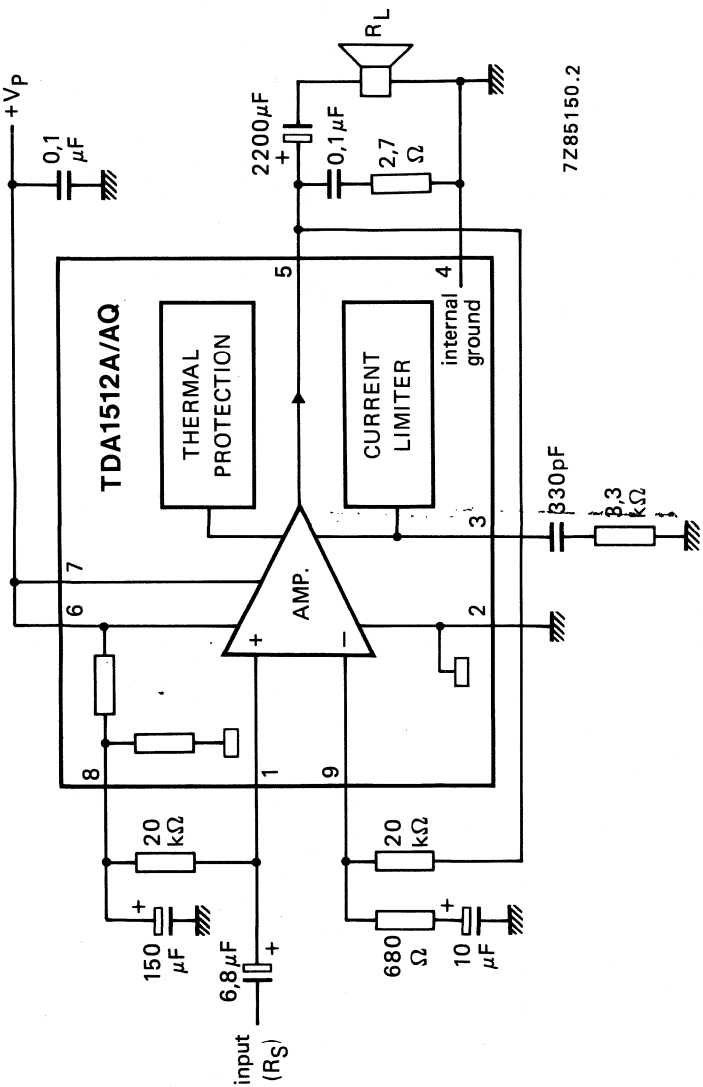


Fig. 3 Test circuit.

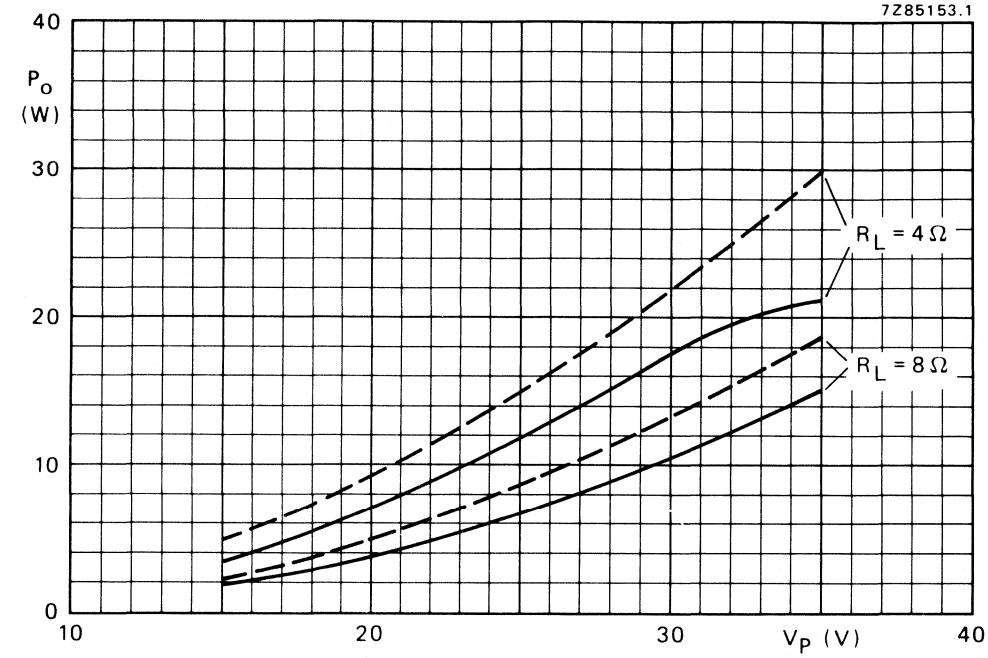


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

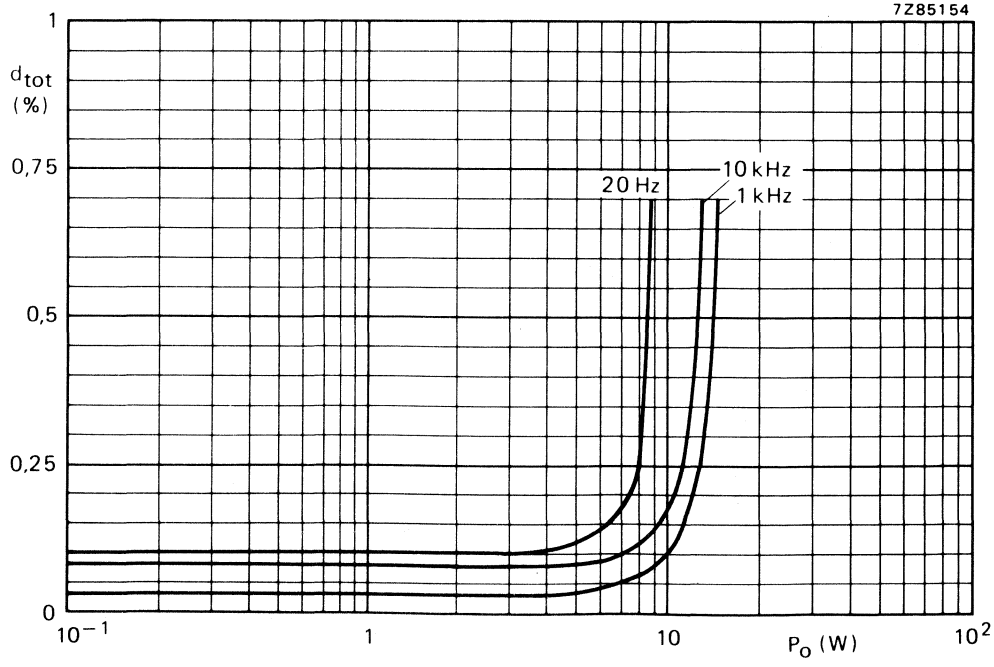


Fig. 5 Total harmonic distortion as a function of the output power.

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	50	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	82	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131A).

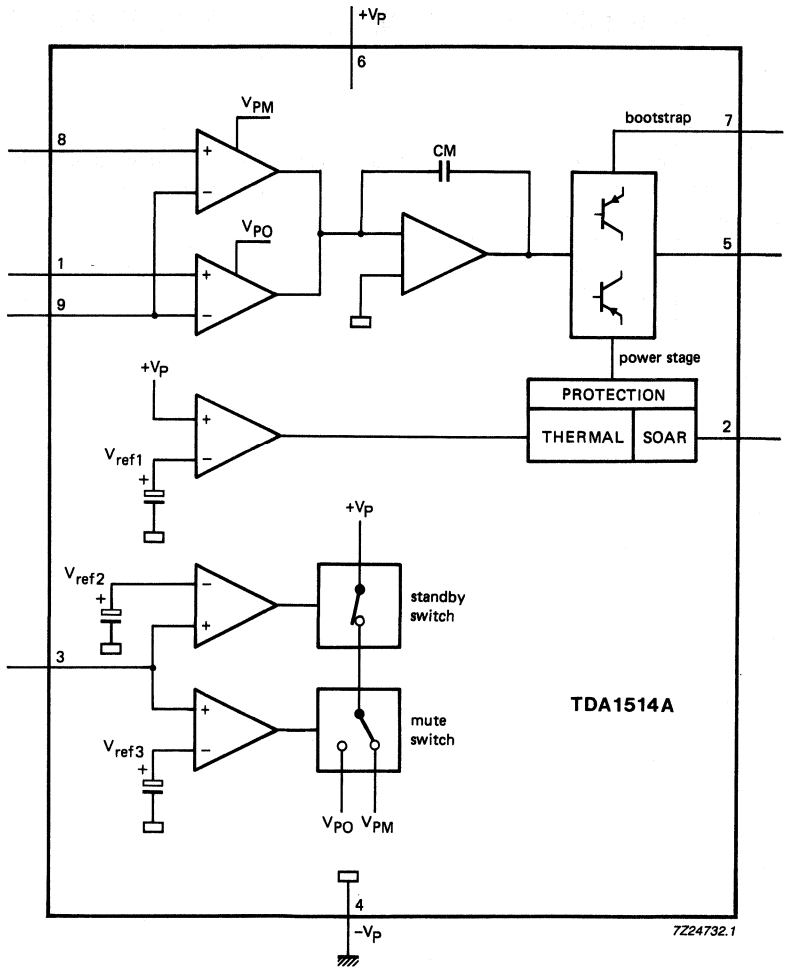


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 4)	V_P	–	±30	V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	–	70	V
Output current (repetitive peak)	I_o	–	8	A
Operating ambient temperature range	T_{amb}	see Fig.2		
Storage temperature range	T_{stg}	−65	+150	°C
Power dissipation		see Fig.2		
Thermal shut-down protection time	t_{pr}	–	1	hour
Mute voltage (pin 3 to pin 4)	V_m	–	7.25	V

THERMAL RESISTANCE

From junction to mounting base $R_{th\ j\text{-}mb}$ max. = 1 K/W

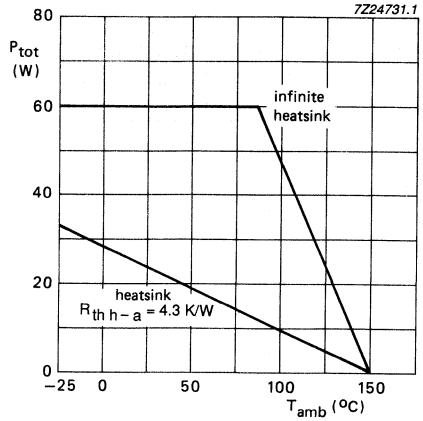


Fig.2 Power derating curve.

The theoretical maximum power dissipation for P_o = 40 W with a stabilized power supply is:

$$\frac{V_P^2}{2\pi^2 R_L} = 19\ W; \text{ where } V_P = \pm 27.5\ V;\ R_L = 8\ \Omega$$

Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C the total thermal resistance is:

$$R_{th\ j\text{-}a} = \frac{150 - 50}{19} = 5.3\ K/W$$

Since the thermal resistance of the SOT131A encapsulation is $R_{th\ j\text{-}mb} < 1$ K/W, the thermal resistance required of the heatsink is $R_{th\ h\text{-}a} < 4.3$ K/W.

SAFE OPERATING AREA (SOAR) PROTECTION

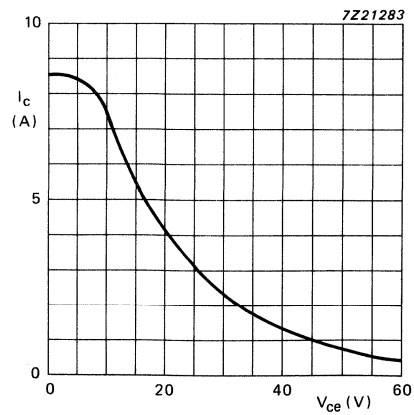


Fig.3 SOAR protection curve.

CHARACTERISTICS

V_P = ± 27.5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; test circuit as Fig.4; unless otherwise specified.

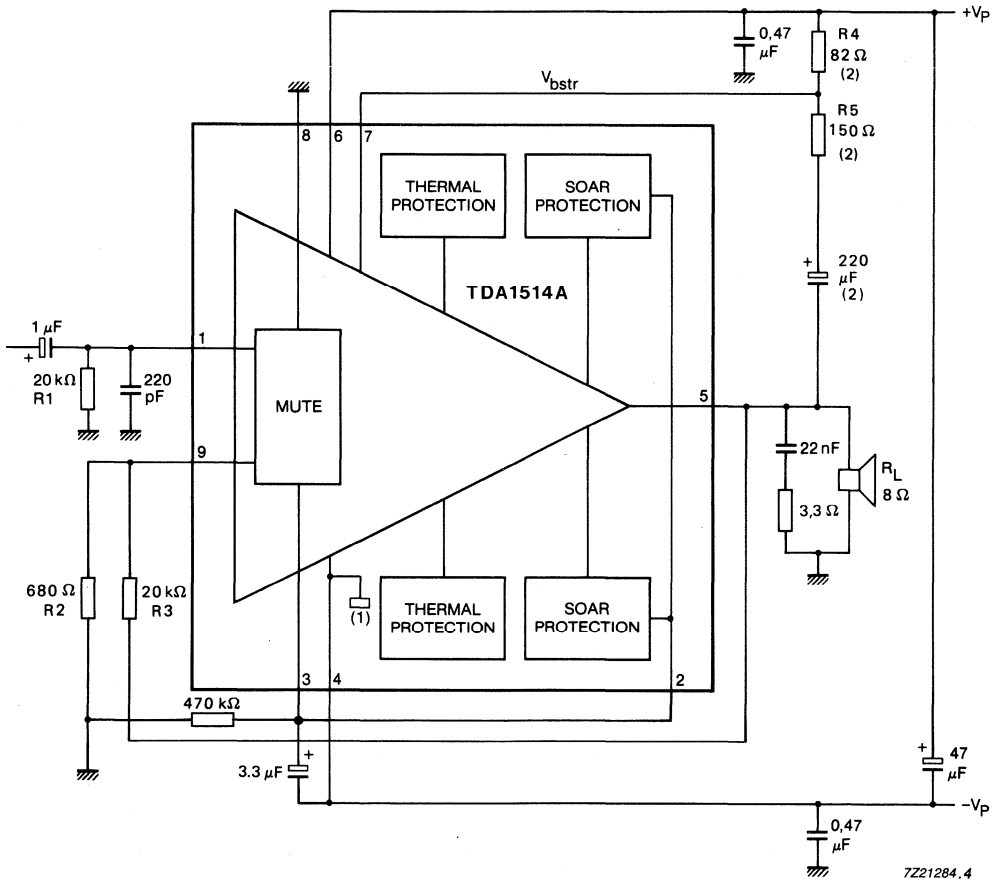
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Maximum output current (peak value)		$I_{OM\,max}$	6.4	–	–	A
Operating state						
Voltage (pins 3 to 4)		V_{3-4}	6	–	7.25	V
Total quiescent current	$R_L = \infty$	I_{tot}	30	56	90	mA
Output power	THD = –60 dB	P_o	37	40	–	W
	THD = –20 dB	P_o	–	51	–	W
Output power	V_P = ± 23 V; THD = –60 dB					
	R_L = 8 Ω	P_o	–	28	–	W
	R_L = 4 Ω	P_o	–	50	–	W
Total harmonic distortion	P_o = 32 W	THD	–	–90	–80	dB
Intermodulation distortion	P_o = 32 W note 1	d_{im}	–	–86	–	dB
Power bandwidth	(–3 dB); THD = –60 dB	B	–	20 to 25 000		Hz
Slew rate		dV/dt	–	14	–	V/μs
Closed loop voltage gain	note 2	G_c	–	30	–	dB
Open loop voltage gain		G_o	–	89	–	dB
Input impedance	note 3	$\|Z_i\|$	1	–	–	MΩ
Signal-to-noise ratio	note 4 P_o = 50 mW	S/N	80	83	–	dB
Output offset voltage		V_o	–	7	200	mV
Input bias current		I_I	–	0.1	1.0	μA
Output impedance		$\|Z_o\|$	–	–	0.1	Ω
Supply voltage ripple rejection	note 5	SVRR	58	64	–	dB
Quiescent current into pin 2	note 6	I_2	–	0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute state						
Voltage on pin 3		V_{3-4}	2	–	4.5	V
Offset voltage		V_o	–	30	200	V
Output voltage	$V_{i(rms)}$ = 1 V f = 1 kHz	V_o	–	450	–	μV
Ripple rejection	note 5	RR	–	60	–	dB
Standby state						
Voltage on pin 3		V_{3-4}	0	–	0.9	V
Total quiescent current		I_{tot}	–	18	25	mA
Ripple rejection	notes 5 and 7	RR	–	60	–	dB
Supply voltage to obtain standby state		$\pm V_P$	5.0	–	7.0	V

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig.4, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig.4) is determined by the bias resistor R1.
4. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistance of 2 kΩ.
5. f = 100 H_3; R_S = 2 kΩ; ripple voltage = 500 $mV_{(eff)}$ on positive and negative supply.
6. The quiescent current into pin 2 has an impact on the mute time.
7. Without bootstrap.



(1) Mounting base connected to $-V_P$.

(2) When used without a bootstrap these components are disconnected and pin 6 is connected to pin 7 thus decreasing the output power by approximately 4 W.

(3) When $R_L = 4\ \Omega$: R4 = 47 Ω and R5 = 82 Ω.

Fig.4 Application and test circuit.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515BQ is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	1	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\|Z_i\|$	>	1	MΩ
Bridge tied load application (BTL)	V_P	=	14,4 | 13,2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = 0,5%	P_o	typ.	18 | 15	W
d_{tot} = 10%	P_o	typ.	24 | 20	W
Supply voltage ripple rejection; R_S = 0 Ω; f = 100 Hz	RR	typ.	50 | 50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5-9}\|$	<	50 | 50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ.	7 | 6	W
R_L = 2 Ω	P_o	typ.	12 | 10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ.	5,5 | 4,5	W
R_L = 2 Ω	P_o	typ.	9 | 7,5	W
Channel separation	α	>	40 | 40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ.	0,2 | 0,2	mV

PACKAGE OUTLINE 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

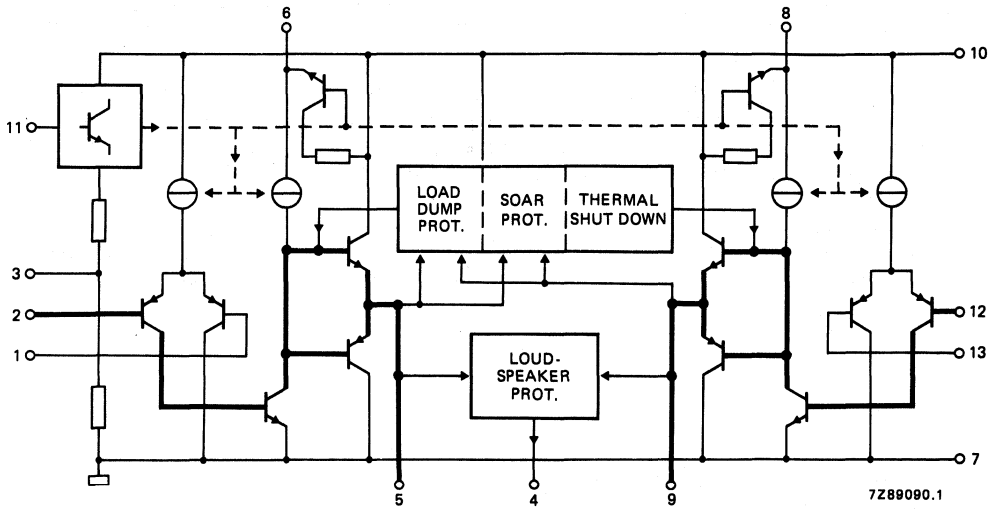


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

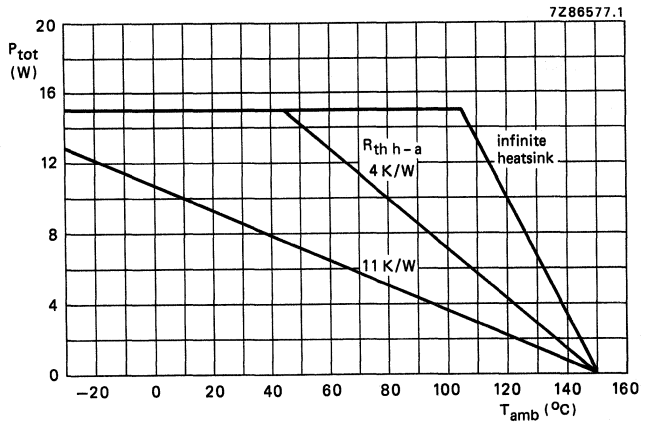


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1,8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$\|Z_{OFF}\|$	>	100 kΩ
Stand-by current at V_{11} = 0 to 0,8 V	I_{sb}	typ.	1 μA
		<	100 μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ.	10 μA
		<	100 μA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)			
V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	>	15,5 W
		typ.	18 W
V_P = 14,4 V; d_{tot} = 10%	P_o	>	20 W
		typ.	24 W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15 W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0,5) dB
Output power without bootstrap (note 9)			
V_P = 14,4 V; d_{tot} = 10 %	P_o	typ.	15 W
V_P = 14,4 V; d_{tot} = 0,5 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 10 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 0,5 %	P_o	typ.	9 W
Frequency response at −3 dB (note 3)	B	20 Hz to min.	20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,35 mV
		<	0,8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	>	42 dB
		typ.	50 dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 mV
		typ.	2 mV
Loudspeaker protection (all conditions) maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; **d_{tot} = 0,5%**	B		30 Hz to 40 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at $\mathbf{d_{tot}}$ **= 0,5%**; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	6 W
Frequency response at −3 dB (note 3)	B	40 Hz to min.	20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,2 mV

Notes

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

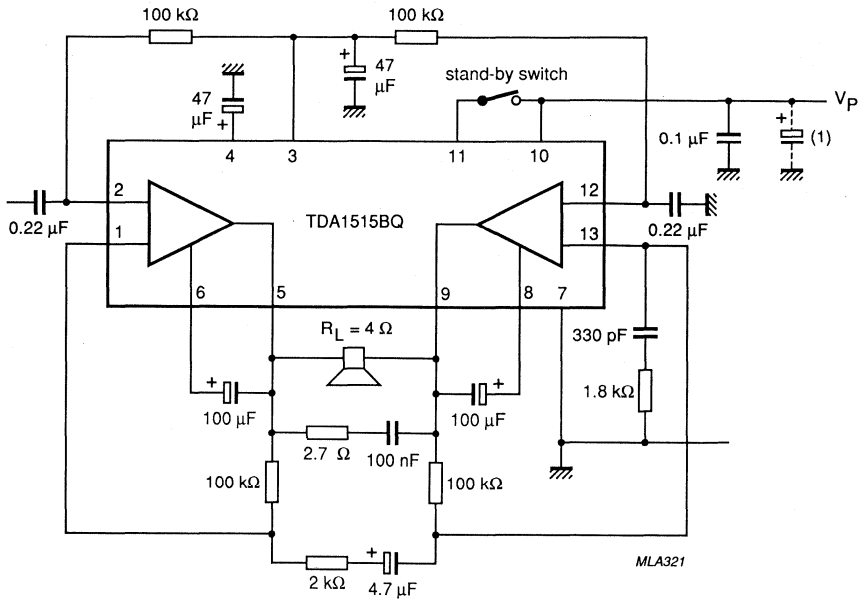


Fig. 3 Test/application circuit bridge tied load (BTL).

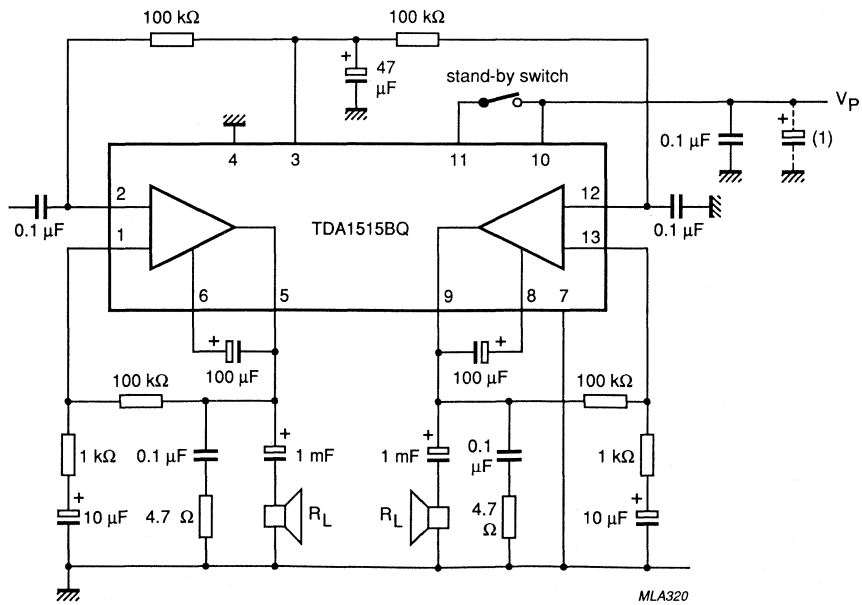


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1516BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use — stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1518Q (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	100	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

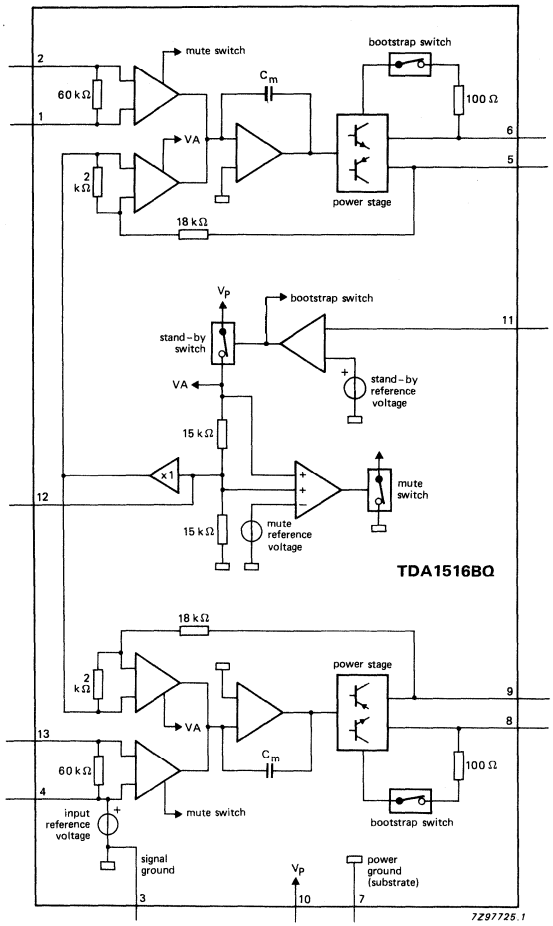


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1516BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

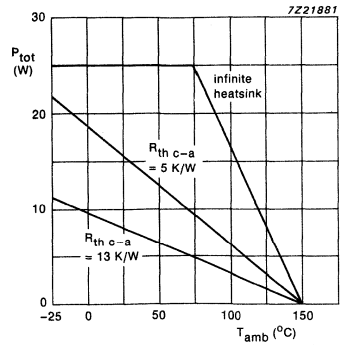


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	2	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7.5	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 9	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	–	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD =0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13,5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5% P_o = 15 W	B_W	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	25	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	100	200	μV
mute	note 9	$V_{no(rms)}$	–	60	–	μV

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,5 to 18 V.
3. At 18 V < V_P < 30 V the d.c. output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (Vp), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

APPLICATION INFORMATION

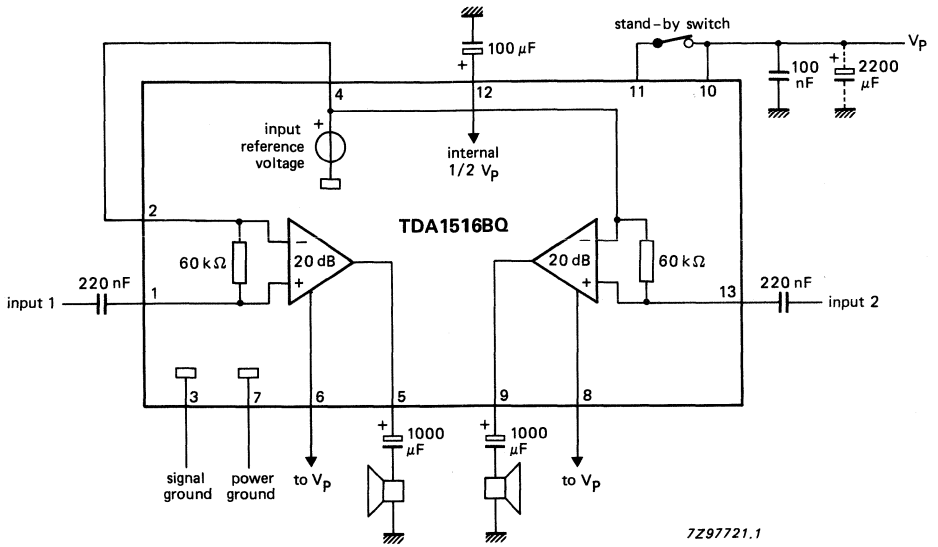


Fig. 3 Stereo application circuit diagram.

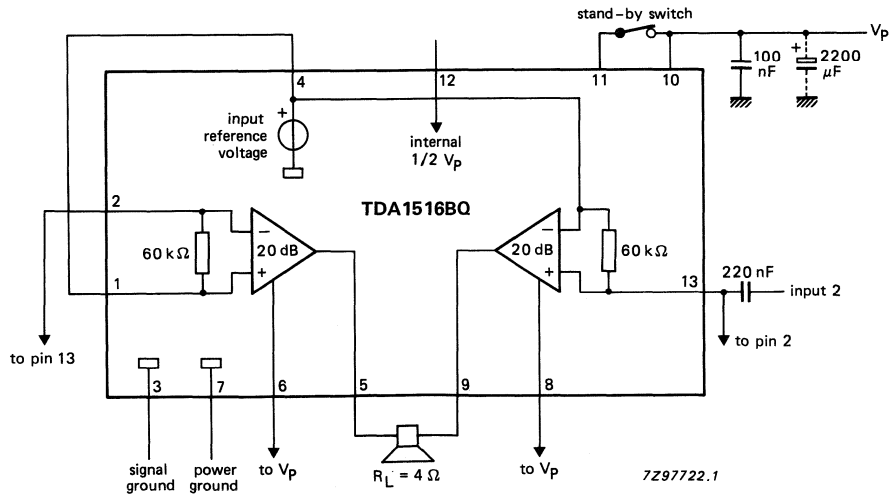


Fig. 4 BTL application circuit diagram (without bootstrapping).

DEVELOPMENT DATA

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a 9-lead single-in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1519 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
Supply voltage ripple rejection	f = 100 Hz to 100 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

PINNING

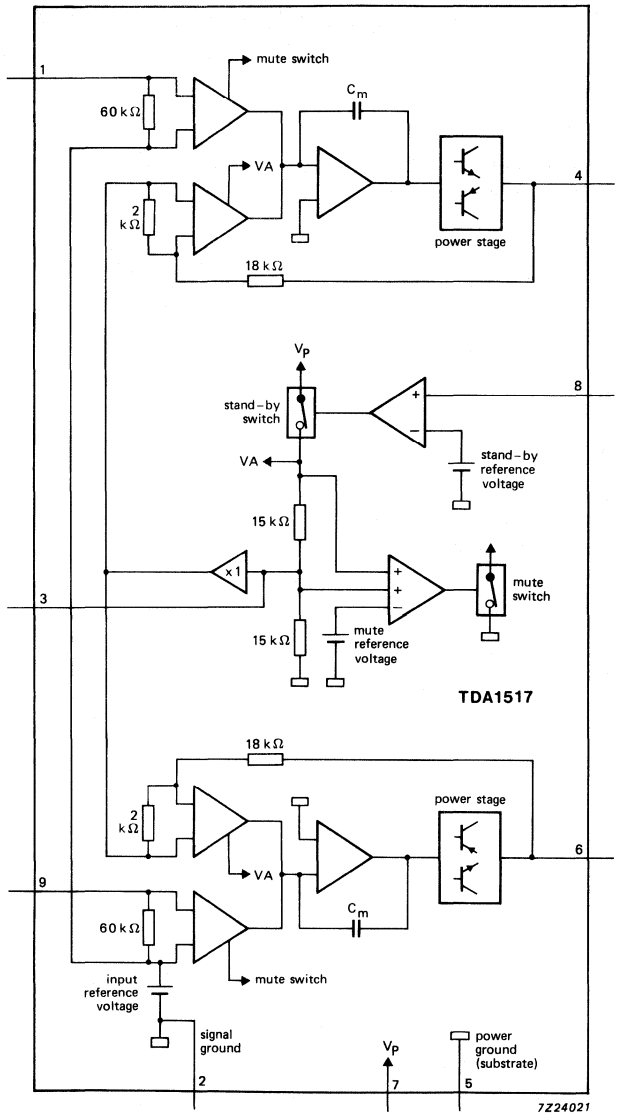


Fig. 1 Block diagram.

1	−INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-interting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C

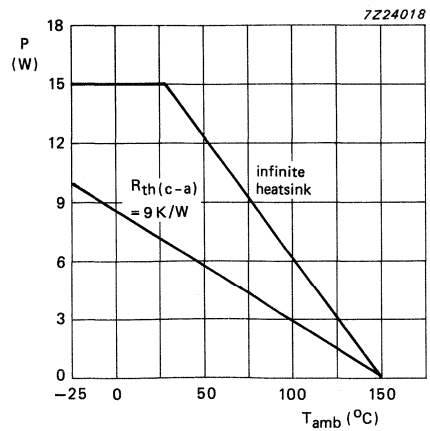


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch	see Fig. 3					
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max); f = 20 Hz to 15 kHz	V_O	–	–	2	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 6					
ON		SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage:	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 8	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

DEVELOPMENT DATA

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

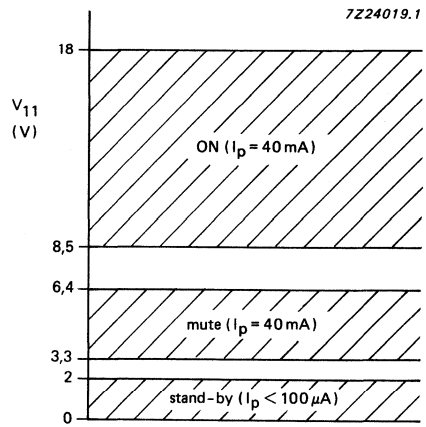


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

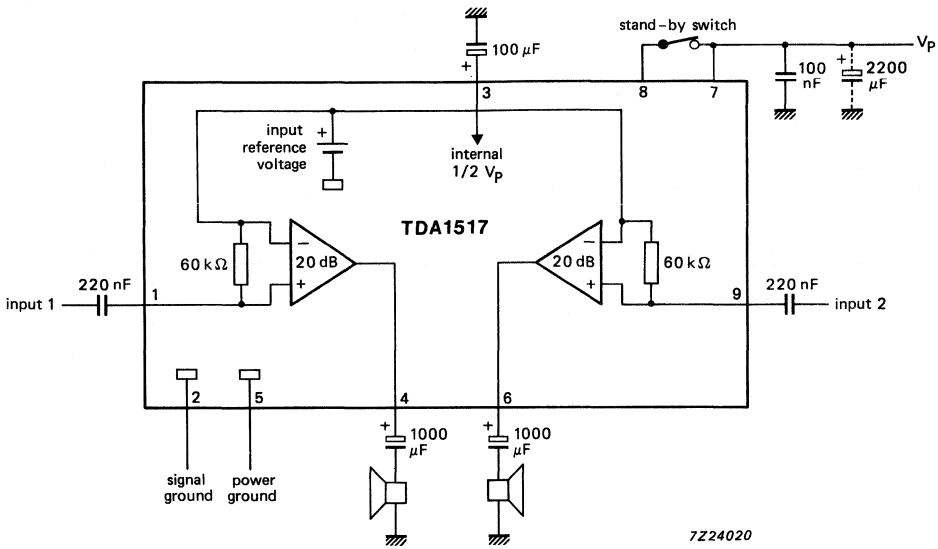


Fig. 4 Application circuit diagram.

DEVELOPMENT DATA

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1518BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use – stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1516BQ (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	250	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

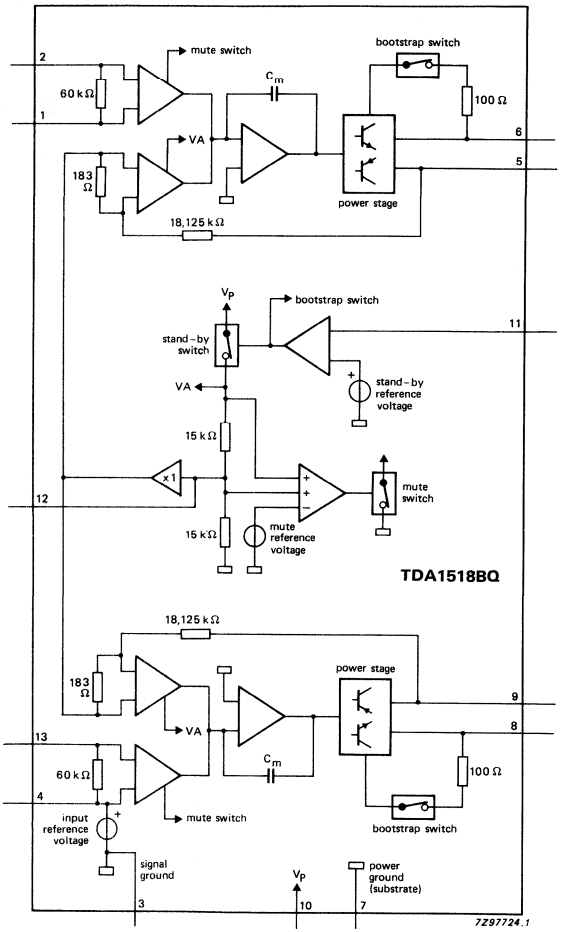


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1518BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C

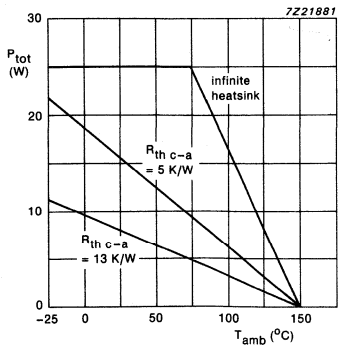


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	30	*	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	200	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	20	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7,75	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	0.1	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD = 0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13.5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5% P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Switch-on/switch-off behaviour		dV/dt	–	–	*	V/ms

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,1 V to 18 V.
3. At 18 V $<$ V_P $<$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (Vp), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

* Value to be fixed.

APPLICATION INFORMATION

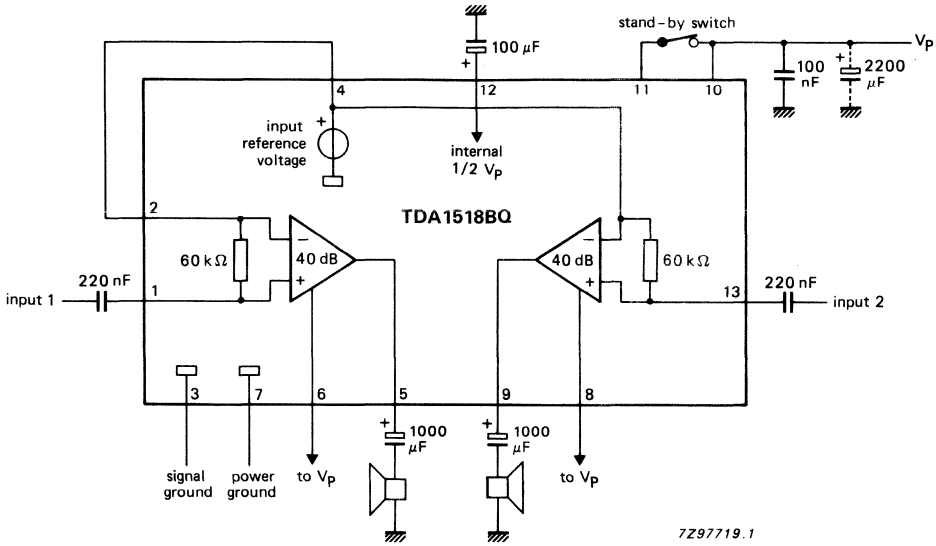


Fig. 3 Stereo application circuit diagram.

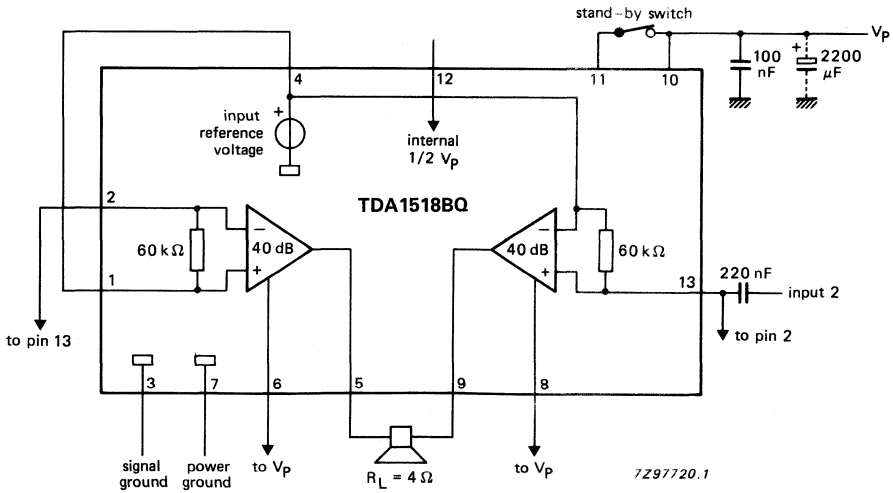


Fig. 4 BTL application circuit diagram (without bootstrapping).

DEVELOPMENT DATA

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519 is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1517 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
Supply voltage ripple rejection	f = 100 Hz	SVRR	40	–	–	dB
	f = 1 kHz to 10 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

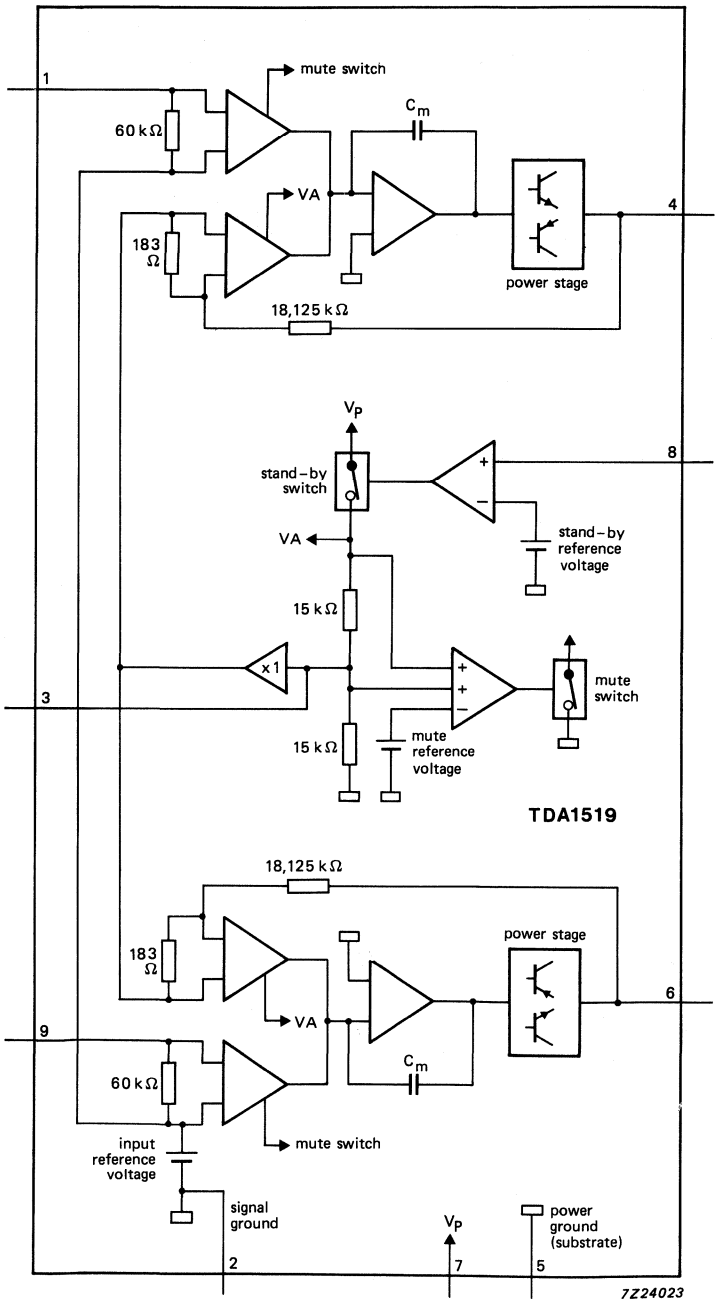


Fig. 1 Block diagram.

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1519 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+ 150	°C

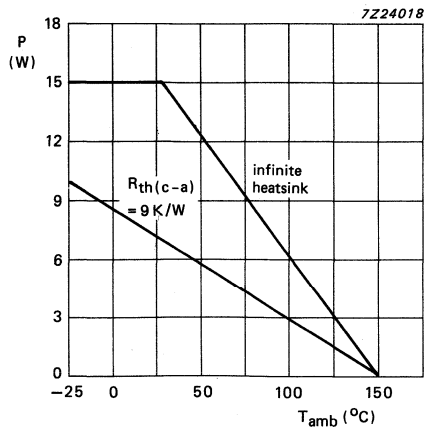


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch						
Switch-on voltage level	see Fig. 3	V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection	note 6					
ON	f = 100 Hz	SVRR	40	–	–	dB
ON	f = 10 Hz to 10 kHz	SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 8	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

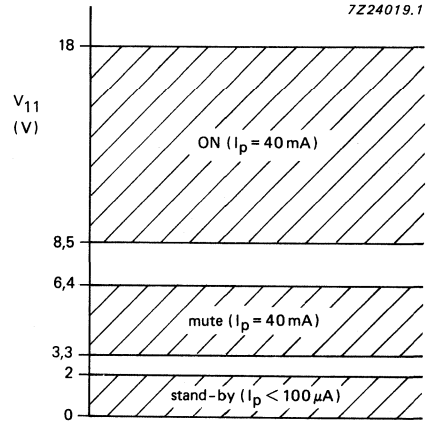


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

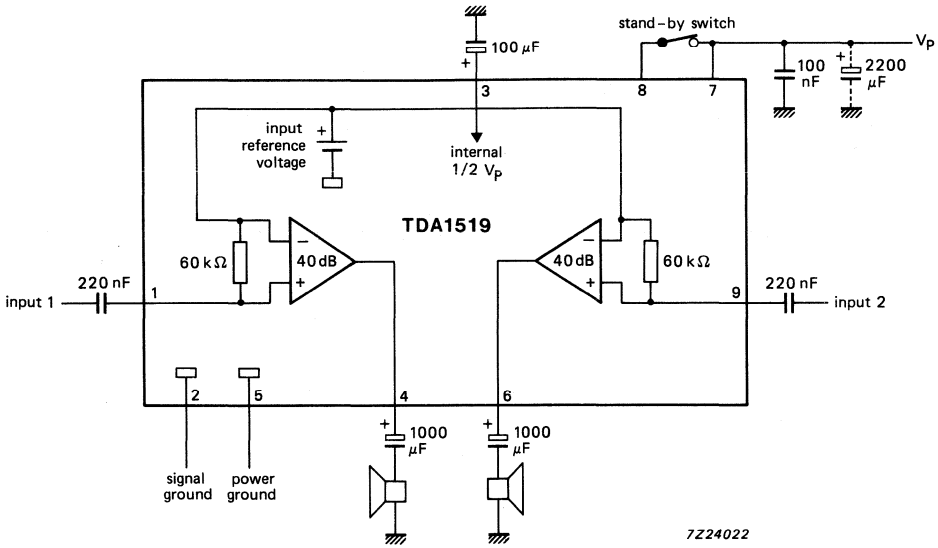


Fig. 4 Application circuit diagram.

DEVELOPMENT DATA

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMLIFIER

GENERAL DESCRIPTION

The TDA1519A is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519B (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	17.5	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

9-lead SIL; plastic power (SOT131).
9-lead SIL-bent-to-DIL; plastic power (SOT157).

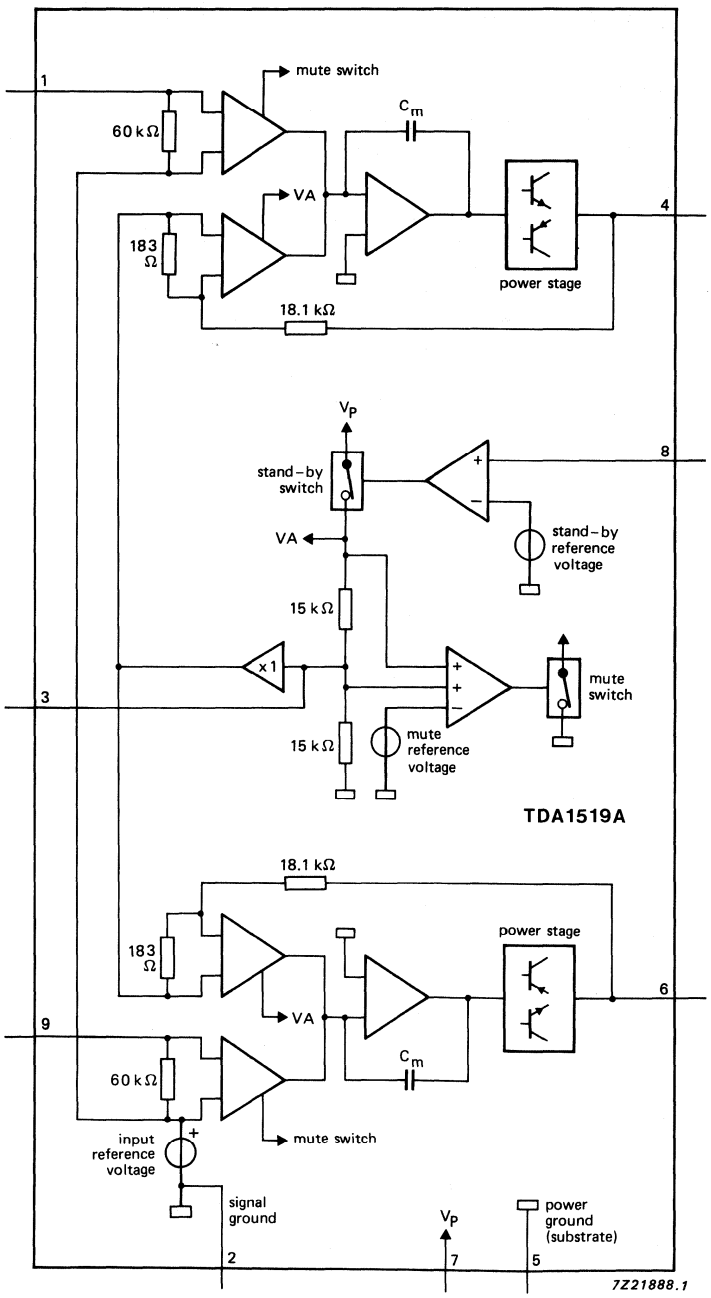


Fig.1 Block diagram.

PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1519A contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	17.5	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig.2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C

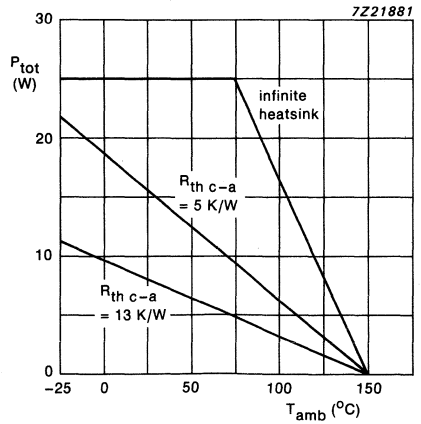


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	17.5	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6.0	–	W
Output power at R_L = 2 Ω	note 3					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5 and 8	RR	45	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 10	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	13	–	W
	THD = 10%	P_o	–	17.5	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_W	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5 and 8	RR	48	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 10	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 17.5 V and AC operating at V_P = 8.5 V to 17.5 V.
2. At 17.5 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Frequency between 100 Hz and 10 kHz.
9. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
10. Noise output voltage independent of R_S (V_I = 0 V).

DEVELOPMENT DATA

APPLICATION INFORMATION

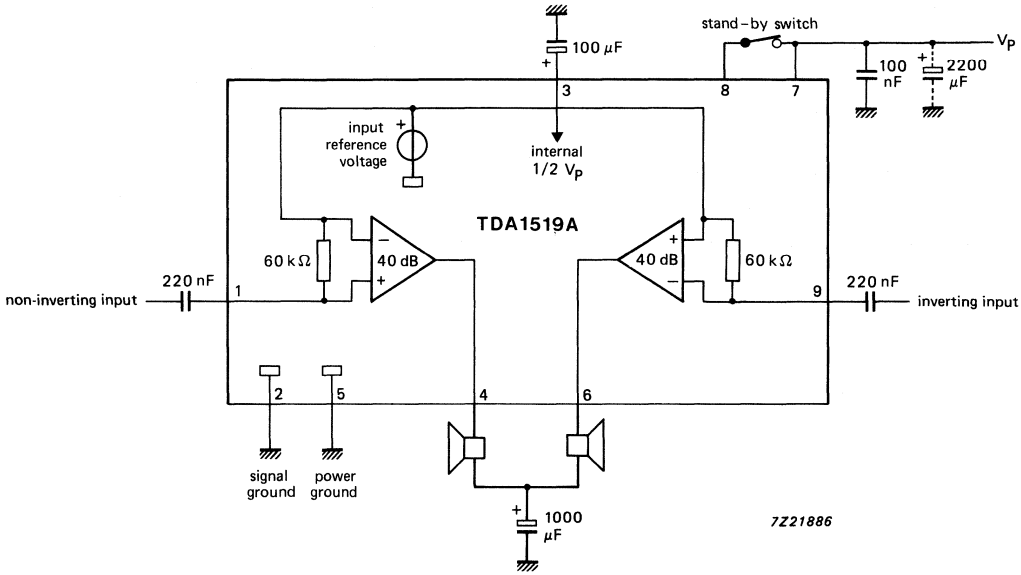


Fig.3 Stereo application circuit diagram.

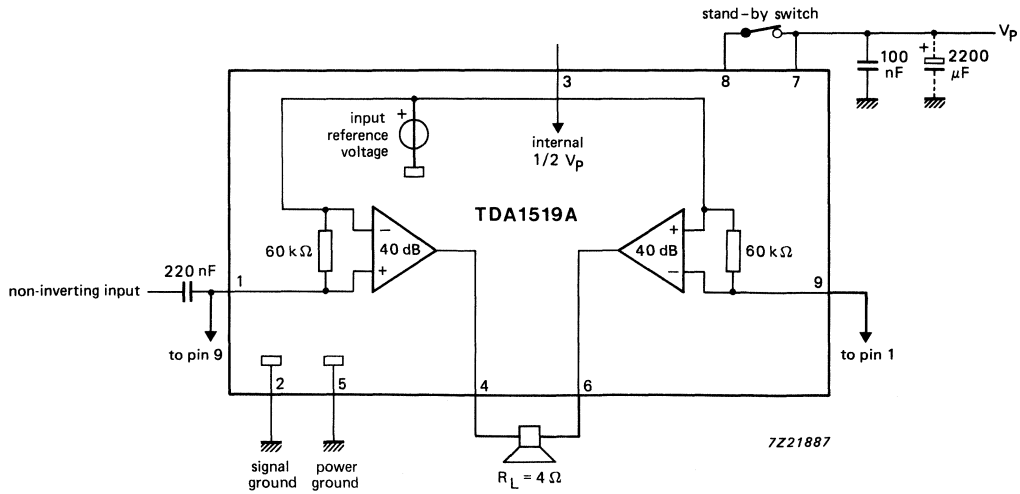


Fig.4 BTL application circuit diagram.

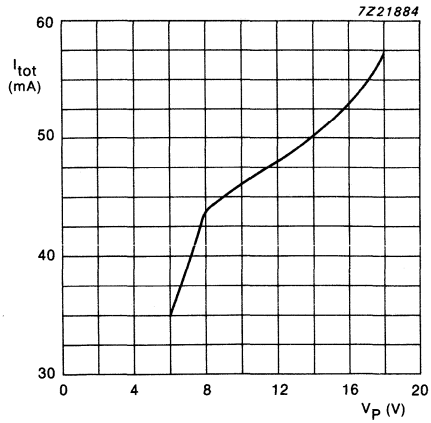


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

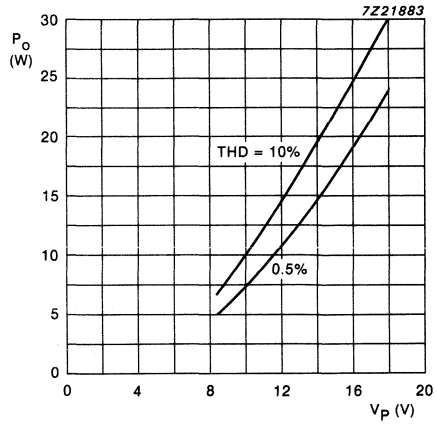


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

DEVELOPMENT DATA

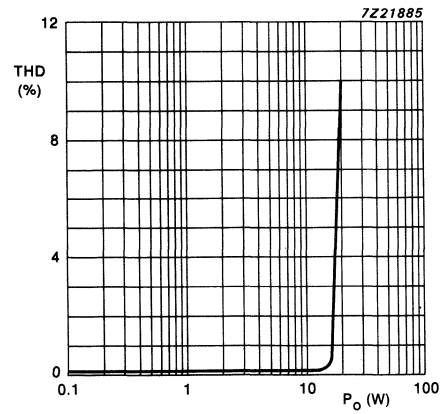


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

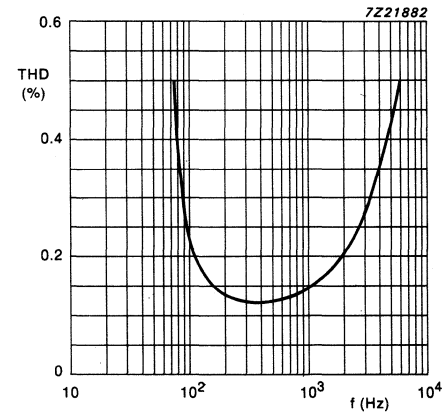


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at $R_L = 4\ \Omega$; $P_o = 1$ W.

12 W BTL OR 2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519B is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

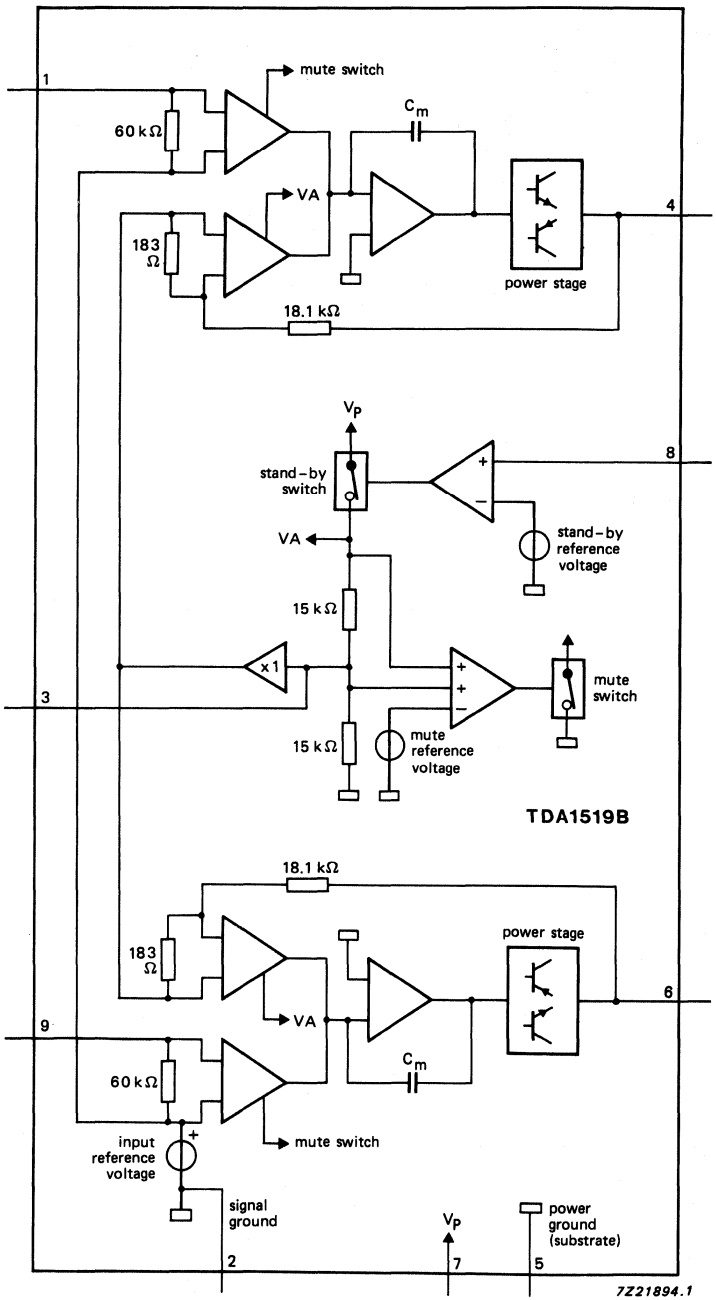
- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519A (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2.5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 8 Ω	P_o	–	12	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).



PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

Fig.1 Block diagram.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1519B contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2.5	A
Total power dissipation	see Fig.2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+150	°C

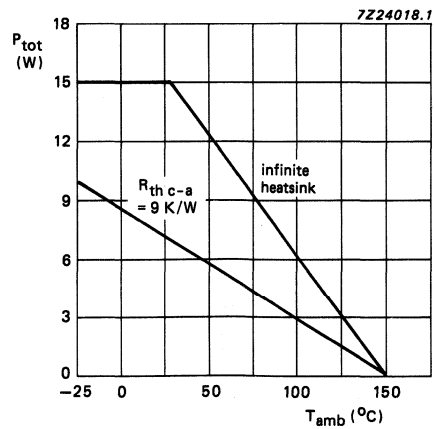


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10!	P_o	5.5	6.0	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	3.5	–	W
	THD = 10%	P_o	–	4.8	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5, 6 and 7	RR	45	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	8	10	–	W
	THD = 10%	P_o	11	12	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	7.5	–	W
	THD = 10%	P_o	–	10	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_W	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5, 6 and 7	RR	48	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ≤ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

DEVELOPMENT DATA

APPLICATION INFORMATION

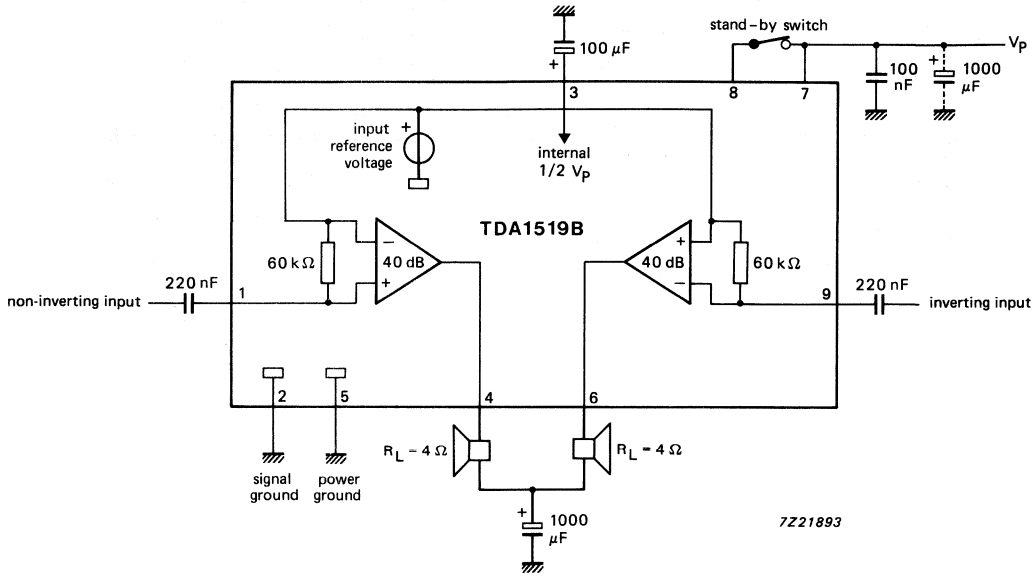


Fig.3 Stereo application circuit diagram.

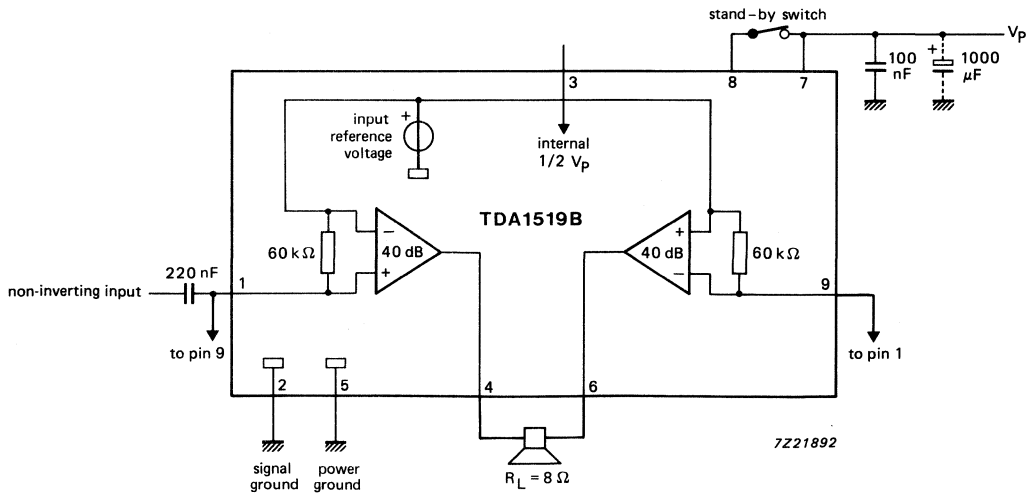


Fig.4 BTL application circuit diagram.

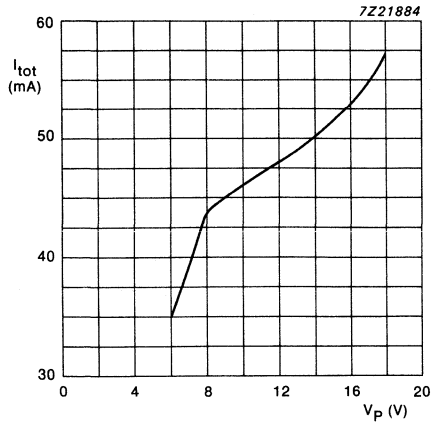


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

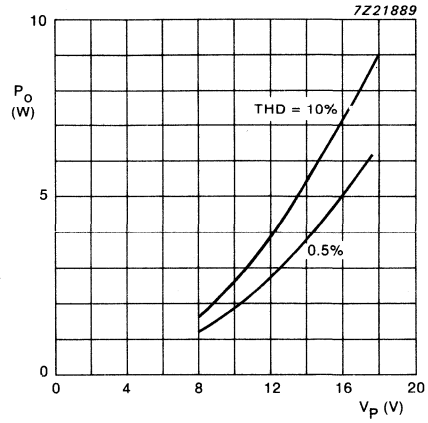


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

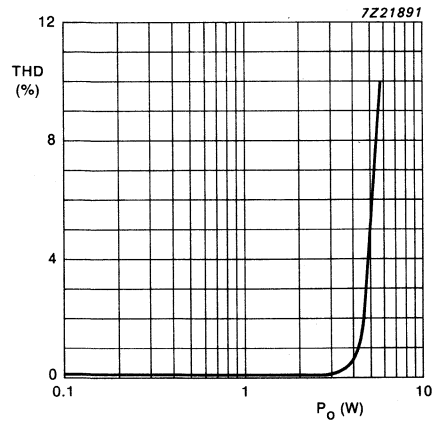


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

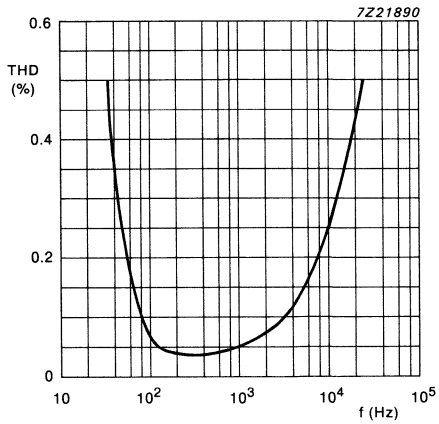


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for stereo application at $R_L = 4\ \Omega$, $P_o = 1$ W.

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520B is an integrated hi-fi audio power amplifier designed for use with non-stabilized symmetrical or stabilized asymmetrical power supplies in mains-fed applications (e.g. stereo radio, stereo TV sound and cassette recorder).

Features

- Low offset voltage at output (suitable for BTL application)
- Low cross-over and secondary cross-over distortion
- Low intermodulation and transient intermodulation distortion
- Low harmonic distortion
- Good hum suppression
- High slew rate
- No switch-on/switch-off plop
- Thermal protection

QUICK REFERENCE DATA (note 1)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_{tot}	22	60	105	mA
Output power at THD = 0,5%		P_o	20	22	–	W
Input impedance		Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O = 50 mW	note 2	(S+N)/N	70	75	–	dB
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB

Notes to the Quick Reference Data

1. All values measured from test circuit Fig.6; V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.
2. Bandwidth is 20 Hz to 20 kHz; R_S = 2 kΩ (RMS value).

PACKAGE OUTLINES

TDA1520B: 9-lead SIL; plastic power (SOT131).
TDA1520BQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

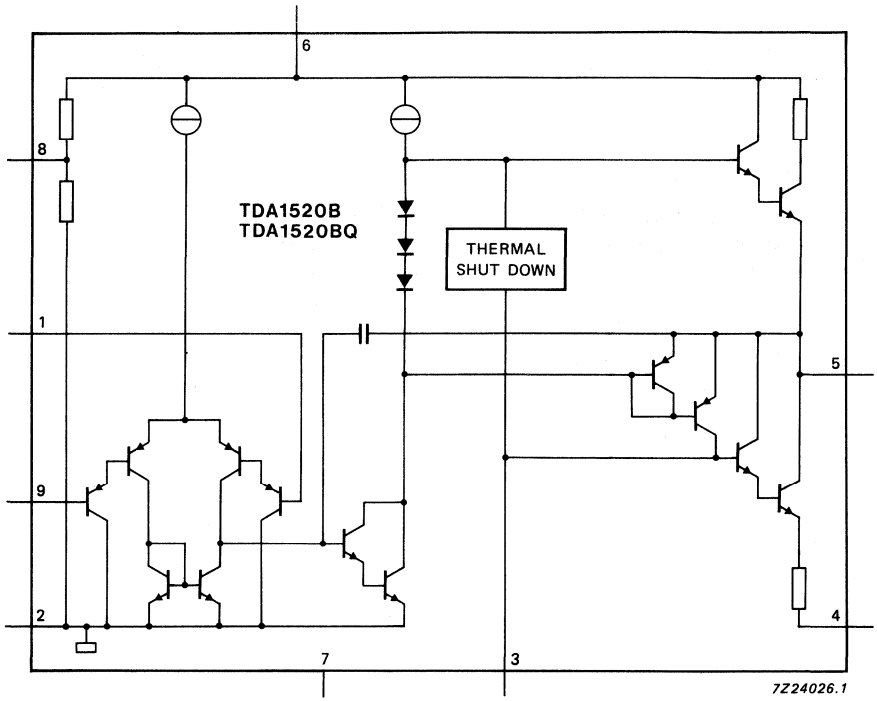


Fig. 1 Block diagram.

PINNING

1 Non-inverting input
2 Input ground (substrate)
3 Compensation
4 Negative supply (ground)
5 Output
6 Positive supply (V_P)
7 Not connected
8 Supply voltage ripple rejection
9 Inverting input (feedback)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	note 1	V_P	–	50	V
Input voltage					
pins 1 to 2		V_I	–	25	V
pins 9 to 2		V_I	–	25	V
Repetitive peak output current		I_{ORM}	–	4	A
Non-repetitive peak output current	note 2	I_{OSM}	–	5	A
Total power dissipation		P_{tot}	see Fig.2		
AC short-circuit time of the load impedance during signal drive at					
$V_P = \pm 20$ V	symmetrical supply; $R_S = 2\ \Omega$; $f = \geqslant 20$ Hz	T_{sc}	–	1	hour
$V_P = 30$ V	asymmetrical supply; $R_S = 4\ \Omega$	T_s	–	1	hour
Operating ambient temperature range		T_{amb}	see Fig.2		
Storage temperature range		T_{stg}	−55	+ 150	°C

Notes to the Ratings

1. Minimum rise time of the supply must be $\geqslant 20$ ms.
2. Maximum peak current is defined by the internal protection circuits.

POWER DISSIPATION AND HEATSINK INFORMATION

The maximum theoretical power dissipation with a stabilized power supply is ($V_P = 33$ V and $R_L = 4\ \Omega$):

$$\frac{V_P^2}{2\pi^2 R_L} = 13.8\ \text{W}.$$

Worst case power dissipation with a non-stabilized power supply is (regulation factor of 15%; over voltage of 10% and R_L min. = 0.8 x R_L typ.; V_{PL} is the loaded supply voltage):

$$\frac{(1.1 \times V_{PL})^2}{2\pi^2 R_{L\,\text{min.}}} = 23.4\ \text{W}.$$

With a maximum ambient temperature of 50 °C and a maximum crystal temperature of 150 °C, the required thermal resistance is:

$$R_{th\,j\text{-}a} = \frac{150 - 50}{23.4} = 4.3\ \text{K/W}.$$

The thermal resistance of the encapsulation is $\leqslant 2.5$ K/W, therefore the thermal resistance of the heatsink must be < 1.8 K/W.

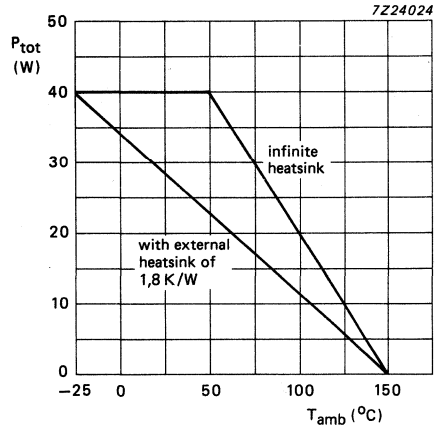


Fig.2 Power derating curve.

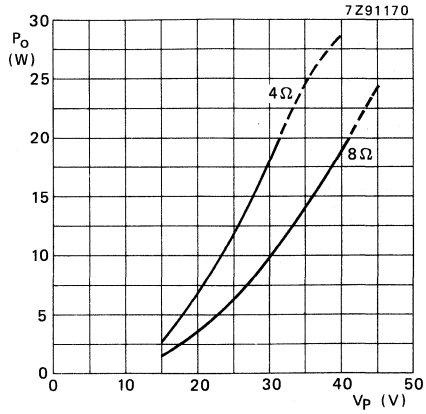


Fig. 3 Output power (P_O) as a function of supply voltage (V_P); f = 1 kHz; d_{tot} = 0.5%; G_V = 30 dB.

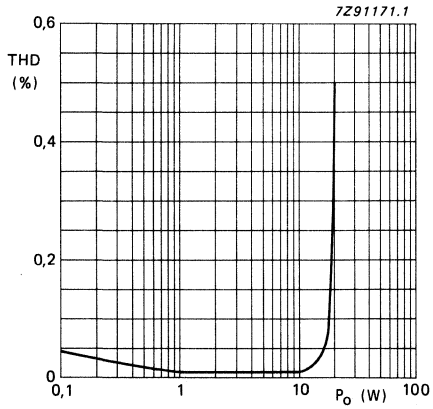


Fig. 4 Total harmonic distortion (THD) as a function of output power (P_O); V_P = 33 V; R_L = 4 Ω; f = 1 kHz.

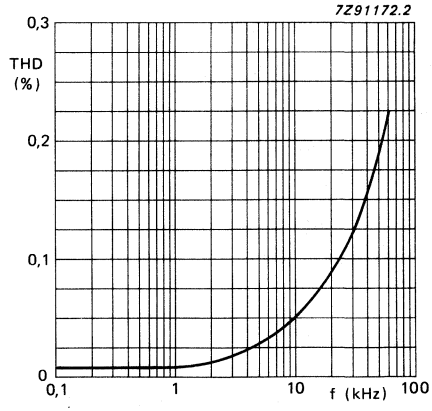


Fig. 5 Total harmonic distortion (THD) as a function of operating frequency (f); V_P = 33 V; R_L = 4 Ω; P_O = 10 W (constant).

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_P	22	60	105	mA
Peak output current		I_{OM}	–	–	3,2	A
Power output at THD = 0.5%	note 1	P_O	20	22	–	W
Total harmonic distortion at P_O = 12 W	note 1	THD	–	0.01	0.1	%
Power bandwidth at THD = 0.5%	P_O = 50 mW to 10 W	B	–	20 to 20 000	–	Hz
Input voltage at P_O = 20 W	note 2	V_I	225	290	325	mV
Input impedance	note 3	Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O at 50 mW	note 4	(S+N)/N	70	75	–	dB
Offset voltage		$\lvert V_{5\text{-}8} \rvert$	0	± 10	± 100	mV
Input offset current		I_{os}	–	0	1	μA
Output impedance		Z_O	–	–	0.1	Ω
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB
Intermodulation distortion at P_O = 10 W		d_{IM}	–	0.02	–	%
Transient intermodulation distortion	note 5	d_{TIM}	–	0.01	–	%
Slew rate		SR	–	6	–	V/μs

Notes to the Characteristics

1. Output power is measured directly at the output pin.
2. The closed-loop gain is determined by external resistors and is variable between 20 to 40 dB.
3. Input impedance in the test circuit is determined by the bias resistor R.
4. Unweighted noise measured in a bandwidth of 20 Hz to 20 kHz at R_S = 2 kΩ.
5. The transient intermodulation distortion is measured at P_O = 10 W. The input signal is a 3.18 kHz square-wave signal mixed with a 15 kHz sine-wave signal and a peak-to-peak voltage ratio of 4:1.

APPLICATION INFORMATION

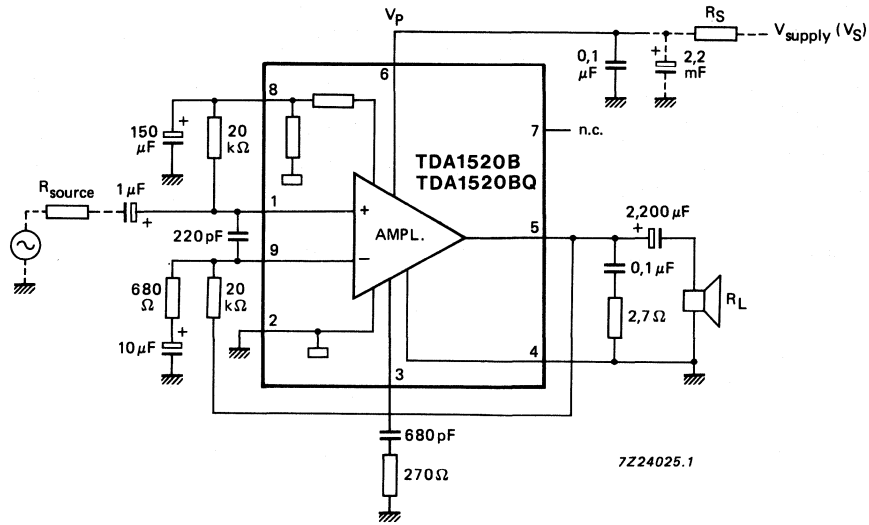


Fig. 6 Test and application diagram.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_O	typ. 12	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

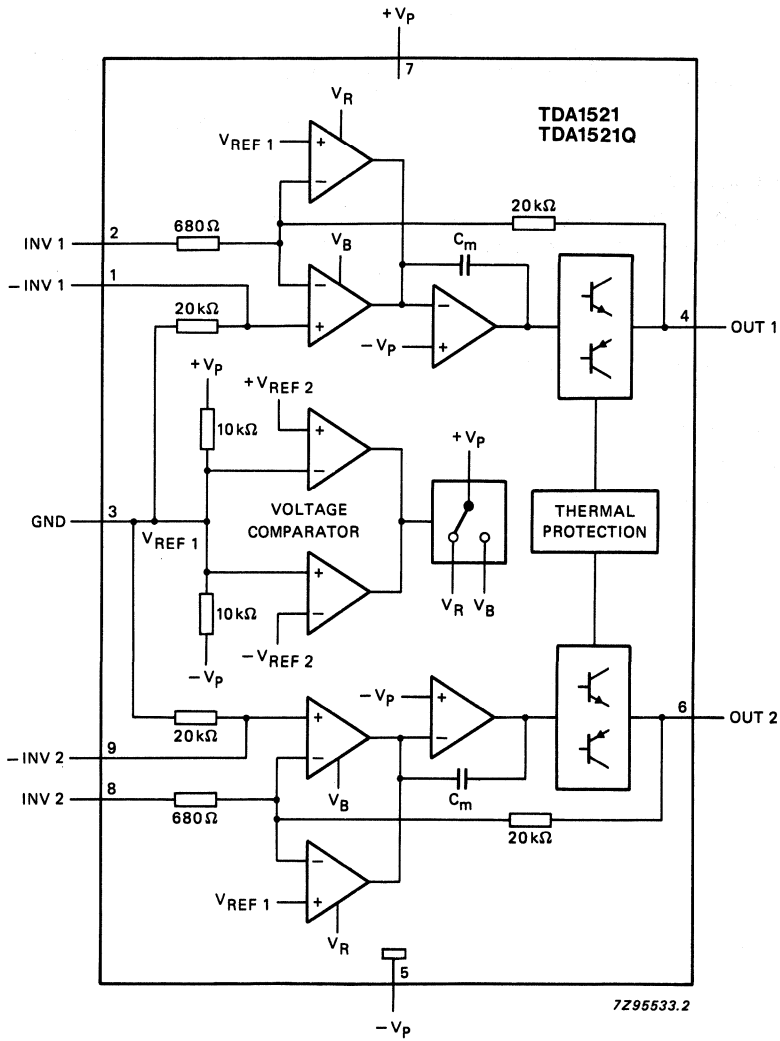


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	–20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

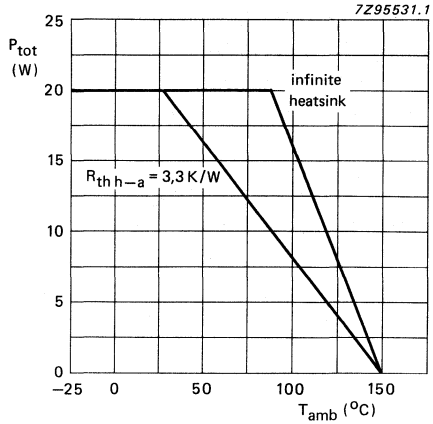


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ = 2,5 K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 16$ V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14{,}6} - 2{,}5 = 3{,}3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_P$)

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\,max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

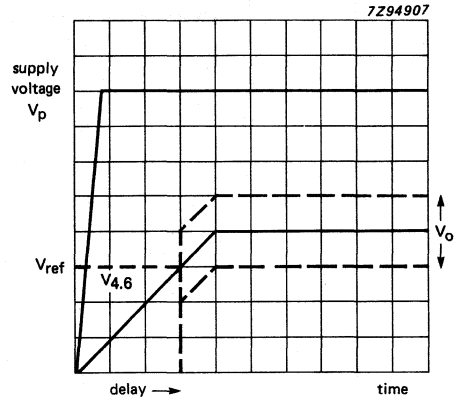


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

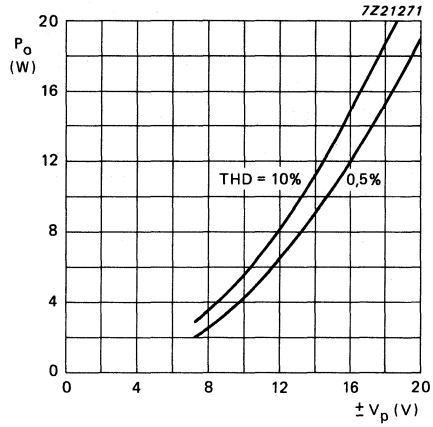


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

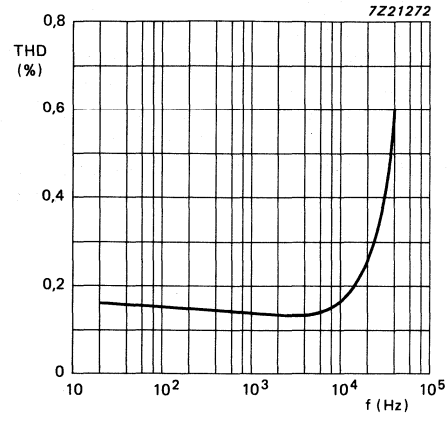


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_O = 6$ W.

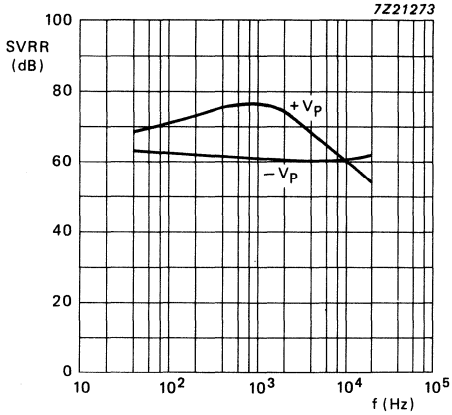


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

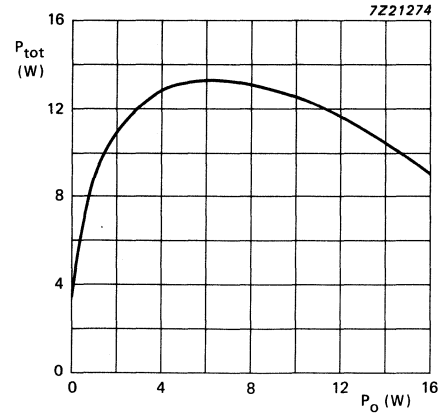


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

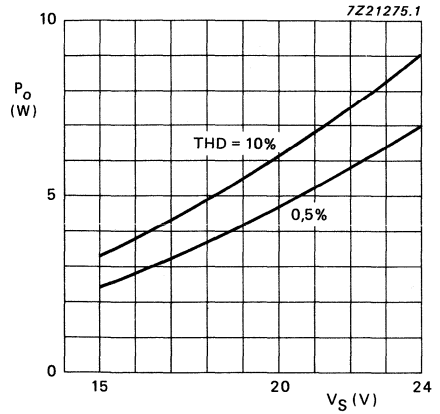


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

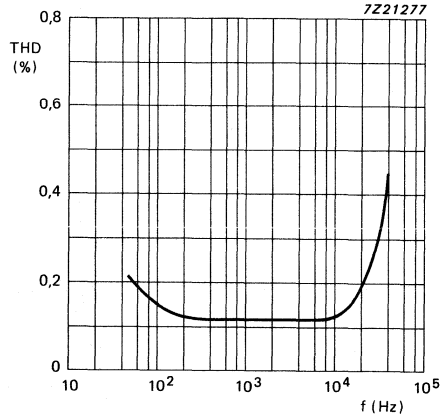


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 4$ W.

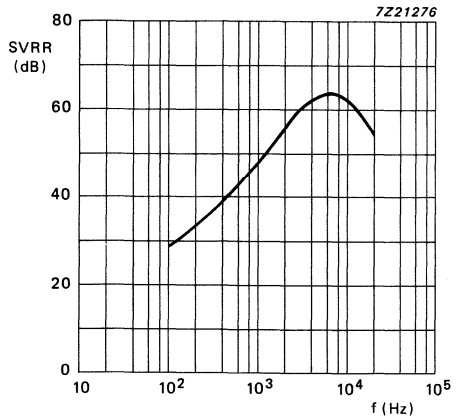


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

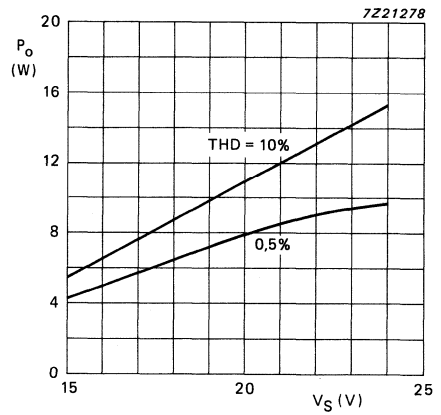
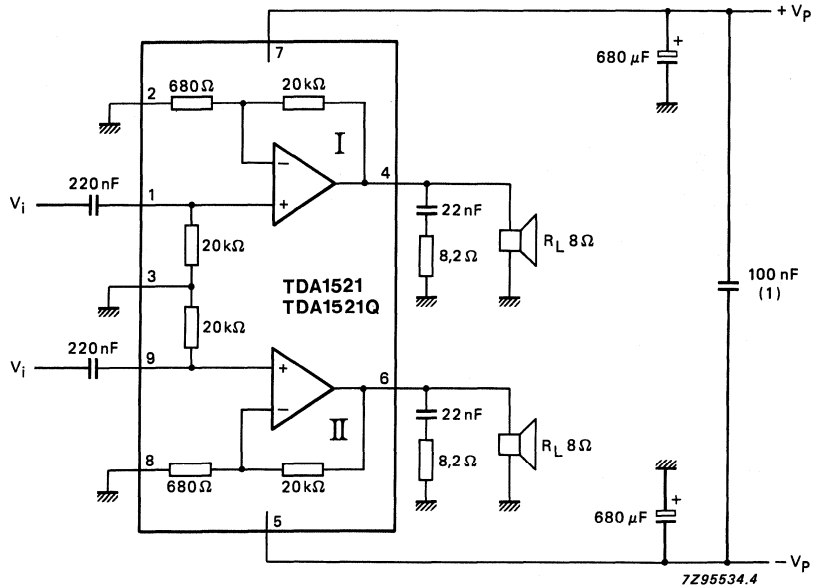
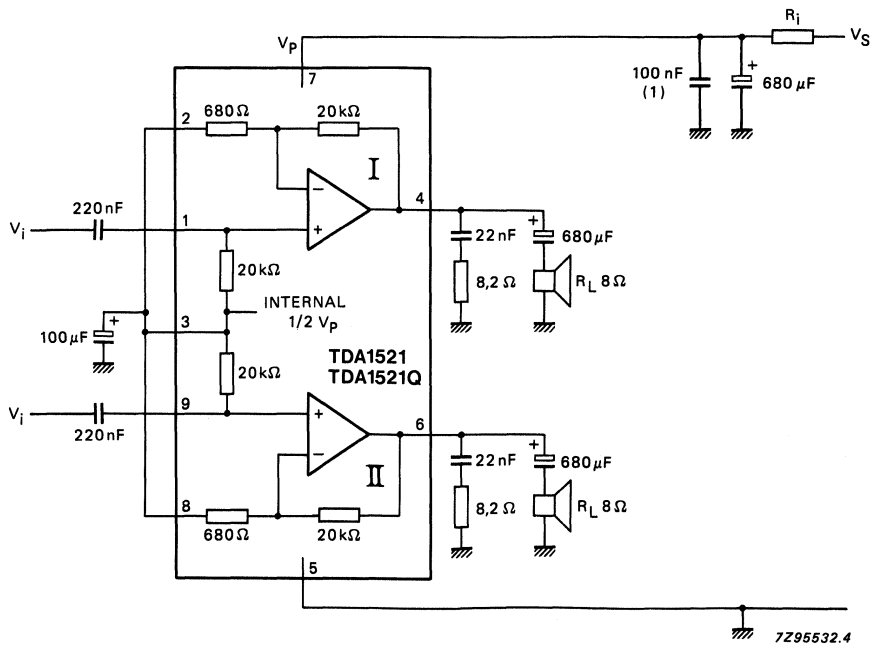


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4\ \Omega$; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

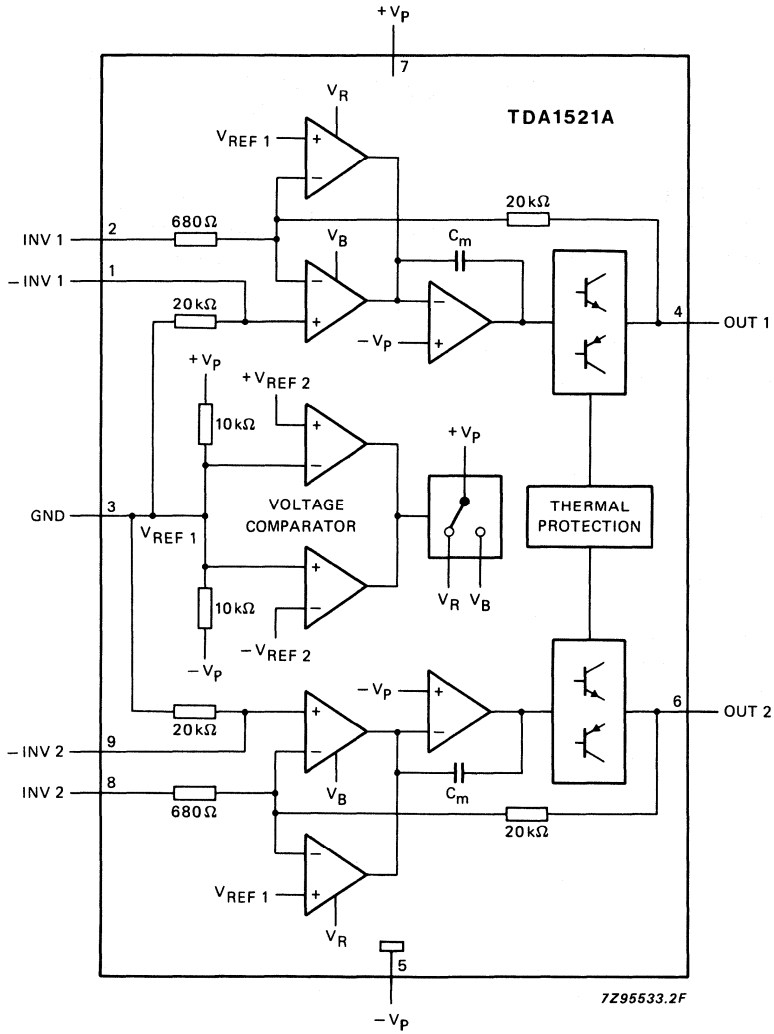


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

DEVELOPMENT DATA

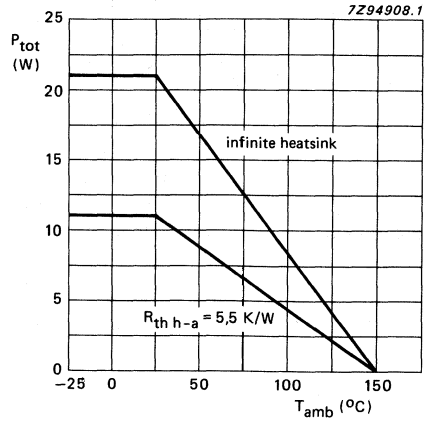


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz;
   ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

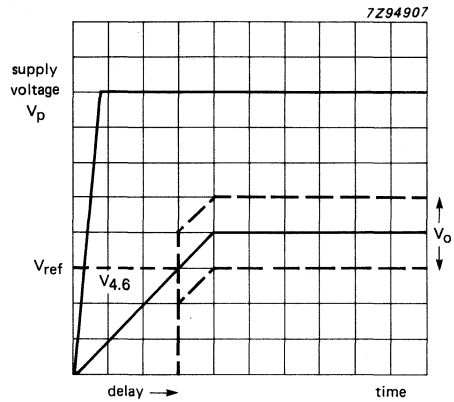


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

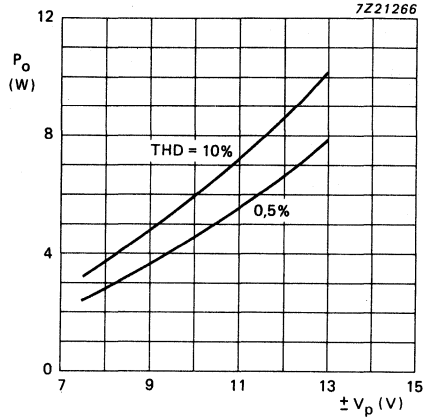


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

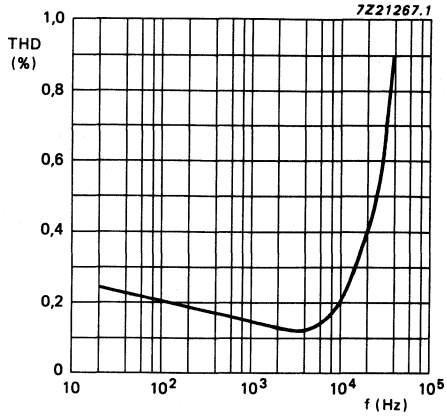


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_p = \pm 12$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

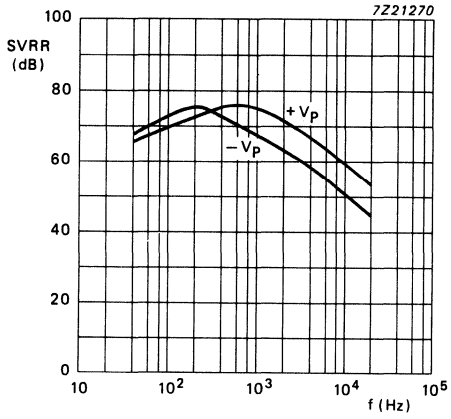


Fig. 6 Supply voltage ripple rejection; symmetrical supply, $V_P = \pm 12$ V; $V_{RR} = 200$ mV.

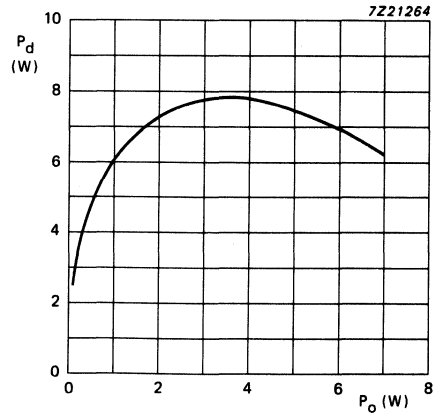


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; f = 1 kHz.

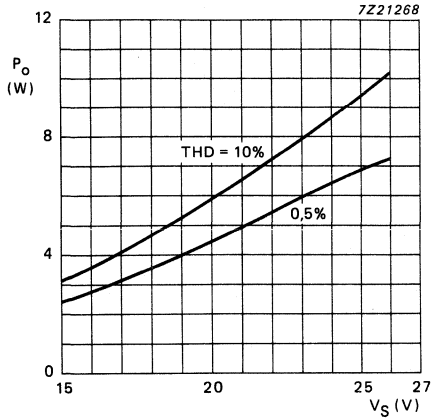


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

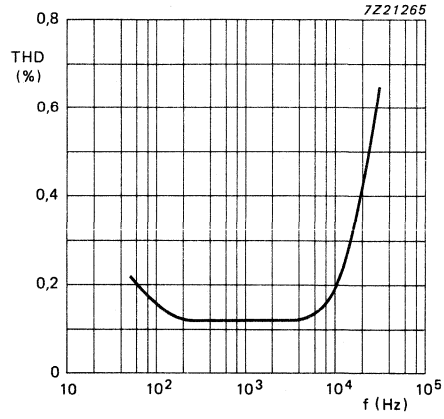


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

DEVELOPMENT DATA

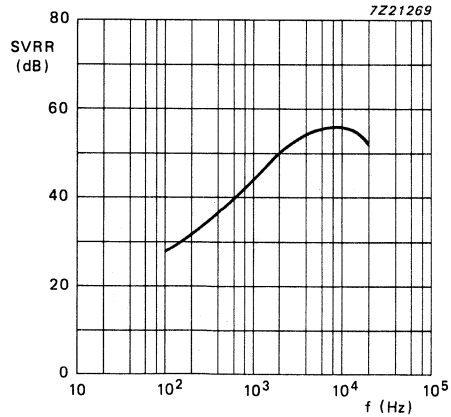
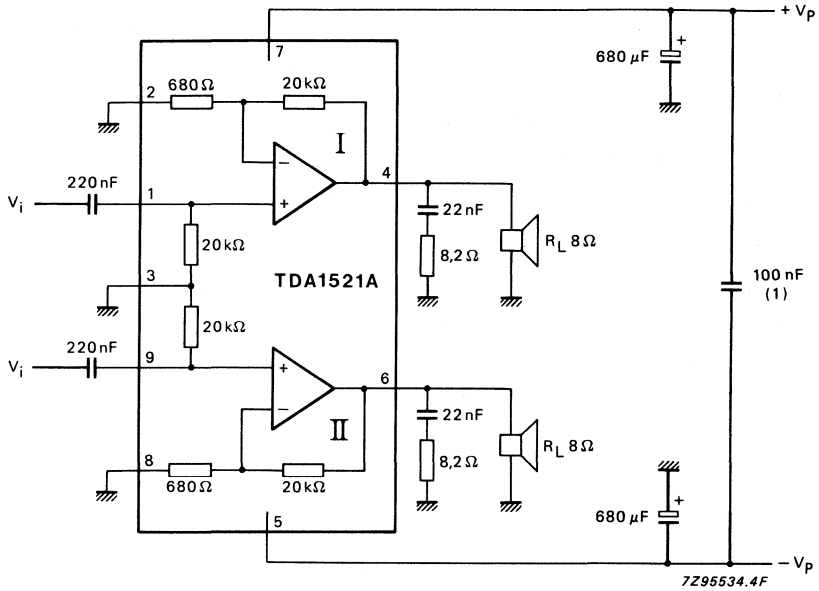


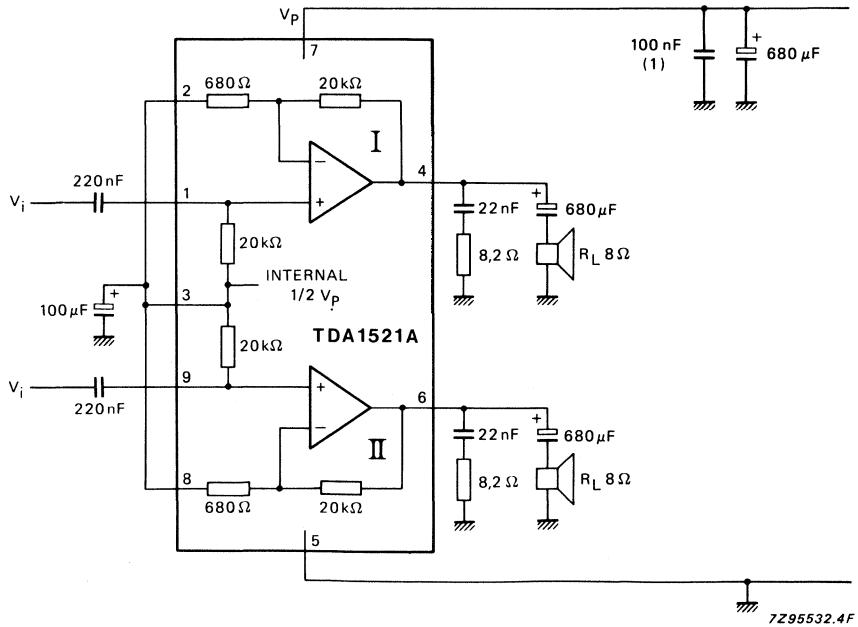
Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

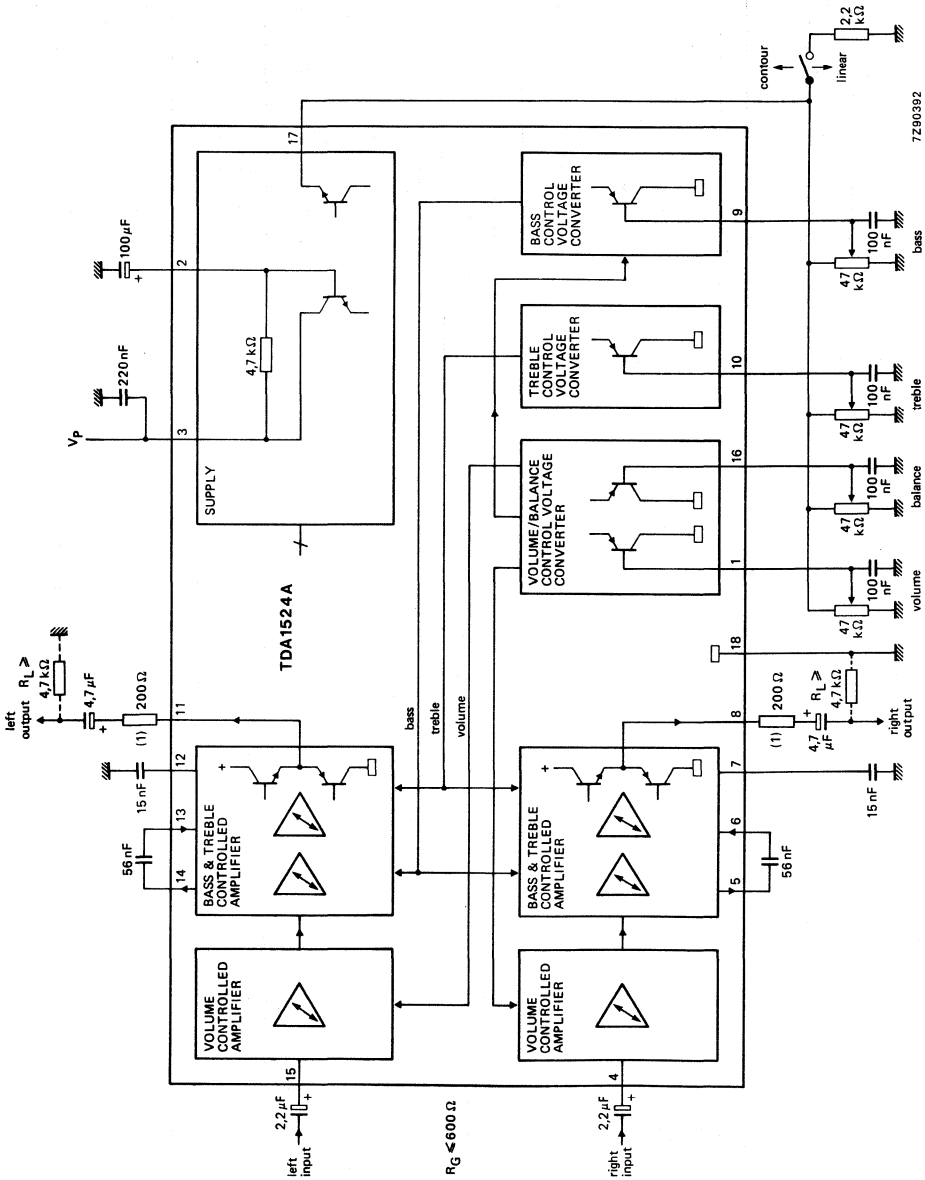
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_V		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_V		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_V	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_V = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_V = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_V = −20 to + 26 dB	ΔG_V	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

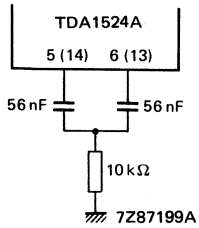


Fig. 2 Double-pole low-pass filter for improved bass-boost.

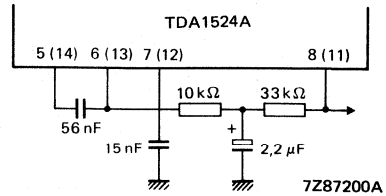


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3-18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at V_P = 8,5 V	$I_P = I_3$	19	27	35	mA
at V_P = 12 V	$I_P = I_3$	25	35	45	mA
at V_P = 15 V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at V_P = 8,5 V	$V_{4,15-18}$	3,8	4,25	4,7	V
at V_P = 12 V	$V_{4,15-18}$	5,3	5,9	6,6	V
at V_P = 15 V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at V_P = 8,5 V	$V_{8,11-18}$	3,3	4,25	5,2	V
at V_P = 12 V	$V_{8,11-18}$	4,6	6,0	7,4	V
at V_P = 15 V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at V_P = 8,5 V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at V_{17-18} = 5 V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\,max}$	20,5	21,5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to −26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = –3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = –40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = –16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = –40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

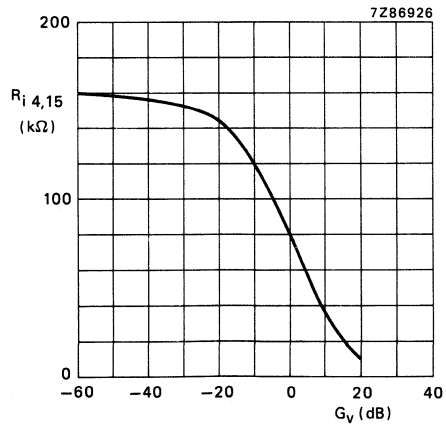


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

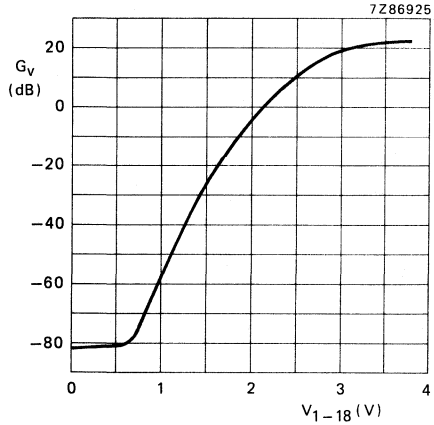


Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

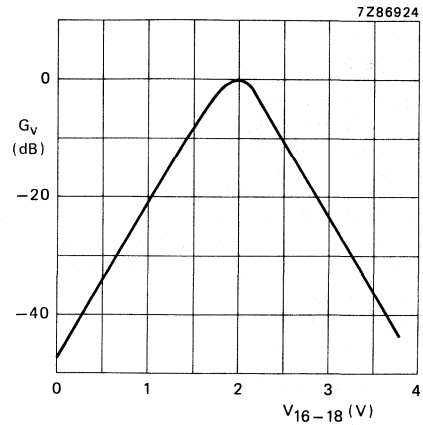


Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

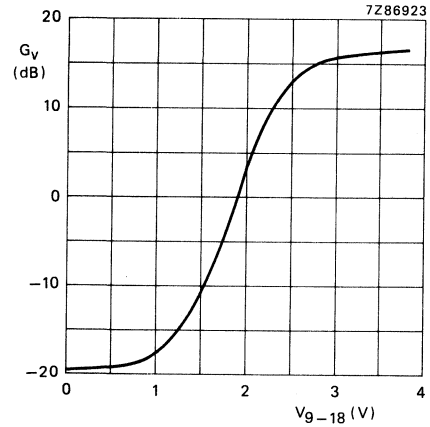


Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

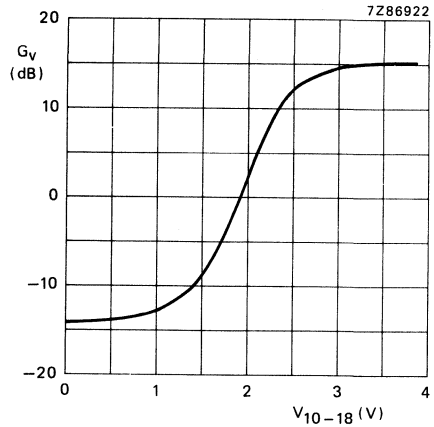


Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

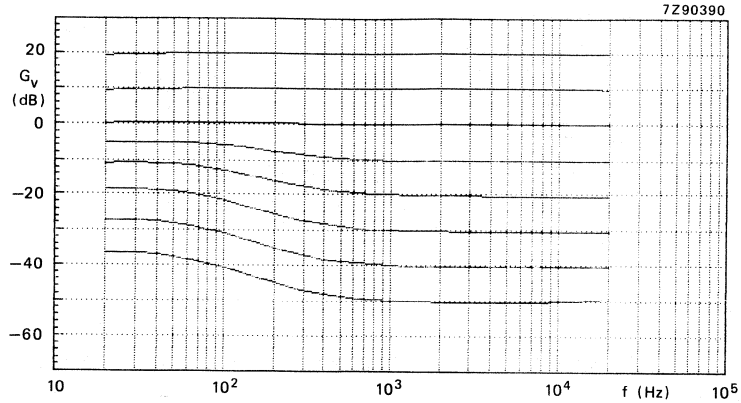


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

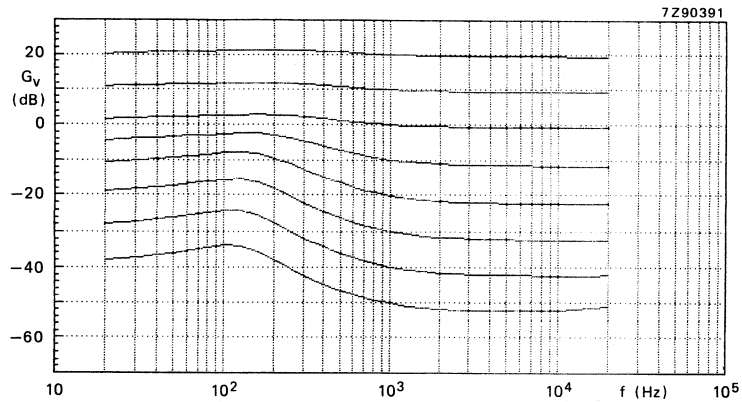


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

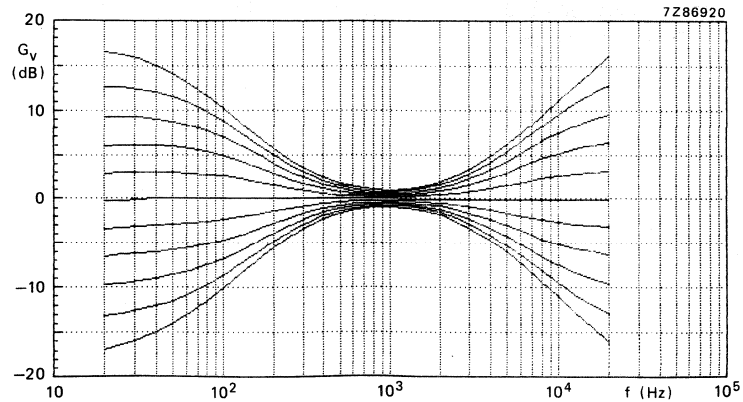


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

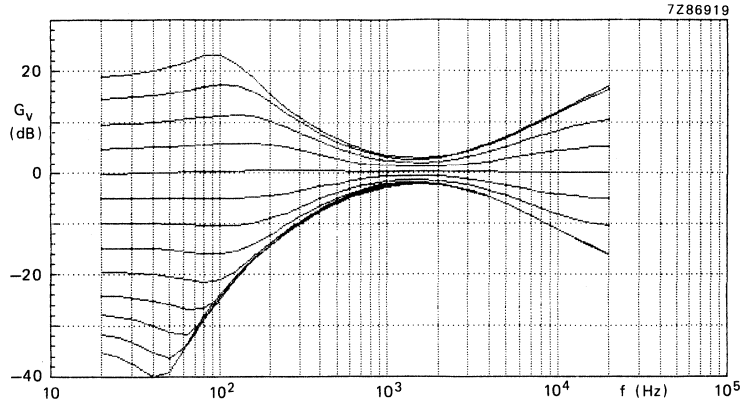


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

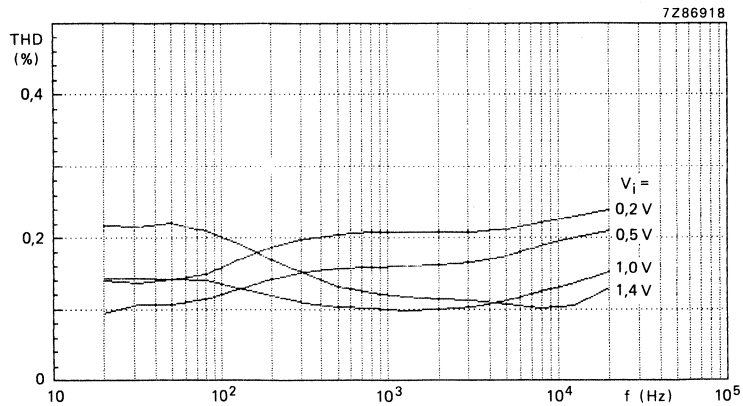


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

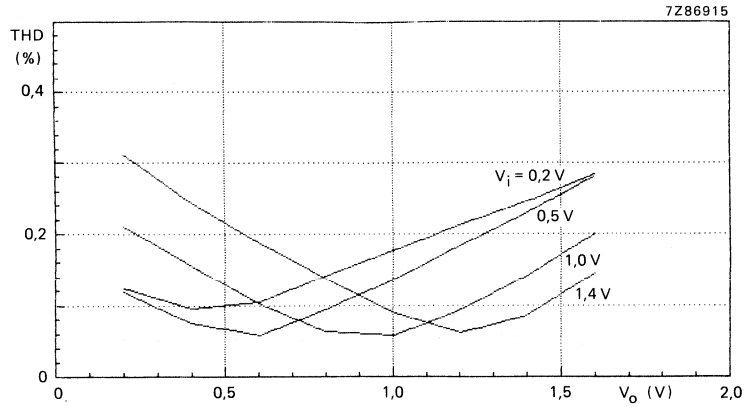
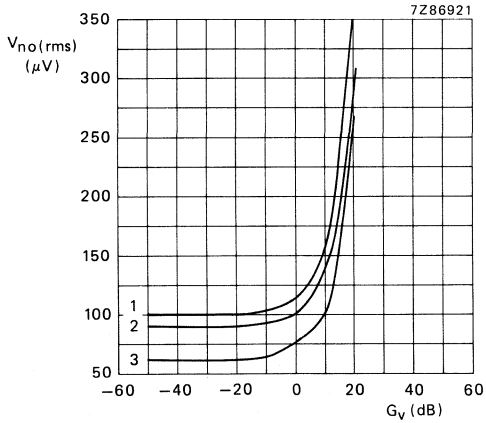


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

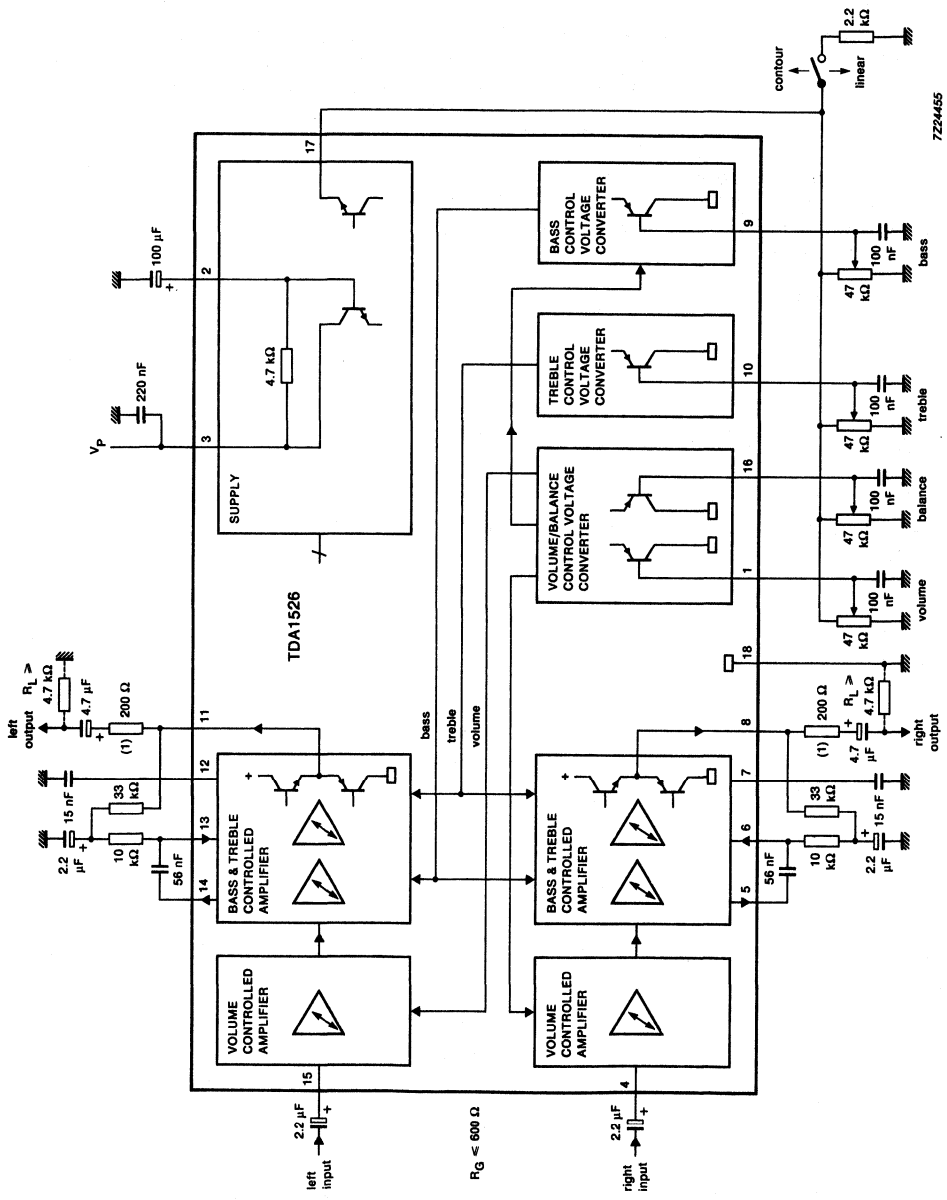
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range	$G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range	G_V = 0 dB; see Fig. 5	ΔG_V	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_V	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_V	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_V = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_V = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels	f = 250 Hz to 6.3 kHz; balance at G_V = 10 dB					
for G_V = 21.5 to –26 dB		ΔG_V	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

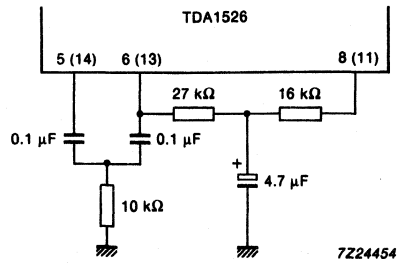


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–30	+ 80	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 5)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	–19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics			see Figs 9 and 10		
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = –40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz) at G_V = –20 to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage $V_{1-18} = 0.5\,V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0.5\,V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels for G_V = 21.5 to –26 dB f = 250 Hz to 6.3 kHz; balance adjusted at G_V = 10 dB	ΔG_V	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_v = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_v}; G_{v\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

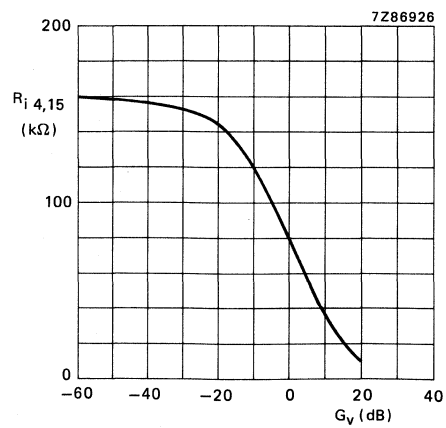


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_v). Measured in Fig.1.

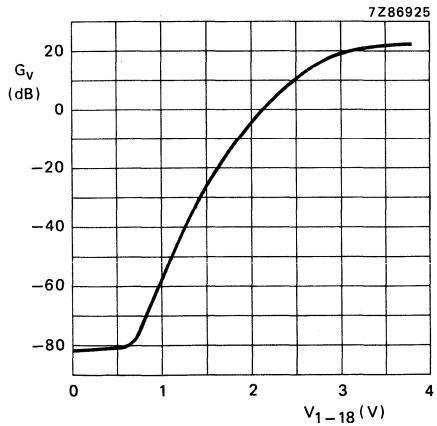


Fig.4 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

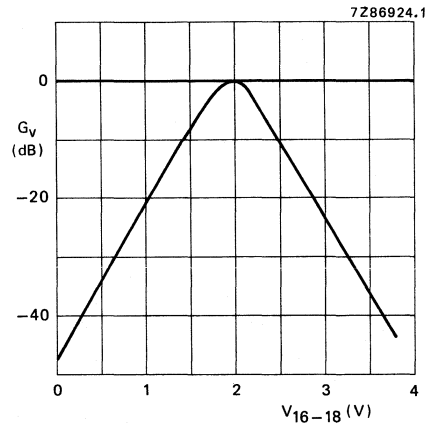


Fig.5 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

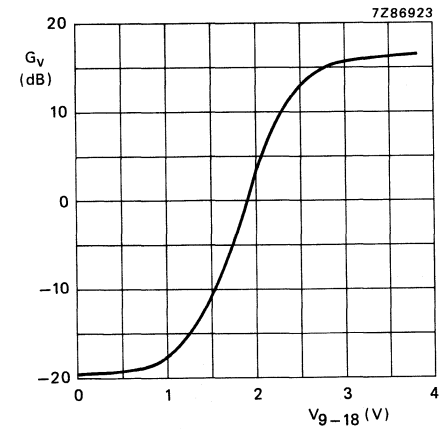


Fig.6 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

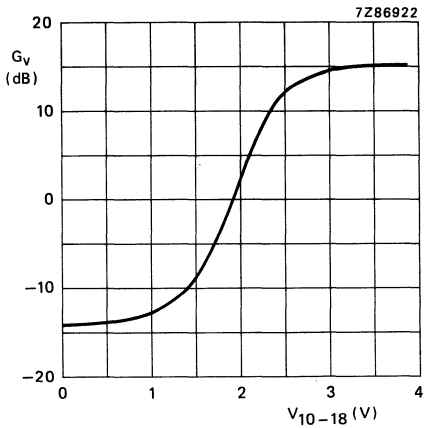


Fig.7 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

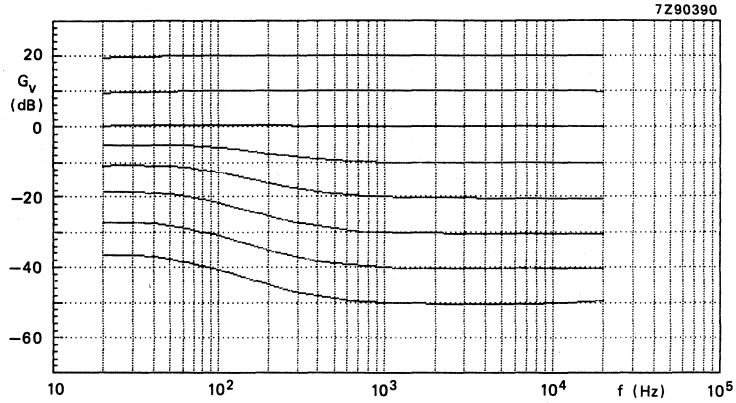


Fig.8 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

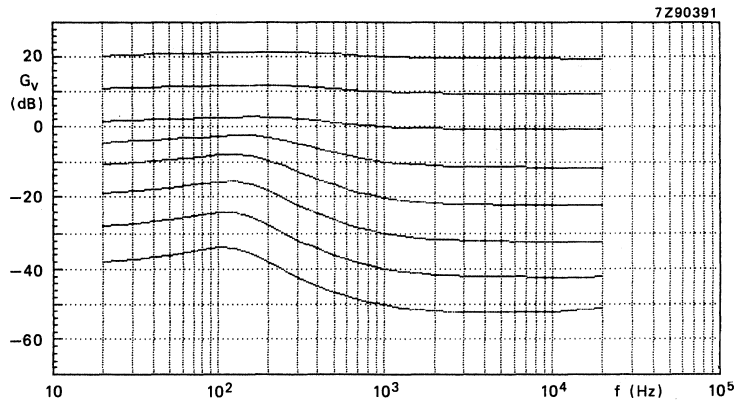


Fig.9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

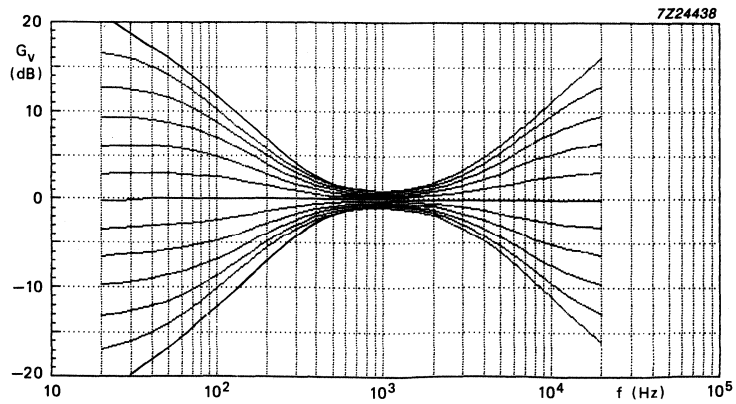


Fig.10 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

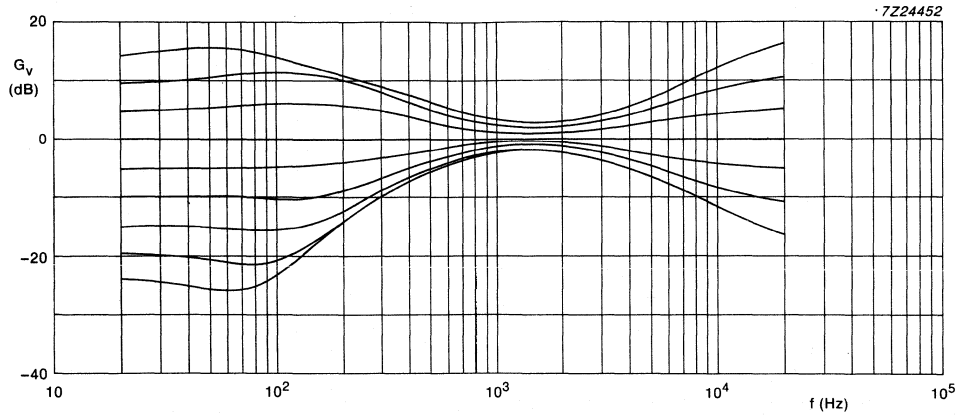


Fig.11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

DEVELOPMENT DATA

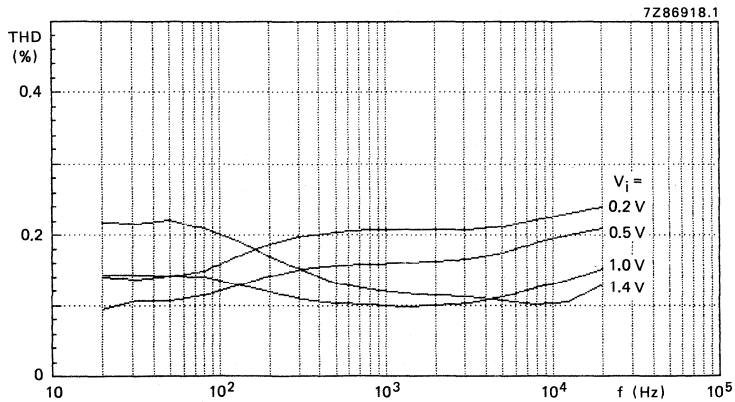


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

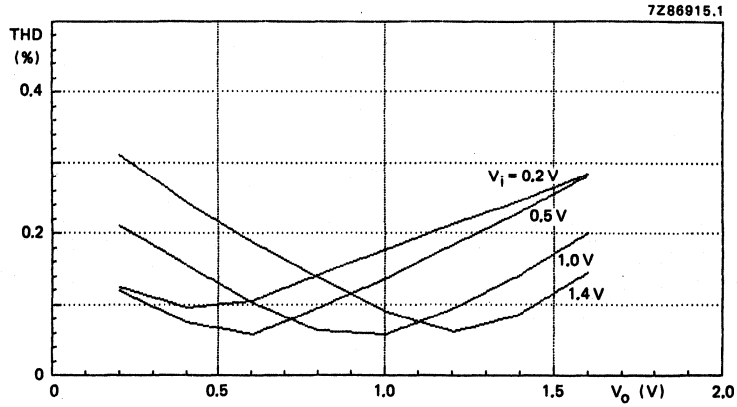


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

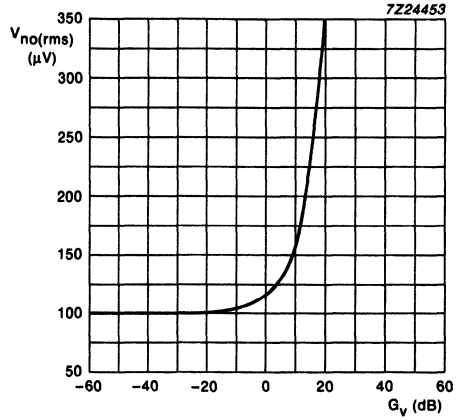


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time

QUICK REFERENCE DATA

Supply voltages			
pin 28	V_{DD}	typ.	5 V
pin 26	V_{DD1}	typ.	−5 V
pin 15	V_{DD2}	typ.	−15 V
Supply currents			
pin 28	I_{DD}	typ.	45 mA
pin 26	I_{DD1}	typ.	45 mA
pin 15	I_{DD2}	typ.	25 mA
Signal-to-noise ratio (full scale sine-wave) at analogue outputs (AOL; AOR)	S/N	typ.	95 dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB
Current settling time to ± 1 LSB	t_{cs}	typ.	1 μs
Maximum input bit rate at data input (pin 3)	BR_{max}	min.	6 Mbits/s
Maximum clock frequency			
at clock input (pin 2)	f_{BCKmax}	min.	6 MHz
at clock input (pin 4)	f_{SCKmax}	min.	12 MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	typ.	± 200 x 10^{-6} K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Total power dissipation	P_{tot}	typ.	850 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117).

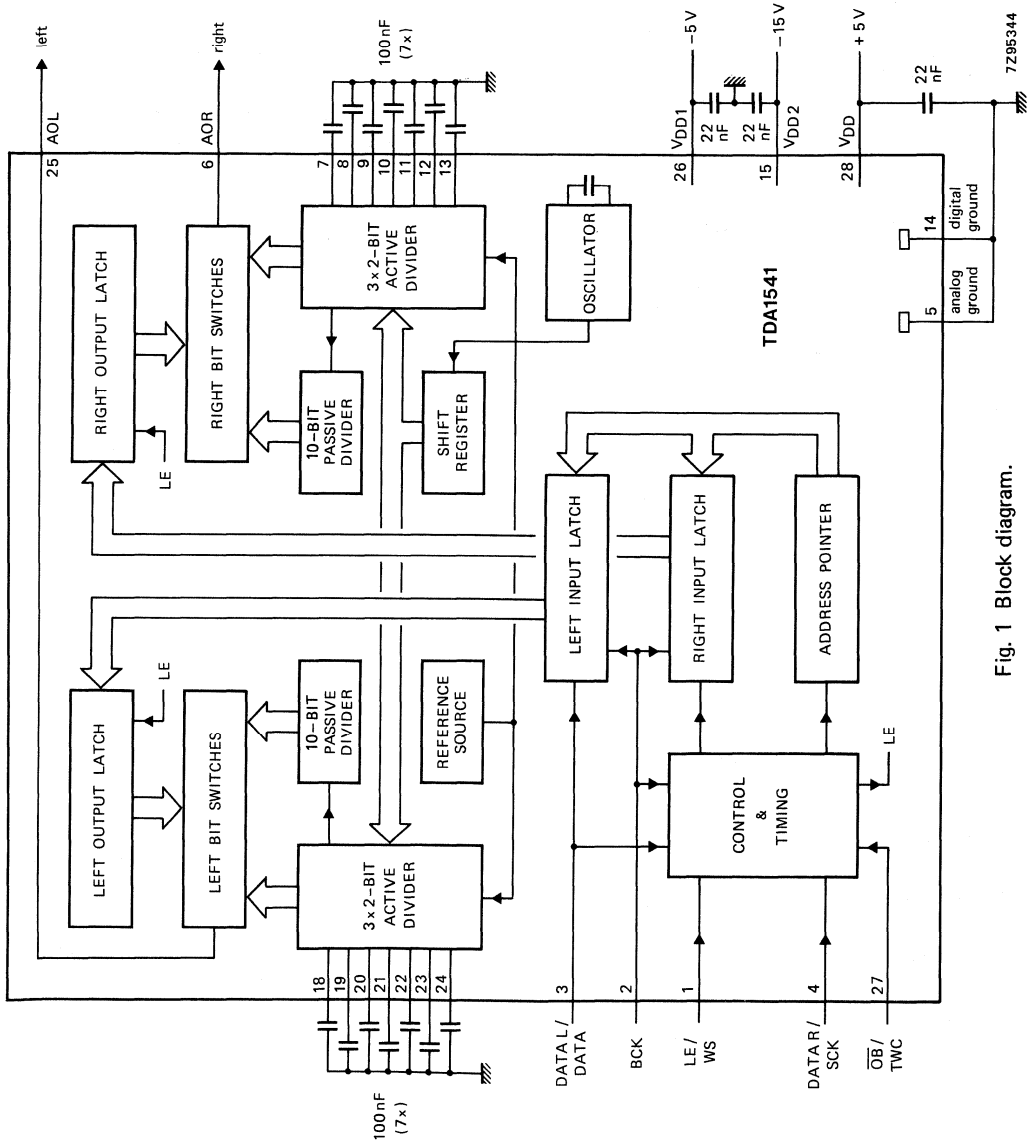


Fig. 1 Block diagram.

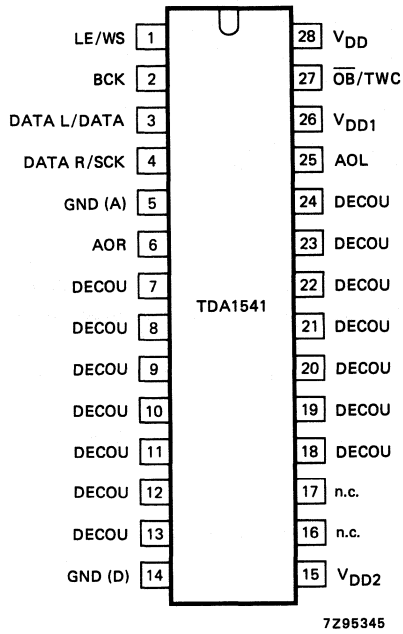


Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input / word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input / data input (selected format)
4	DATA R/SYS*	data right channel input / system clock input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	n.c.	not connected
17	n.c.	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

FUNCTIONAL DESCRIPTION

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analogue outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary.

The format of data input signals is shown in figures 3, 4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	SCK
+5 V	time MUX TWC	WS	BCK	DATA TWC	SCK

Where:

LE = latch enable
WS = word select
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges		
pin 28	V_{DD}	0 to + 7 V
pin 26	V_{DD1}	0 to −7 V
pin 15	V_{DD2}	0 to −17 V
Crystal temperature range	T_{XTAL}	−55 to + 150 °C
Storage temperature range	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Electrostatic handling*	V_{es}	−1000 to + 1000 V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	35 K/W

* Discharging a 250 pF capacitor through a 1 kΩ series resistor.

CHARACTERISTICS

V_{DD} = + 5 V; V_{DD1} = −5 V; V_{DD2} = −12 V; T_{amb} = + 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage ranges					
pin 28	V_{DD}	4,0	5,0	6,0	V
pin 26	$-V_{DD1}$	4,5	5,0	6,0	V
pin 15	$-V_{DD2}$	14	15	16	V
Supply currents					
pin 28	I_{DD}	–	45	tbf	mA
pin 26	$-I_{DD1}$	–	45	tbf	mA
pin 15	$-I_{DD2}$	–	25	tbf	mA
Resolution	Res	–	16	–	bits
Inputs					
Input current (pin 3 and pin 4)					
digital inputs LOW (< 0,8 V)	I_{IL}	–	–	tbf	mA
digital inputs HIGH (> 2,0 V)	I_{IH}	–	–	tbf	µA
Input frequency					
at clock input (pin 4)	f_{SCK}	–	–	12	MHz
at clock input (pin 2)	f_{BCK}	–	–	6	MHz
at data inputs (pin 3 and pin 4)	f_{DAT}	–	–	6	MHz
at word select input (pin 1)	f_{WS}	–	–	200	kHz
Input capacitance of digital inputs	C_I	–	12	–	pF
Oscillator					
Oscillator frequency with internal capacitor	f_{osc}	150	200	250	kHz
Analogue outputs (AOL; AOR)					
Output voltage compliance	V_{OC}	tbf	–	tbf	mV
Full scale current	I_{FS}	3,4	4,0	4,6	mA
Zero scale current	$\pm I_{ZS}$	–	tbf	–	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 200 \times 10^{-6}$	–	K^{-1}
Linearity error integral					
at T_{amb} = 25 °C	E_1	–	0,5	–	LSB
at T_{amb} = −20 to + 70 °C	E_1	–	tbf	–	LSB
Linearity error differential					
at T_{amb} = 25 °C	E_{d1}	–	0,5	1	LSB
at T_{amb} = −20 to + 70 °C	E_{d1}	–	tbf	–	LSB

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio + THD*	S/N	90	95	–	dB
Settling time to ± 1 LSB	t_{cs}	–	1	–	μs
Channel separation	α	80	tbf	–	dB
Unbalance between outputs	ΔI_{FS}	–	0,1	0,2	dB
Time delay between outputs	t_d	–	–	1	μs
Power supply ripple rejection**					
V_{DD} = + 5 V	RR	–	tbf	–	dB
V_{DD1} = –5 V	RR	–	tbf	–	dB
V_{DD2} = –15 V	RR	–	tbf	–	dB
Signal-to-noise ratio at bipolar zero	S/N	–	–100	–	dB
Timing (see Figs 3, 4 and 5)					
Rise time	t_r	–	–	35	ns
Fall time	t_f	–	–	35	ns
Bit clock cycle time	t_{CY}	160	–	–	ns
Bit clock HIGH time	t_{HB}	48	–	–	ns
Bit clock LOW time	t_{LB}	48	–	–	ns
Bit clock fall time to latch rise time	t_{FBRL}	0	–	–	ns
Bit clock rise time to latch fall time	t_{RBFL}	0	–	–	ns
Data set-up time to bit clock	t_{SDB}	32	–	–	ns
Data hold time to bit clock	t_{HDB}	0	–	–	ns
Data set-up time to system clock	t_{SDS}	32	–	–	ns
Word select hold time to system clock	t_{HWS}	0	–	–	ns
Word select set-up time to system clock	t_{SWS}	32	–	–	ns
Bit clock fall time to system clock rise time	t_{FBRS}	32	–	–	ns
System clock rise time to bit clock fall time	t_{RSFB}	32	–	–	ns
System clock fall time to bit clock rise time	t_{FSRB}	50	–	–	ns
Bit clock rise time to system clock fall time	t_{RBFS}	0	–	–	ns
Latch enable LOW time	t_{LLE}	20	–	–	ns
Latch enable HIGH time	t_{HLE}	32	–	–	ns

* Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.

** V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

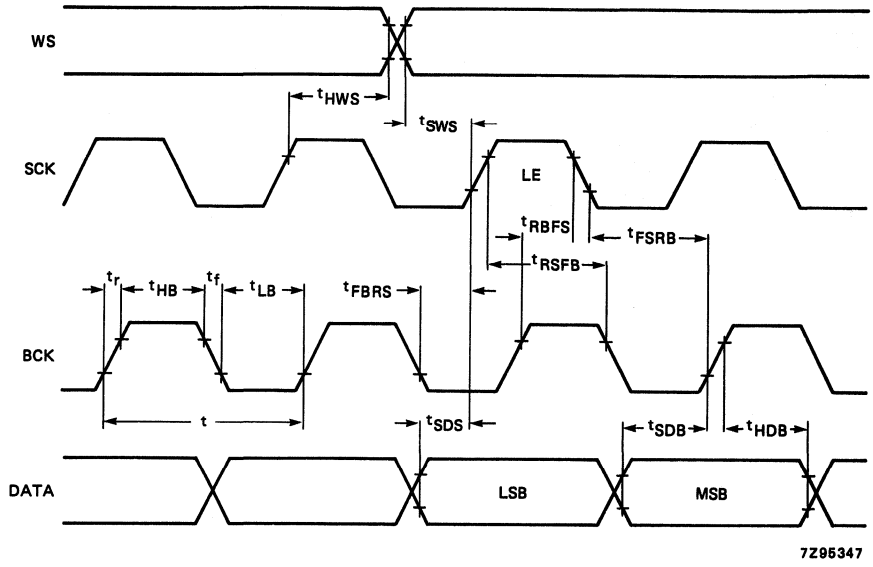


Fig. 3 Format of input signals; time multiplexed at $f_{SCK} = f_{BCK}$ (I^2S format).

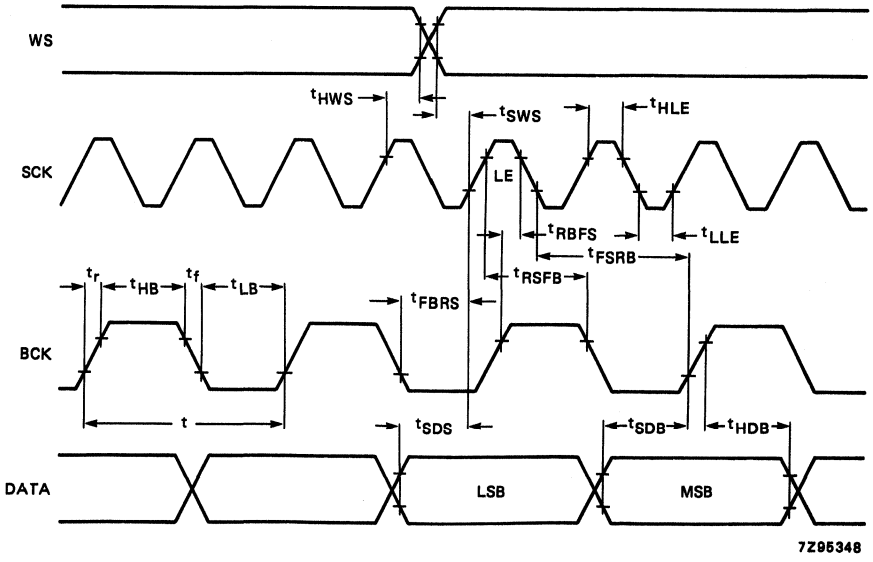


Fig. 4 Format of input signals; **time multiplexed** at $f_{SCK} = 2 \times f_{BCK}$.

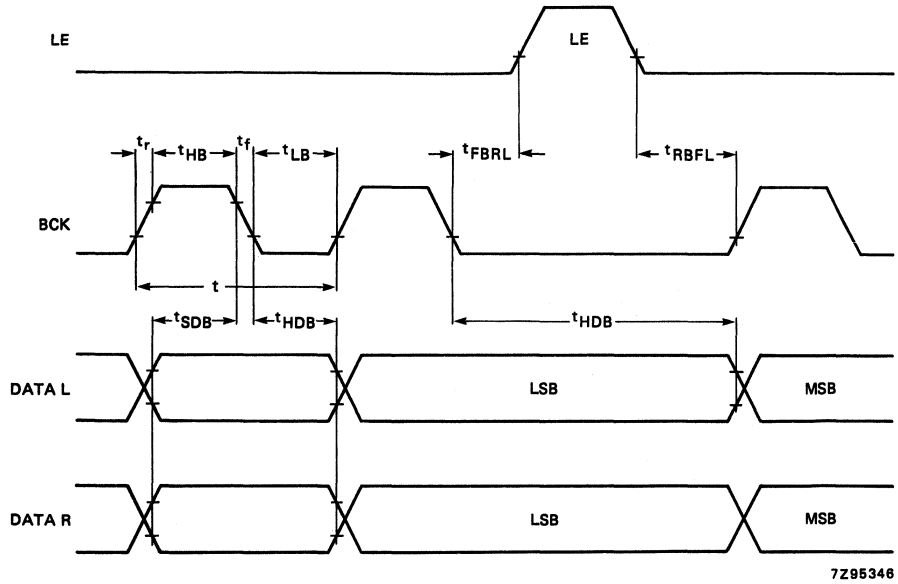


Fig. 5 Format of input signals; **simultaneous data.**

ACTIVE ELEMENT FOR POST FILTERING.

GENERAL DESCRIPTION

The TDA1542 is a dual channel monolithic integrated circuit encapsulated in a 28 pin DIL plastic package. Each channel incorporates five high performance amplifiers and is designed for use in hi-fi digital audio equipment such as a compact disc player.

Features

- Mute function for click and plop free switching (on and off)
- Switch function for activating a de-emphasis circuit
- Two separate output amplifiers per channel
- Flexible use of filtering
- Extremely low distortion
- High slew-rate input amplifier

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Input amplifier (A)						
Slew-rate		$\Delta V/\Delta t$	–	30	–	V/μs
Line amplifier (D)						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 1 kΩ	THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)		$V_{O(rms)}$	–	6	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Filter amplifiers (A, B and C)						
Amplifiers conform to line amplifier D, without mute function						

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

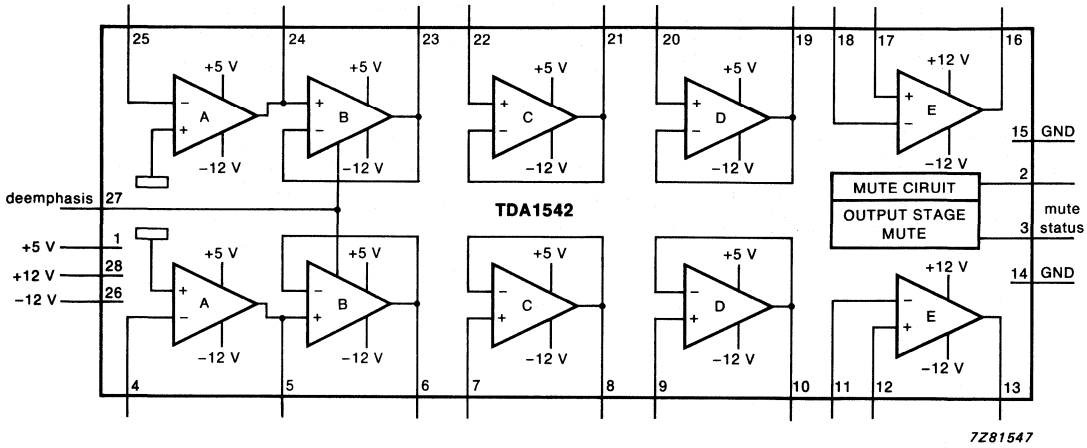


Fig. 1 Block diagram.

PINNING

1	+5 V supply voltage (V_{DD2})	15	Ground left
2	Mute timing capacitor	16	Amplifier E left output
3	Mute status	17	Amplifier E left non-inverting input
4	Amplifier A right input	18	Amplifier E left inverting input
5	Amplifier A right output/Amplifier B input	19	Amplifier D left output
6	Amplifier B right output	20	Amplifier D left input
7	Amplifier C right input	21	Amplifier C left output
8	Amplifier C right output	22	Amplifier C left input
9	Amplifier D right input	23	Amplifier B left output
10	Amplifier D right output	24	Amplifier A left output/Amplifier B input
11	Amplifier E right inverting input	25	Amplifier A left input
12	Amplifier E right non-inverting input	26	−12 V supply voltage (V_{DD3})
13	Amplifier E right output	27	De-emphasis on/off function
14	Ground right	28	+12 V supply voltage (V_{DD1})

FUNCTIONAL DESCRIPTION

The TDA1542 is a high performance, dual channel device designed to perform post filtering in a compact disc player. Since only the active part of the filter is integrated, the user has the option of selecting the desired filter type e.g. Bessel or Cauer etc. Each channel contains two separate output amplifiers, one with fixed gain for line output and the other with variable gain for driving low/high impedance headphones.

A switchable buffer amplifier is incorporated to enable the deemphasis function without producing clicks.

A mute circuit is incorporated to prevent spurious signals appearing at the output.

Both amplifiers are muted, for a preset period of time, when the 5 V supply is switched on or off. An external capacitor determines the mute time. When the mute time has elapsed the signal path is switched directly to the output, without clicks. The mute circuit status is available externally.

The TDA1542 is designed to operate over a wide supply voltage range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage ranges					
pin 28		V_{DD1}	0	18	V
pin 1		V_{DD2}	0	7	V
pin 26		$-V_{DD3}$	0	18	V
Storage temperature range		T_{stg}	−65	150	°C
Operating ambient temperature range		T_{amb}	−30	85	°C
Electrostatic handling *		V_{es}	−	600	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Supply current						
pin 28		I_{DD1}	–	12	18	mA
pin 1		I_{DD2}	–	34	51	mA
pin 26		$-I_{DD3}$	–	46	69	mA
Input current						
Amplifier A (pins 4 and 25)		I_{IA}	–	1	2	μA
Amplifier C (pins 7 and 22)		I_{IC}	–	320	600	nA
Amplifier D (pins 9 and 20)		I_{ID}	–	50	150	nA
Amplifier E (pins 11 and 18)		I_{IE}	–	300	600	nA
Amplifier E (pins 12 and 17)		I_{IE}	–	30	150	nA
Offset voltage						
Amplifier A (pins 4 and 25)		$\lvert V_{IAos}\rvert$	–	1.2	7.0	mV
Amplifier B (pins 6 and 23)		$\lvert V_{IBos}\rvert$	–	0.5	7.0	mV
Amplifier C (pins 8 and 21)		$\lvert V_{ICos}\rvert$	–	0.6	7.0	mV
Amplifier D (pins 10 and 19)		$\lvert V_{IDos}\rvert$	–	1.0	3.0	mV
Amplifier E (pins 11 and 18)		$\lvert V_{IEos}\rvert$	–	0.7	3.0	mV
Mute timing capacitor (pin 2)						
Switch-on voltage		V_{sw}	–	3.5	4.1	V
Loading current		$-I_L$	0.1	0.5	2.0	mA

AC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 2

parameter	conditions	symbol	min.	typ.	max.	unit
Amplifier A to Amplifier E						
Open loop gain		G_{ol}	–	90	–	dB
Overall distortion without de-emphasis		THD	–	−110	−100	dB
Slew rate (Amplifier A)		$\Delta V/\Delta t$	–	30	–	V/μs
Supply voltage ripple rejection						
V_{DD1}	note 1	SVRR	50	60	–	dB
V_{DD2}	note 2	SVRR	50	60	–	dB
V_{DD3}	note 2	SVRR	55	70	–	dB
Line amplifier D						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2.0	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion		THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and mute OFF output voltage (pins 10 and 19)		V_O	–	–	4	mV
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)	R_L = 600 Ω	$V_{O(rms)}$	–	6	–	V
	R_L = 132 Ω	$V_{O(rms)}$	–	5.5	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Total harmonic distortion	R_L = 132 Ω	THD	–	−88	−80	dB
Channel separation	20 Hz to 20 kHz; R_L = 600 Ω	α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and OFF output voltage (pins 13 and 16)		V_O	–	–	6	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute status (pin 3)	open collector output					
Output voltage LOW (mute ON)	$-I_{OL}$ = 3 mA	–	–	–	0.4	V
Output voltage HIGH (mute OFF)	$I_{OL} \leqslant 1\ \mu A$		2.4	–	V_{DD1}	V
Mute timing	note 3					
De-emphasis switch						
Input voltage HIGH	De-emphasis ON	V_{IH}	2.4	–	V_{DD1}	V
Input voltage LOW	De-emphasis OFF	V_{IL}	0	–	1	V
Input current HIGH	De-emphasis ON	I_{IH}	–	–	5.0	μA
Input current LOW	De-emphasis OFF	$-I_{IL}$	–	–	25	μA

Notes to the characteristics

1. The ripple rejection is measured at the output of the line amplifier; amplitude = 0.5 V_{tt}; f = 100 Hz to 10 kHz.
2. The ripple rejection is measured at the output of the line amplifier; amplitude = 1 V_{tt}; f = 100 Hz to 10 kHz.
3. The mute timing is provided by an external capacitor connected to pin 2.

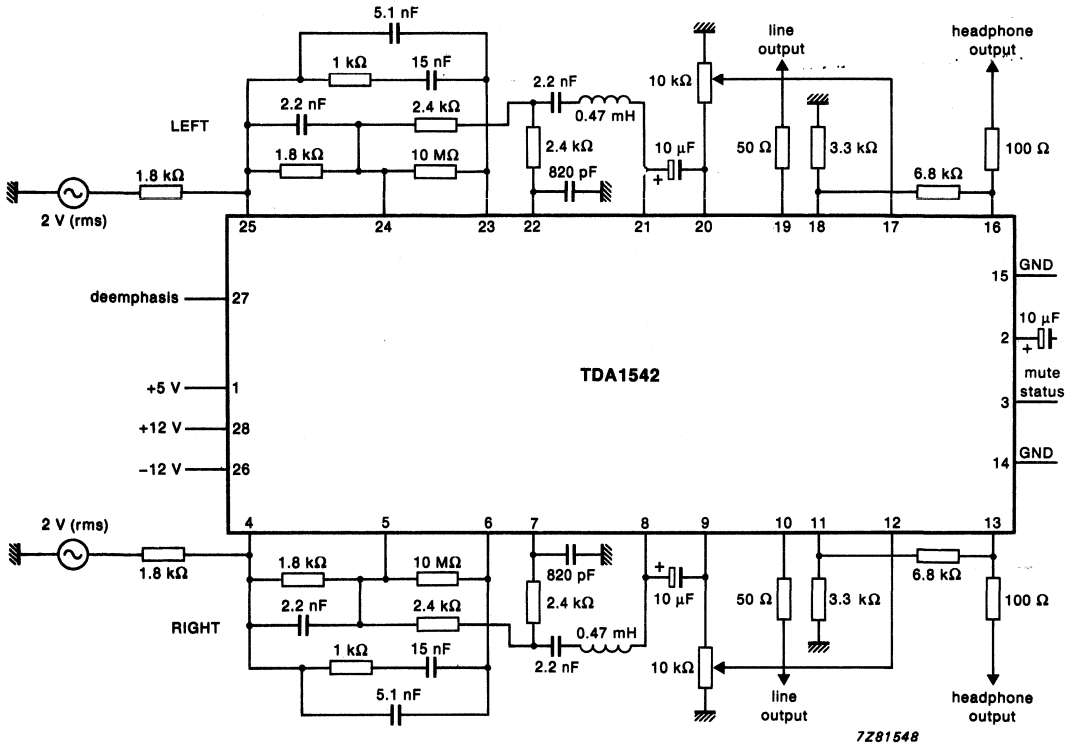


Fig. 2 Test and application circuit.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

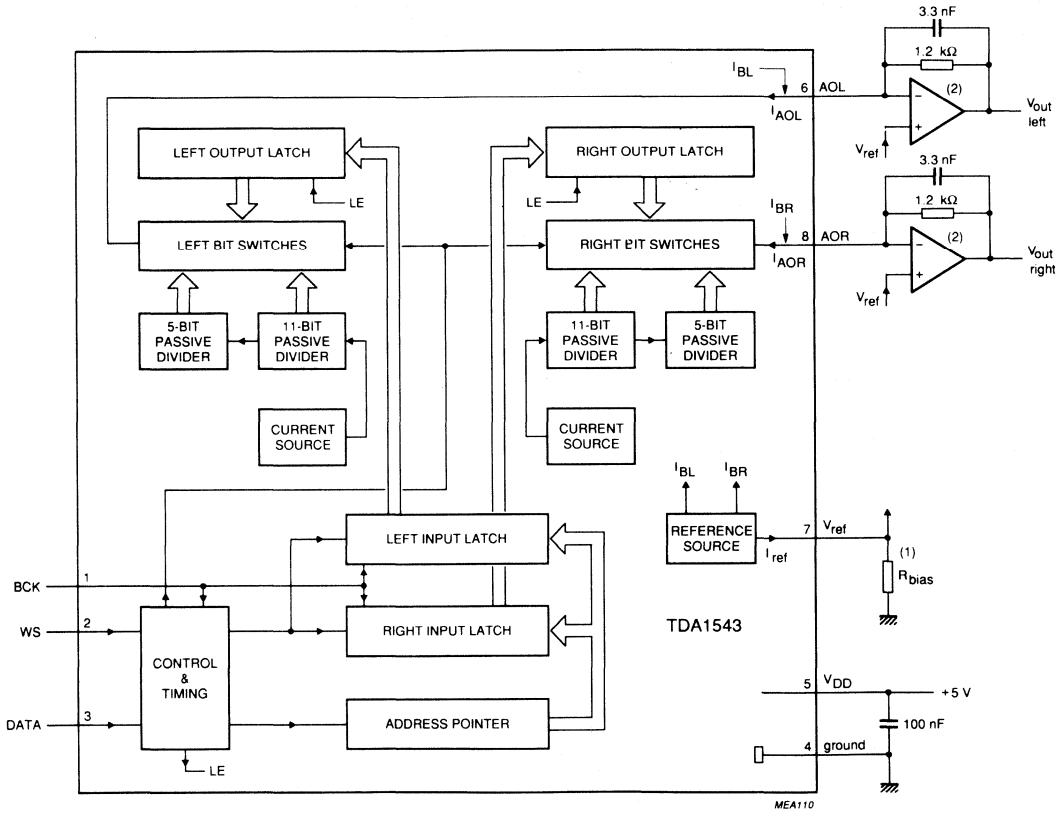
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise at 0 dB	-	−75	−70	dB
			-	0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB	-	−30	−23	dB
			-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (I²S input format)

TDA1543



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

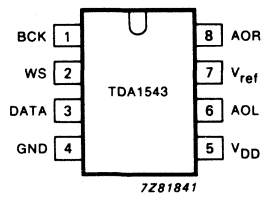


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

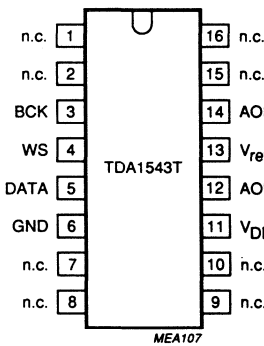
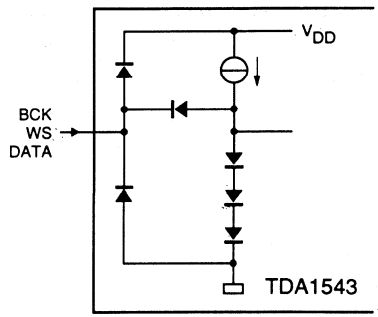
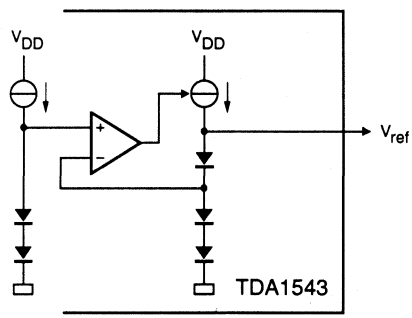


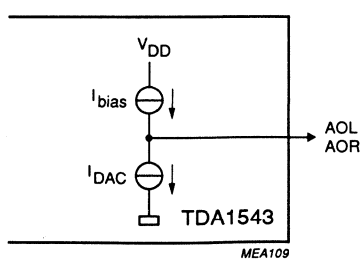
Fig.2(b) Pin configuration TDA1543T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	μA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	μs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	μs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

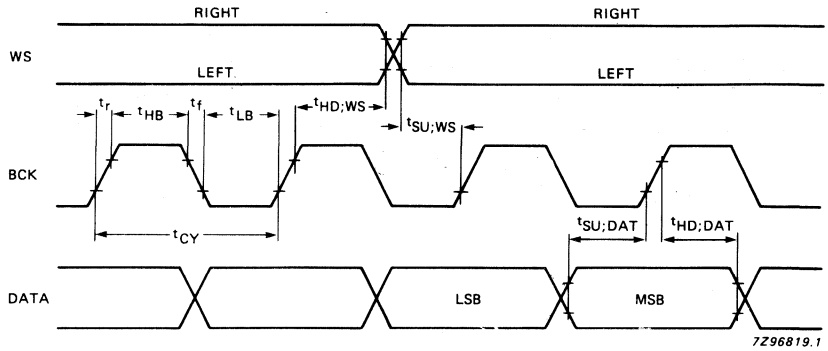


Fig.4 Format of input signals (I²S format).

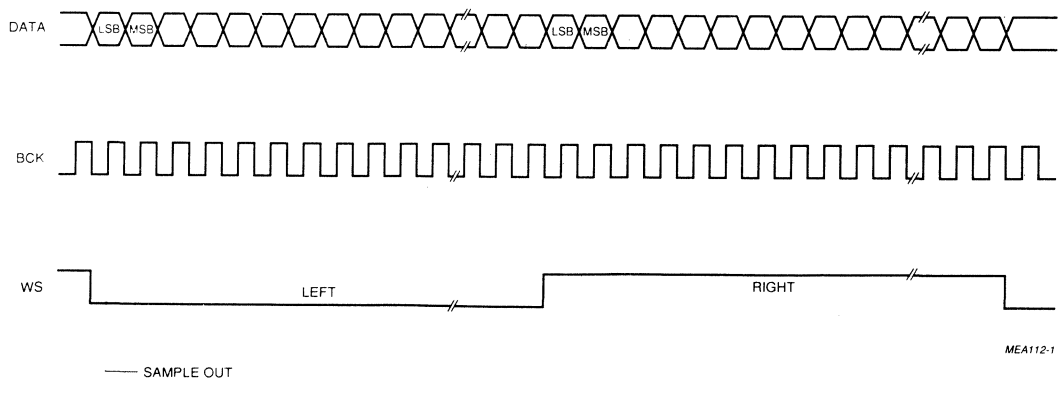


Fig.5 Format of input signals.

DUAL 16-BIT DAC (ECONOMY VERSION)
(Japanese-input format)

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in television systems and digital amplifiers.

Features

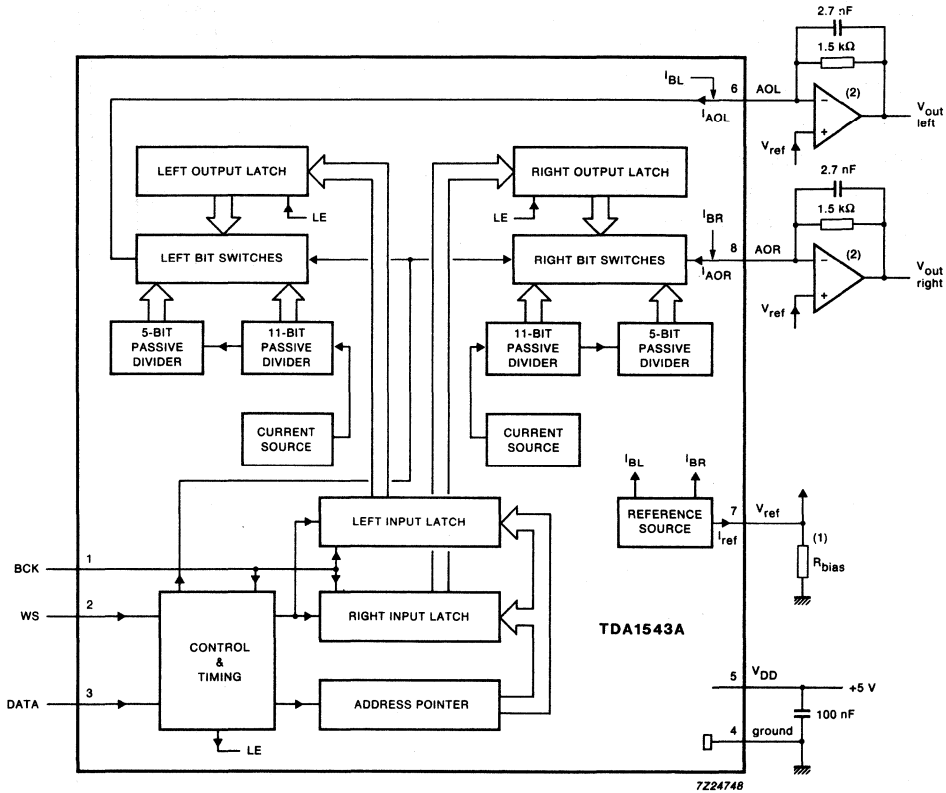
- Low distortion
- High dynamic range
- 16-bit resolution
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese-input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Total harmonic distortion (including noise)	(D + N)/S	–	–75	–70	dB
		–	0.018	0.032	%
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	9.2	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	9.2	MHz
Signal-to-noise ratio at bipolar zero	S/N	90	95	–	dB
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+ 85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.6	–	5.0	mA

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig.1 Block diagram.

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

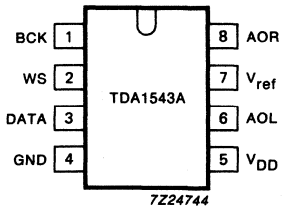
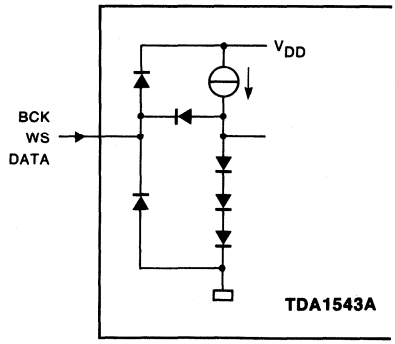
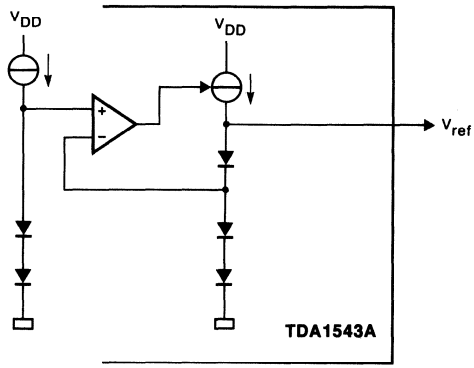


Fig.2 Pinning diagram.

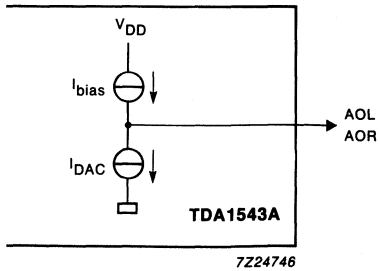
DEVELOPMENT DATA



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	50	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	9.2	MHz
bit rate data input pin 3		BR	–	–	9.2	Mbits/s
word select input pin 2		f_{WS}	–	–	192	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.95	2.3	2.65	mA
Full scale temperature coefficient		TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Offset current	I_{ref} = 0 mA; $V_{AO} = V_{ref}$	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.6	–	5.0	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	2.1	2.2	2.3	V
Reference current output		I_{ref}	−0.3	−	2.5	mA
Total harmonic distortion (including noise)	note 3	(D + N)/S	−	−75	−70	dB
			−	0.018	0.032	%
Settling time ± 1 LSB		t_{cs}	−	0.5	−	μs
Channel separation		α	84	90	−	dB
Unbalance between outputs	note 3	$\lvert d_{IO} \rvert$	−	< 0.2	0.3	dB
Time delay between outputs		t_d	−	< 0.2	−	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	−	dB
Timing	Fig.4					
Rise time		t_r	−	−	32	ns
Fall time		t_f	−	−	32	ns
Bit clock cycle time		t_{CY}	108	−	−	ns
Bit clock HIGH time		t_{HB}	22	−	−	ns
Bit clock LOW time		t_{LB}	22	−	−	ns
Data set-up time		$t_{SU;DAT}$	32	−	−	ns
Data hold time to bit clock		$t_{HD;DAT}$	2	−	−	ns
Word select hold time		$t_{HD;WS}$	2	−	−	ns
Word select set-up time		$t_{SU;WS}$	32	−	−	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

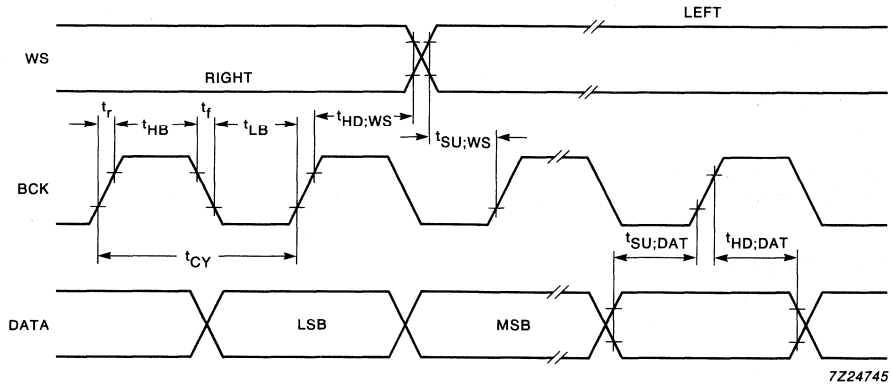


Fig.4 Format of input signals (Japanse format).

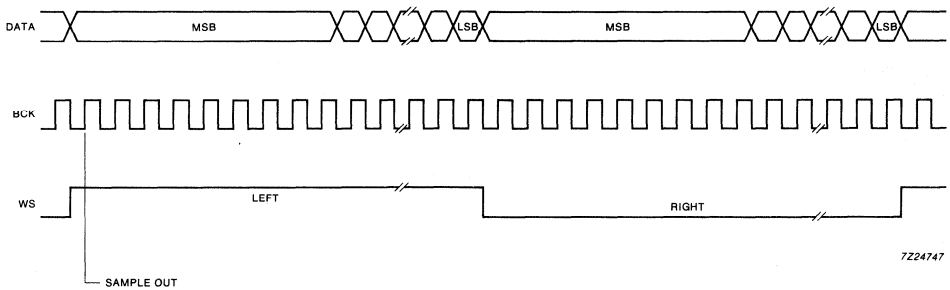


Fig.5 Format of input signals.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	September 1990

TDA1551Q

2 x 22 W BTL car radio power amplifier with diagnostic facility

FEATURES

- Requires very few external components
- Flexible in use – quad, single ended or stereo BTL
- I²C-bus control
- Dynamic distortion detector
- Thermal protection
- Output status information
- Power supply dip detection
- High output power
- MUTE/sleep mode by writing to I²C-bus
- Stand-by mode
- Fixed gain
- Good ripple rejection
- Load dump protection
- AC/DC short circuit safe to ground and V_P
- Reverse polarity safe
- Low offset voltage at output
- Capable of handling high energy at outputs (V_P = 0 V)
- Electrostatic discharge protection
- No switch-ON/switch-OFF plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

DESCRIPTION

The TDA1551Q is an integrated class-B output amplifier encased in a 17-lead single-in-line plastic power package. The device contains 4 x 11 W single-ended (SE) or 2 x 22 W BTL amplifiers and is intended for use in car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	operating	6	14.4	18	V
V_P	supply voltage	non-operating	-	-	30	V
I_P	total quiescent current		-	80	160	mA
Quad single-ended application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	6	-	W
		R_L = 2 Ω; THD = 10 %	-	11	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	50	-	μV
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	22	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	70	-	μV
ΔV_o	DC output offset voltage		-	-	100	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1551Q	17	SIL bent to DIL	plastic	SOT243RAA, RGA

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

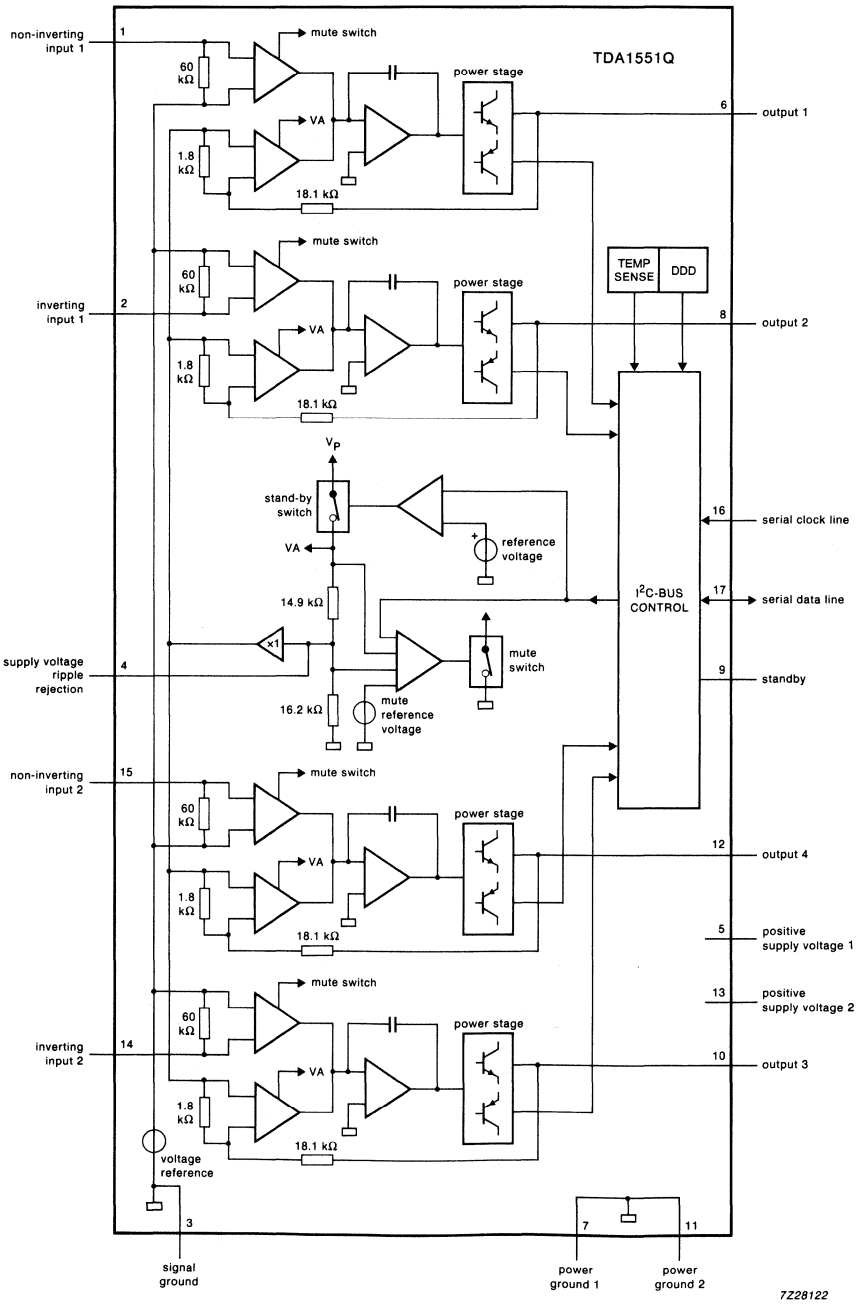


Fig.1 Block diagram.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

PIN CONFIGURATION

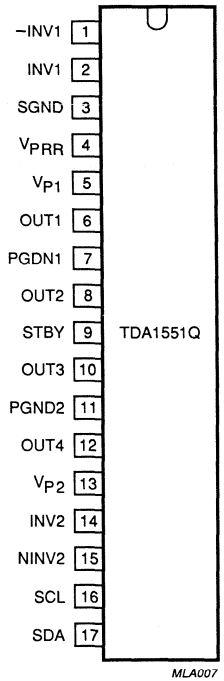


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
INV1	2	inverting input 1
GND	3	signal ground
V_{PRR}	4	supply voltage ripple rejection
V_{p1}	5	positive supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
SB	9	standby
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{p2}	13	positive supply voltage 2
INV2	14	inverting input 2
−INV2	15	non-inverting input 2
SCL	16	serial clock line
SDA	17	serial data line

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Supply voltage				
V_P	operating voltage	–	18	V
V_P	non-operating voltage	–	30	V
	load dump protect	–	45	V
IOSM	non-repetitive peak output current	–	6	A
IORM	repetitive peak output current	–	4	A
T_{stg}	storage temperature range	−65	150	°C
T_c	crystal temperature	–	150	°C
V_{Psc}	AC/DC short-circuit safe voltage	–	18	V
	energy handling capability at outputs (V_P = 0)	–	200	mJ
V_{Pr}	reverse polarity	–	6	V
P_{tot}	total power dissipation (Fig.2)	–	60	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction to case (Fig.3)	1.5	–	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40	–	K/W

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

FUNCTIONAL DESCRIPTION

The TDA1551Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) which can be used in SE or BTL applications. The gain of each amplifier is fixed at 20 dB for SE and 26 dB for BTL. The device also contains an I²C-bus facility which operates in the read or write mode.

In the **write** mode the device can be switched to either the sleep condition (low sleep current of 0.6 mA typ.), the MUTE condition or the ON condition.

In the **read** mode an 8-bit status word is available. Data bits D0 to D3 contain status information of each of the 4 outputs. If the device is switched to the ON or MUTE condition and there is a short-circuit at one or more outputs, the power transistors will be outside their safe operating area consequently one or more bits of D0 to D3 will be HIGH. Bits D0 to D3 are LOW when in the normal safe operating area. Bit D4 is normally LOW, if one or more channels reaches the clipping level D4 will go HIGH. Bit D5 is normally LOW, if the crystal temperature reaches 150 °C D5 will go HIGH. After a power-on reset bit 7 will go HIGH and a dip in the power supply will be noticed. Bit 7 will go LOW after the I²C-bus is read. When pin 9 is LOW the device will switch OFF and the supply current will be reduced to 0.1 mA (max.).

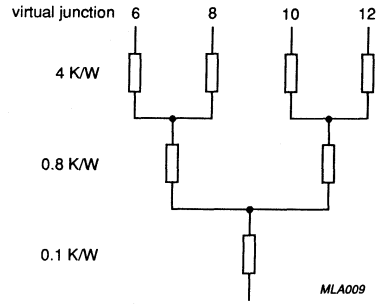


Fig.3 Thermal equivalent resistance network.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25°C; measurements in accordance with Fig.6 unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	7.2	–	V
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	100	mV
MUTE/sleep/standby						
V_O	output signal in MUTE position	$V_{I(max)}$ = 1 V; f = 20 Hz to 15 kHz	–	–	2	mV
I_P	DC current in sleep condition	V9 > 3 V	–	0.7	*	mA
I_P	DC current in standby condition	V9 < 2 V	–	–	0.1	mA
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	100	mV

AC CHARACTERISTICS

V_P = 14.4 V; T_amb = 25°C; f = 1 kHz; R_L = 4 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (Fig.7)						
P_O	output power	THD = 0.5% THD = 10%	15 20	17 22	- -	W W
P_O	output power	V_P = 13.2 V THD = 0.5% THD = 10%	 - -	 12 17	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB with respect to 15 W	-	20 - 15000	-	Hz
f_{LOW}	low frequency roll-off	at −3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at −1 dB	20	-	-	kHz
G_v	closed loop voltage gain		25	26	27	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 standby; note 4	48 48 80	- - -	- - -	dB dB dB
$\lvert Z_i\rvert$	input resistance		25	30	38	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	70 100 60	- 200 -	μV μV μV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%

* Value to be fixed.

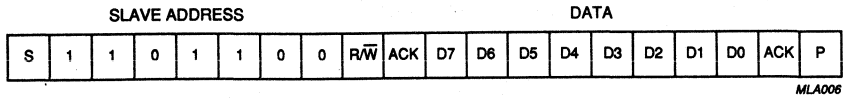
AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad single-ended application (Fig.6)						
P_O	output power	THD = 0.5%; note 7 THD = 10%; note 7	4 5.5	5 6	- -	W W
P_O	output power	R_L = 2 Ω THD = 0.5%; note 7 THD = 10%; note 7	 7.5 10	 8.5 11	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
f_{LOW}	low frequency roll-off	at −3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at −1 dB	20	-	-	kHz
G_v	closed loop voltage gain		19	20	21	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 stand-by; note 4	48 48 80	- - -	- - -	dB dB dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	50 70 60	- 100 -	μV μV μV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\|\Delta G_v\|$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%
I²C-bus (see I²C-bus protocol)						
V_{IH}	input voltage HIGH		3	-	5.5	V
V_{IL}	input voltage LOW		− 0.3	-	1.5	V
I_{IH}	input current HIGH	V = 5.5 V	−10	-	10	μA
I_{IL}	input current LOW	V = GND	−10	-	10	μA
V_{OL}	output voltage LOW	I_L = 3 mA	-	-	0.4	V
Power-on reset (increasing supply voltage)						
V_P	start of reset end of reset		* -	- -	- 5	V V
Standby (pin 9)						
V_9	input voltage HIGH input voltage LOW		3 -	- -	V_P 2	V V

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V and AC operating at V_P = 8 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage < V_P/2.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω and at a frequency of 100 Hz to 10 kHz (amplitude = 2 V(p-p).
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

I²C-bus protocol



S start condition
R/$\overline{W}$ read/write bit; LOW = write, HIGH = read
ACK acknowledge, generated by the receiving device
DATA see Tables 1 and 2
P stop condition

Fig.4 I²C-bus protocol.

Table 1: WRITE definition (R/$\overline{W}$ = LOW)

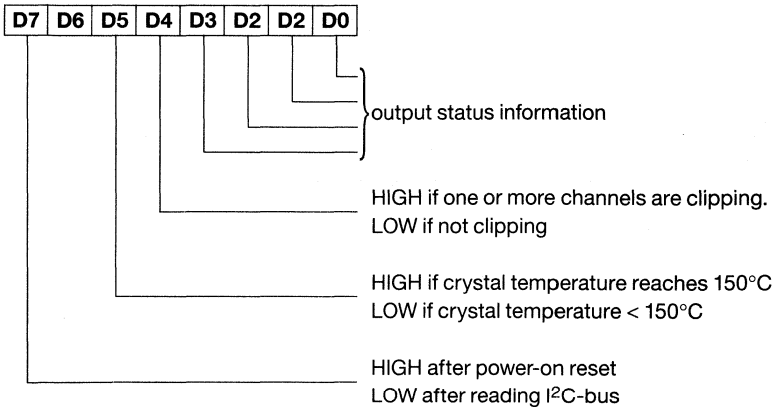
MSB			DATA				LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	SLEEP condition
0	0	0	0	0	0	0	1	MUTE condition
0	0	0	0	0	0	1	0	not allowed (1)
0	0	0	0	0	0	1	1	ON condition (2)

Bit D0 switches from SLEEP to the ON condition
Bit D1 switches the MUTE condition

(1) For test purposes only; I²C-bus controlled during the ON condition, amplifier is in the stand-by condition.

(2) To get into the ON condition without switch-on plops, the device should be switched from the SLEEP condition to the MUTE condition and then, after a period of * ms, to the ON condition.

Table 2: READ definition (R/W = HIGH)



If the device is sinewave driven bit D4 will be HIGH if the THD in one or more channels exceeds 3.5%.

Table 3: Fault conditions

DATA		MSB		
D3	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	all output power transistors in the normal safe operating condition
-	-	-	1	fault condition pin 6
-	-	1	-	fault condition pin 8
-	1	-	-	fault condition pin 10
1	-	-	-	fault condition pin 12

If more outputs are in a fault condition (e.g. short-circuit) then more bits, D3 to D0, will be HIGH.

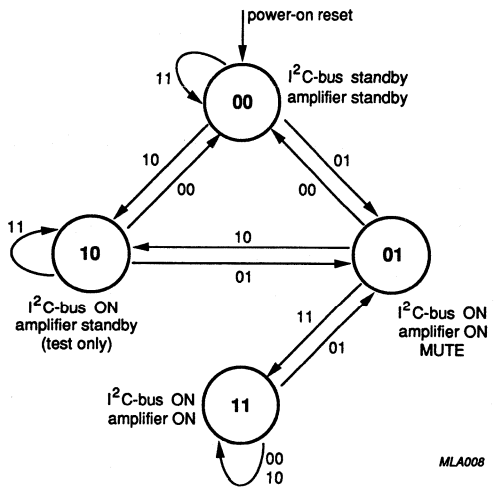


Fig.5 State diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

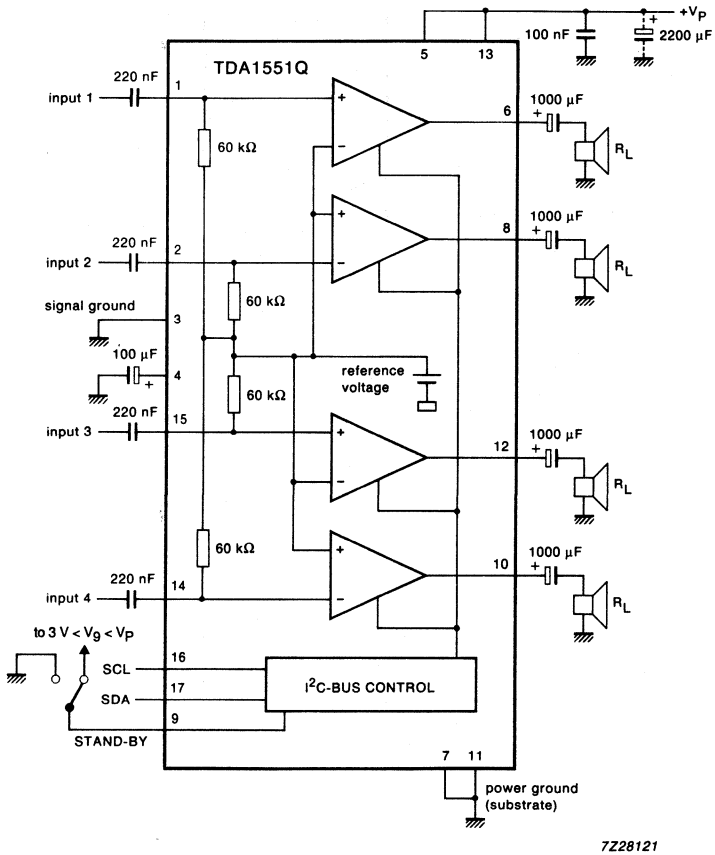


Fig.6 Test circuit quad single-ended.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

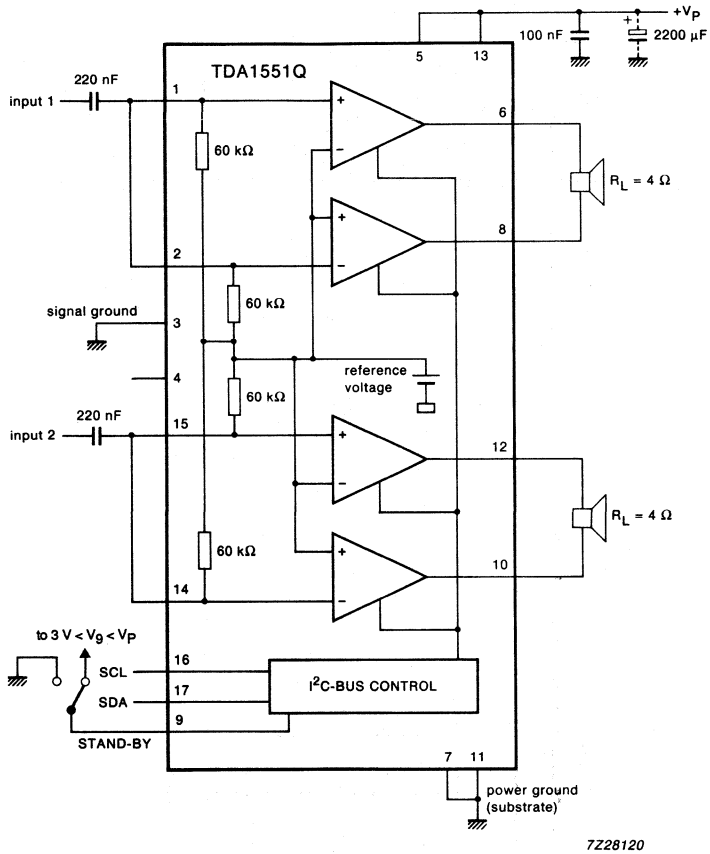


Fig.7 Test circuit stereo BTL.

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1552Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

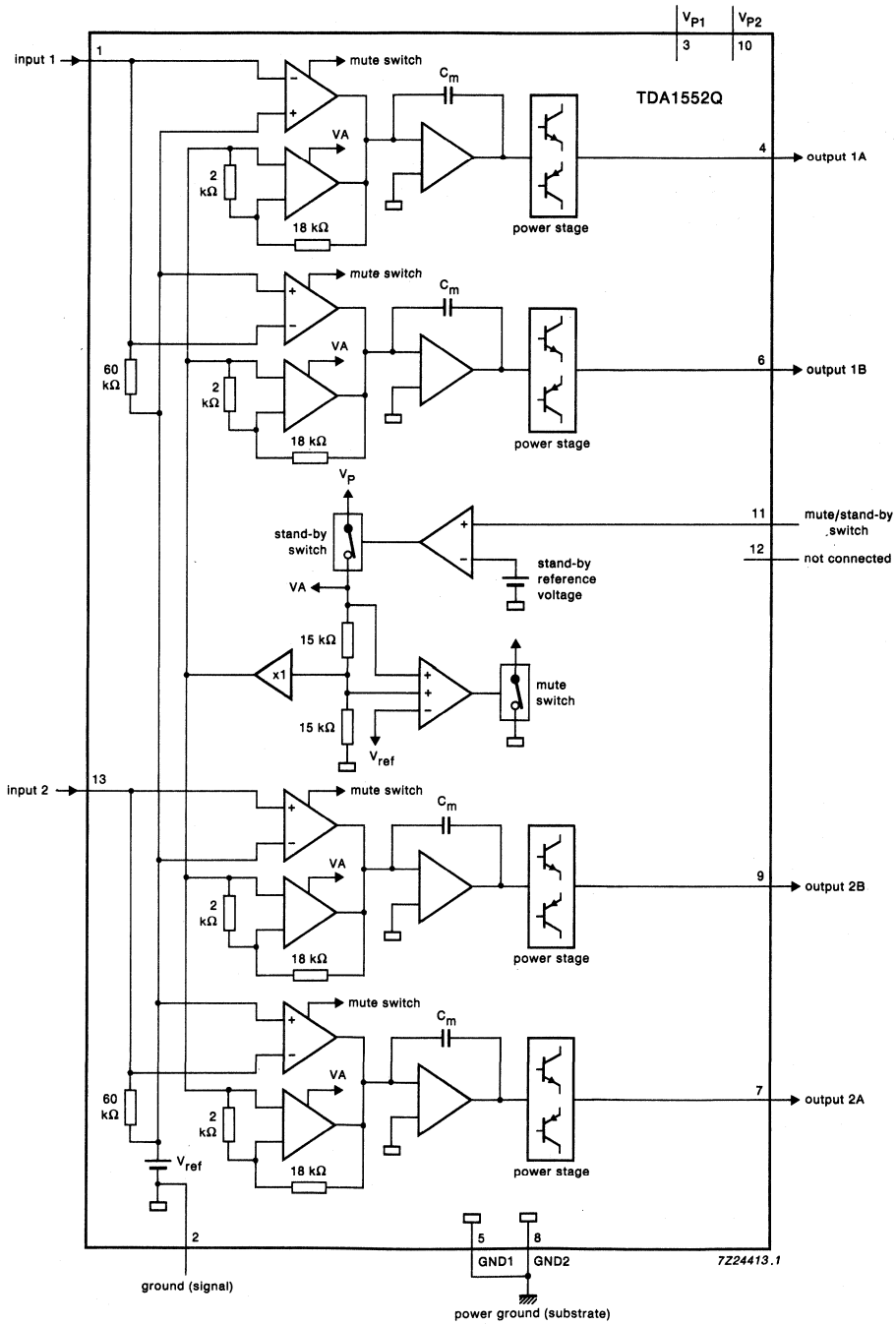


Fig.1 Block diagram.

PINNING

1	IP1	input 1
2	GND	ground (signal)
3	V_{P1}	positive supply voltage 1
4	OUT1A	output 1A
5	GND1	power ground 1 (substrate)
6	OUT1B	output 1B
7	OUT2A	output 2A
8	GND2	power ground 2 (substrate)
9	OUT2B	output 2B
10	V_{P2}	positive supply voltage 2
11	M/SS	mute/stand-by switch
12	n.c.	not connected
13	IP2	input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1552Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–65	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

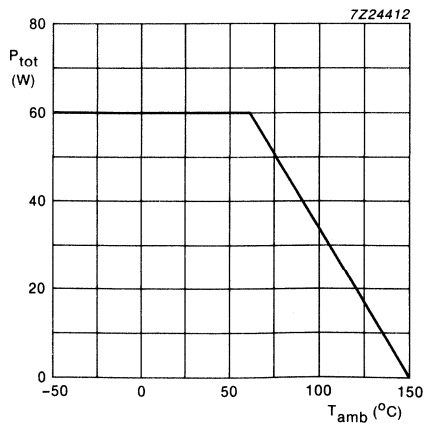


Fig.2 Power derating curve.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_{II} < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \text{ V} \leqslant V_{II} < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to GND note 3	I_P	–	5.5	–	mA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4; −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Conditions: 1. V_{II} = 0 V
   2. short-circuit to GND
   3. switch V_{II} to MUTE or ON condition
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

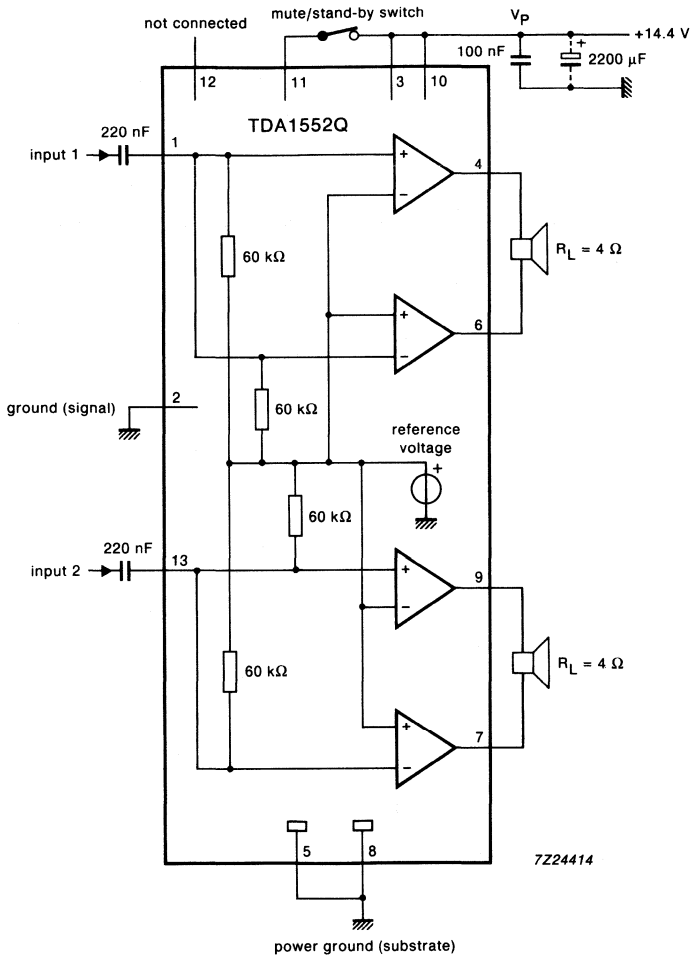


Fig.3 Application circuit diagram.

DEVELOPMENT DATA

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER WITH LOUDSPEAKER PROTECTION

GENERAL DESCRIPTION

The TDA1553Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Loudspeaker protection (LSP)
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

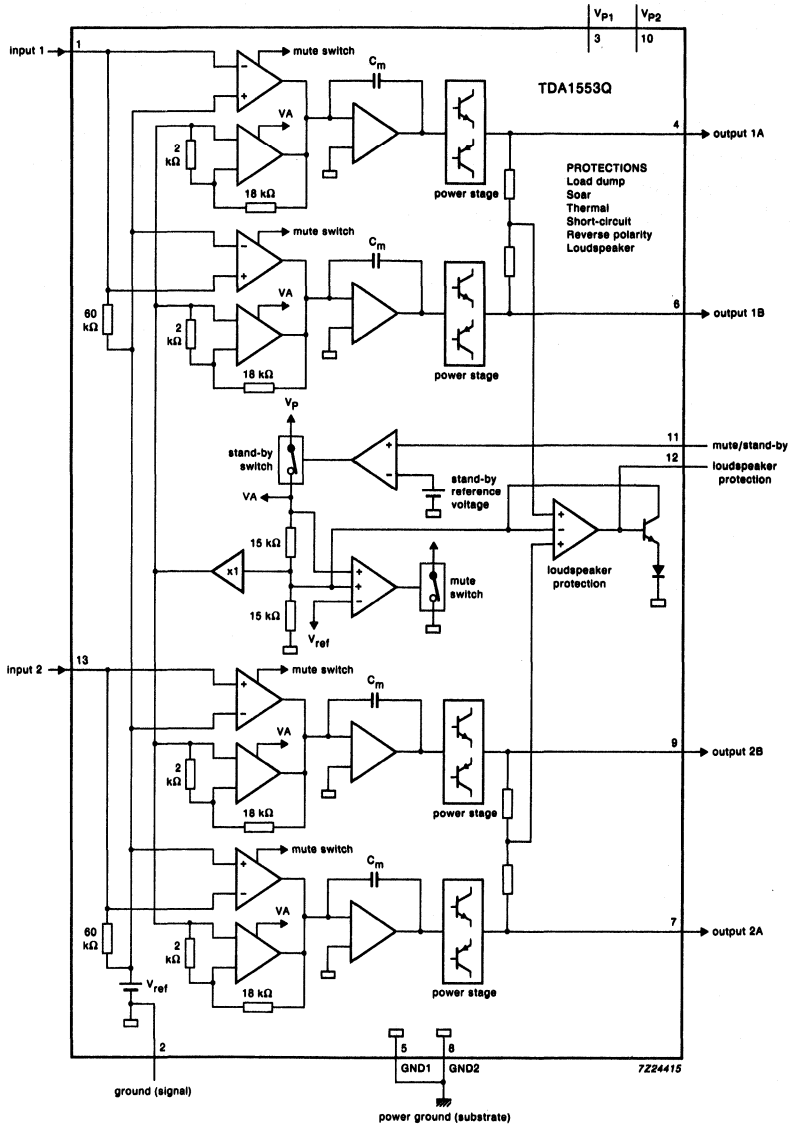


Fig.1 Block diagram.

PINNING

1	IP1	input 1
2	GND	ground (signal)
3	V_{P1}	positive supply voltage 1
4	OUT1A	output 1A
5	GND1	power ground 1 (substrate)
6	OUT1B	output 1B
7	OUT2A	output 2A
8	GND2	power ground 2 (substrate)
9	OUT2B	output 2B
10	V_{P2}	positive supply voltage 2
11	M/SS	mute/stand-by switch
12	LSP	loudspeaker protection
13	IP2	input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1553Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

Mute/stand-by switch

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Loudspeaker protection

When a short-circuit to ground is made, which forces a DC voltage across the loudspeaker of $\geqslant$ 1 V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to $\leqslant$ 1 V. The delay time of the protection circuit can be controlled by an external capacitor connected to pin 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–65	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	V_P = 0 V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

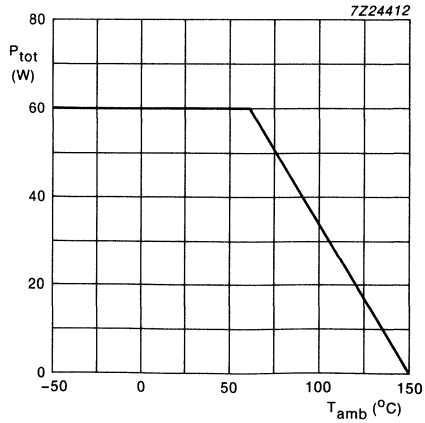


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_{I1} < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \leqslant V_{I1} < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to ground note 3	I_p	–	5.5	–	mA
Loudspeaker protection						
DC voltage across R_L pin 4 to pin 6		ΔV_{4-6}	–	–	1	V
pin 7 to pin 9		ΔV_{7-9}	–	–	1	V
Delay time		t_d	–	0.5	–	s
Protection active	$\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert \geqslant 1.0$ V					
Current information		I_{12}	–	25	–	μA
Voltage information		V_{12}	2	–	–	V
Protection not active	$\lvert\Delta V_{4-6}\rvert$ and $\lvert\Delta V_{7-9}\rvert \leqslant 0.1$ V					
Voltage information		V_{12}	–	–	0.3	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4; −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Conditions: 1. V_{II} = 0 V
   2. short-circuit to GND
   3. switch V_{II} to MUTE or ON condition.
   (t_I V_{II} > 10 μs)
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

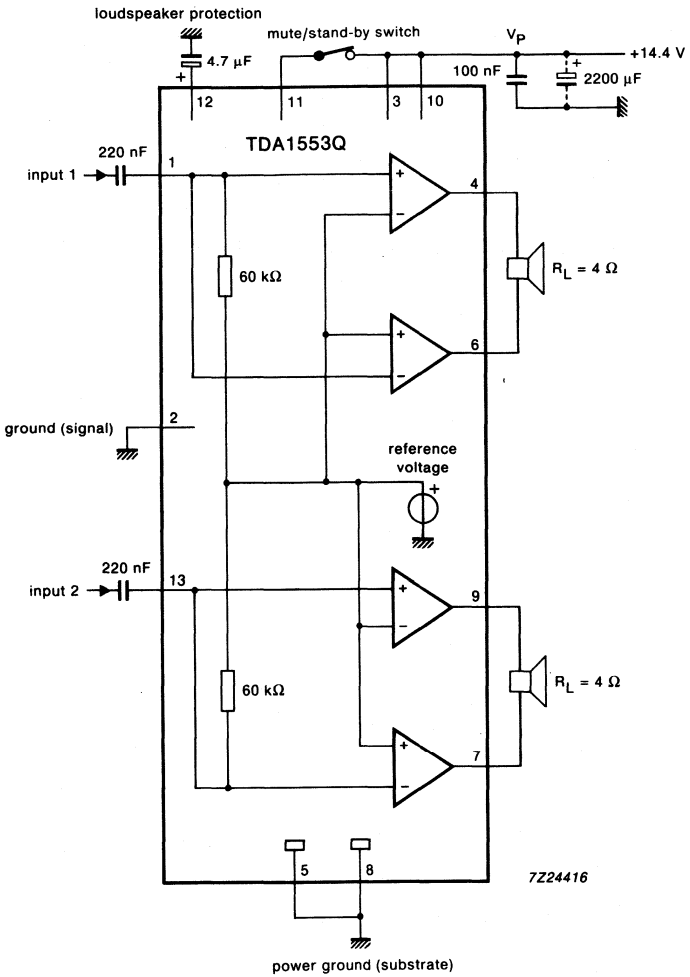


Fig.3 Application circuit diagram.

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1554Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243).

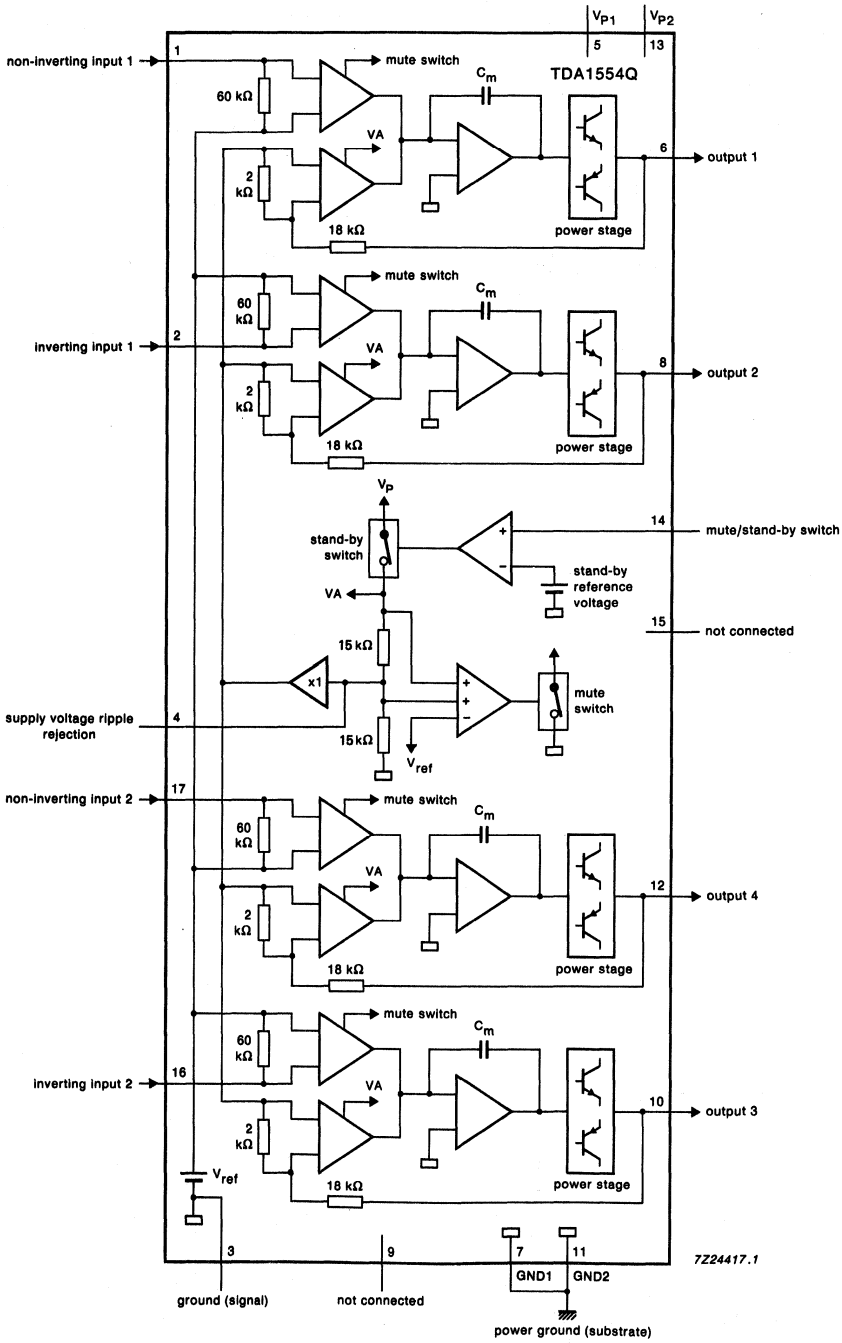


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (signal)
4	RR	supply voltage ripple rejection
5	V_{P1}	positive supply voltage 1
6	OUT1	output 1
7	GND1	power ground 1 (substrate)
8	OUT2	output 2
9	n.c.	not connected
10	OUT3	output 3
11	GND2	power ground 2 (substrate)
12	OUT4	output 4
13	V_{P2}	positive supply voltage 2
14	M/SS	mute/stand-by switch
15	n.c.	not connected
16	INV2	inverting input 2
17	NINV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1554Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–65	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

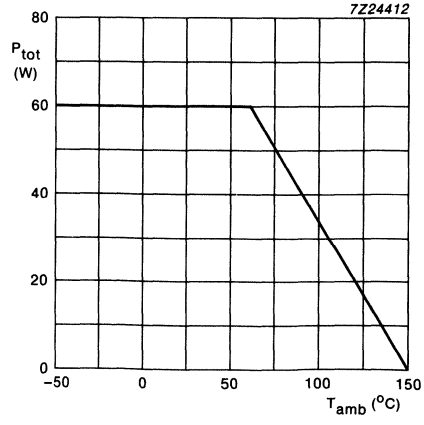


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3 −1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

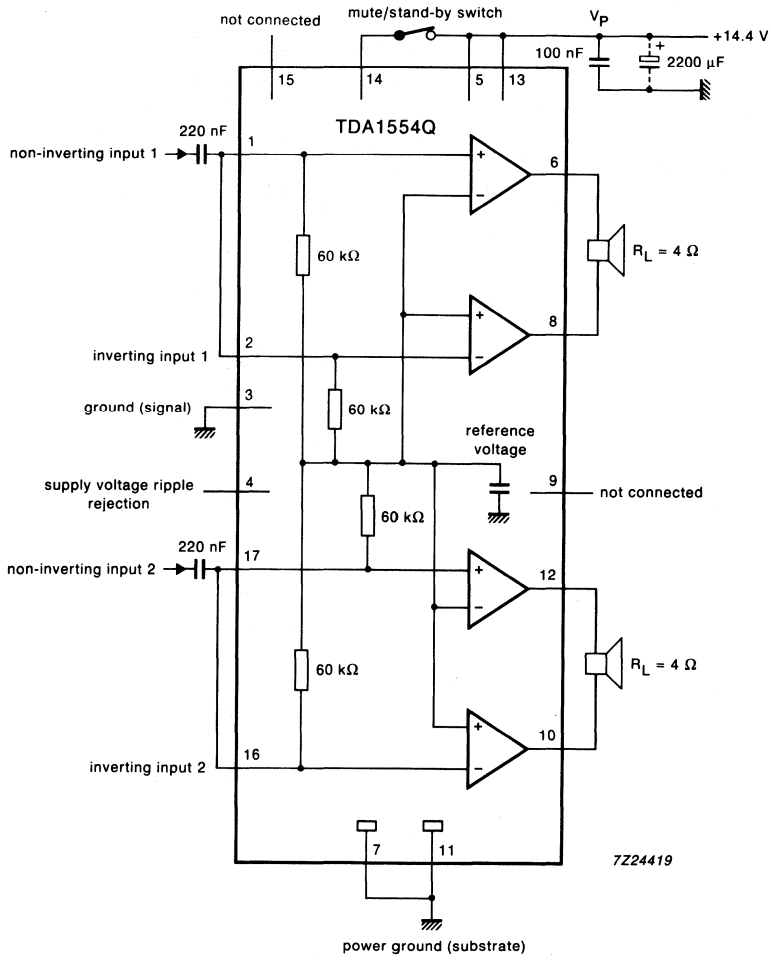


Fig.3 Stereo BTL application circuit diagram.

DEVELOPMENT DATA

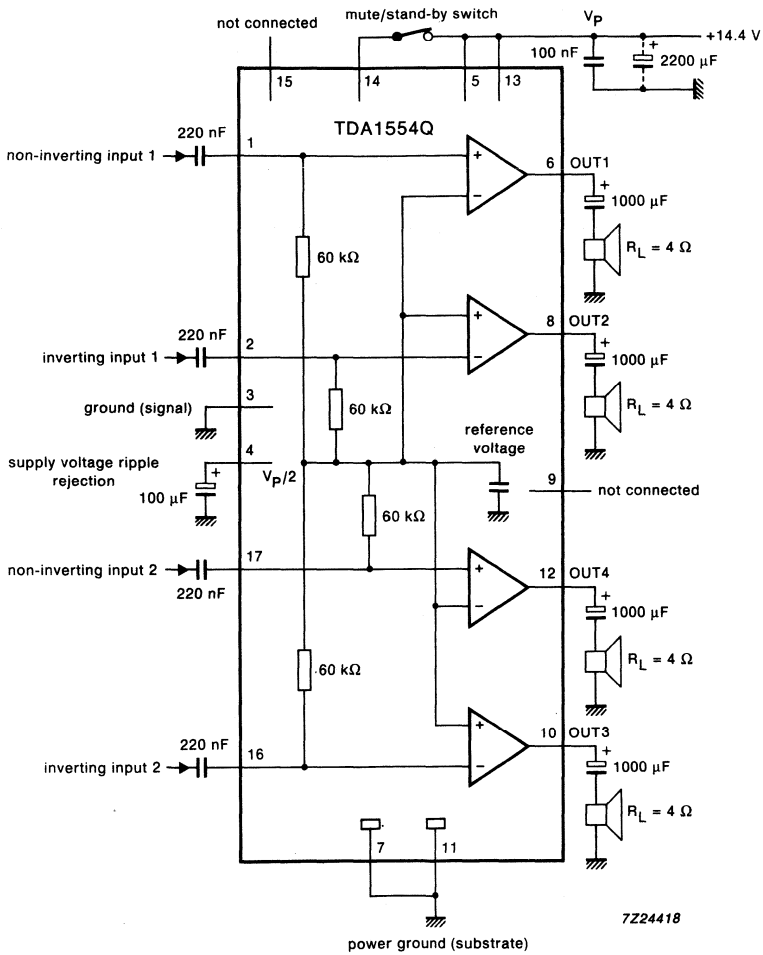


Fig.4 Quad single-ended application circuit diagram.

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER WITH DISTORTION DETECTOR

GENERAL DESCRIPTION

The TDA1555Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads
- Distortion detector

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243).

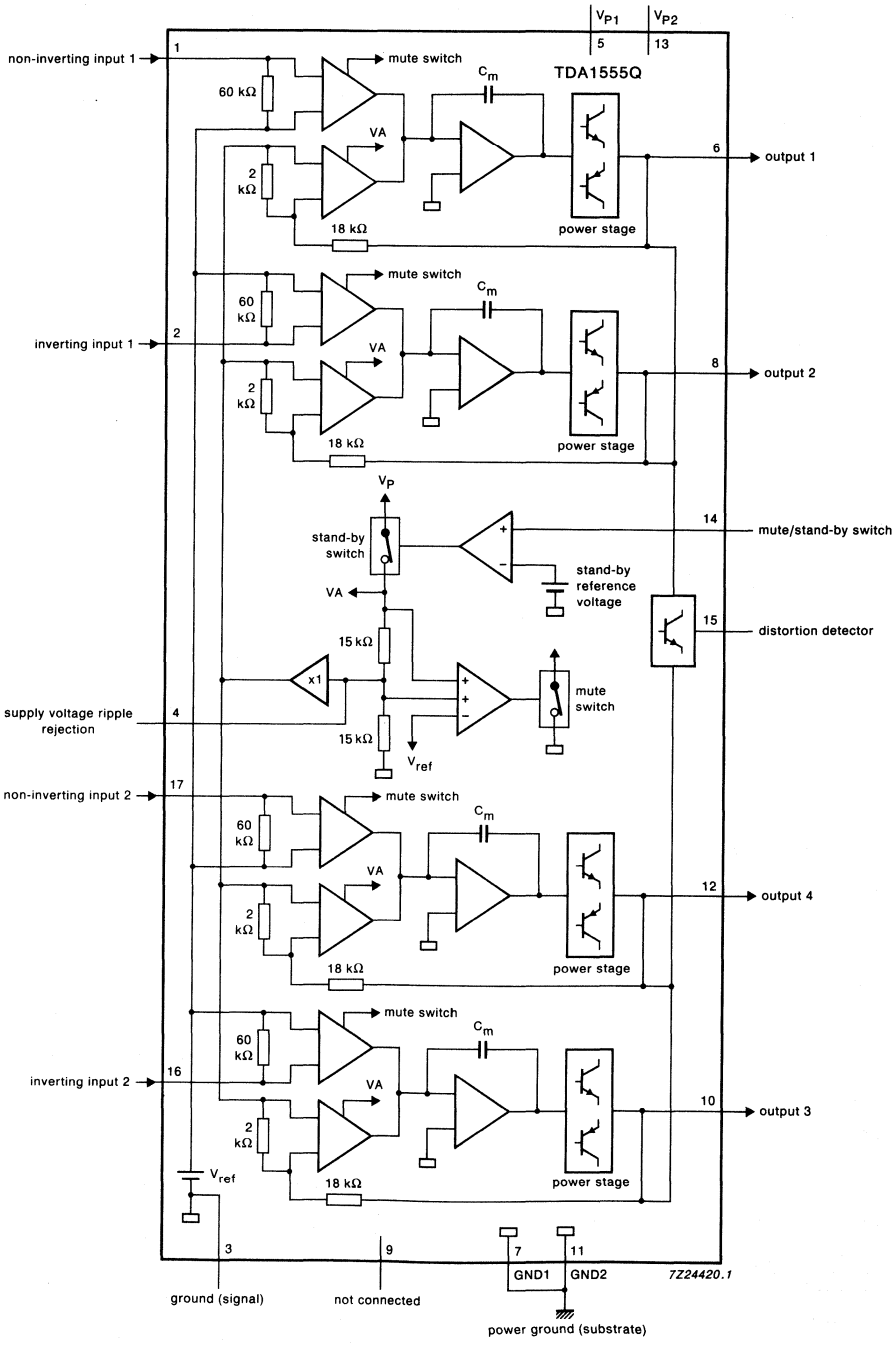


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (signal)
4	RR	supply voltage ripple rejection
5	V_{P1}	positive supply voltage 1
6	OUT1	output 1
7	GND1	power ground 1 (substrate)
8	OUT2	output 2
9	n.c.	not connected
10	OUT3	output 3
11	GND2	power ground 2 (substrate)
12	OUT4	output 4
13	V_{P2}	positive supply voltage 2
14	M/SS	mute/stand-by switch
15	DD	distortion detector
16	INV2	inverting input 2
17	NINV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1555Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of this device are:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Distortion detector

- At onset of clipping of one or more channels the distortion detector (pin 15) becomes active. This information can be used to drive a sound processor or DC volume control to decrease the input signal and so limit distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–65	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

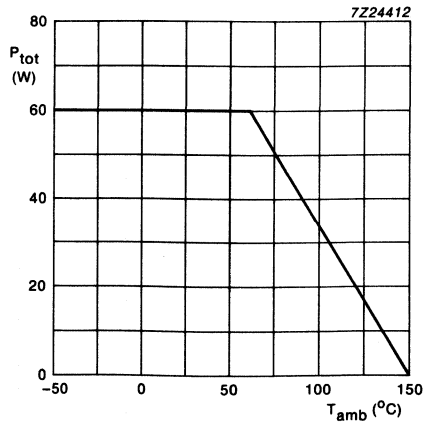


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = –1 dB w.r.t. 15 W	B_W	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3 –1 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	–3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB
Distortion detector	$\hat{I}_{DD}$ = 50 μA	THD	2	–	5	%

DEVELOPMENT DATA

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

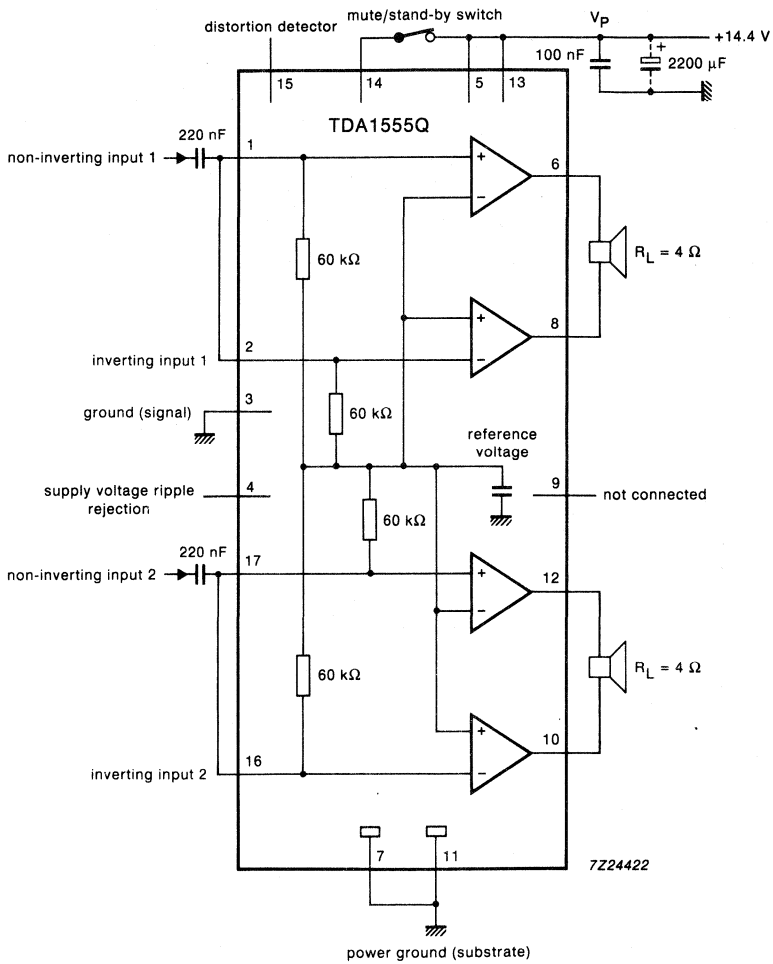


Fig.3 Stereo BTL application circuit diagram.

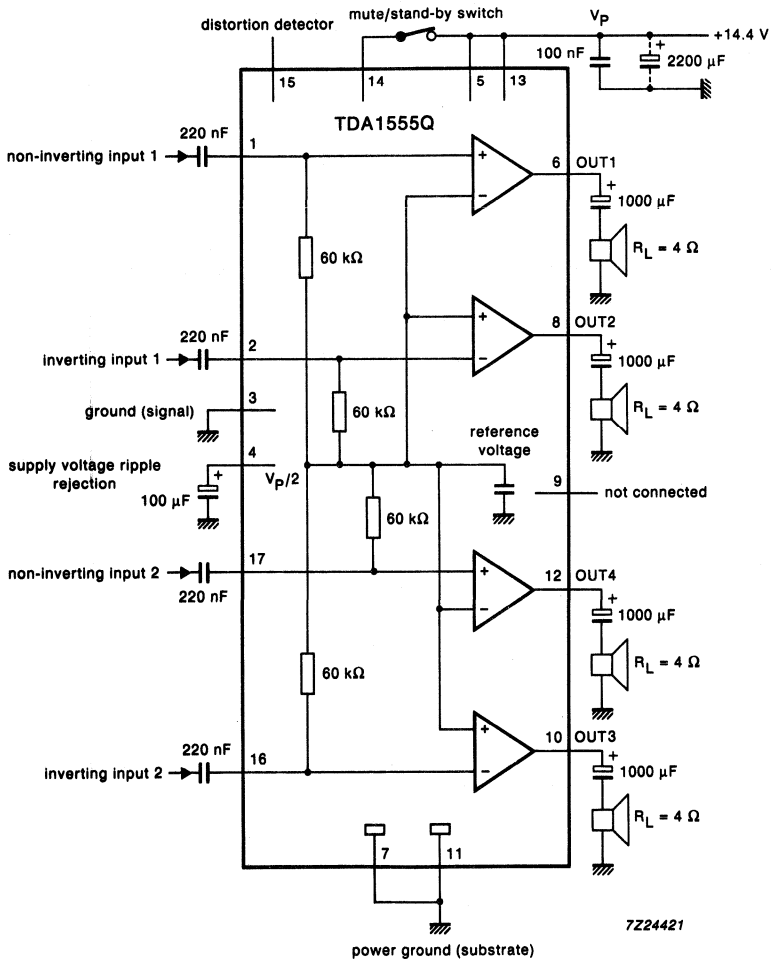


Fig.4 Quad single-ended application circuit diagram.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1572 integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

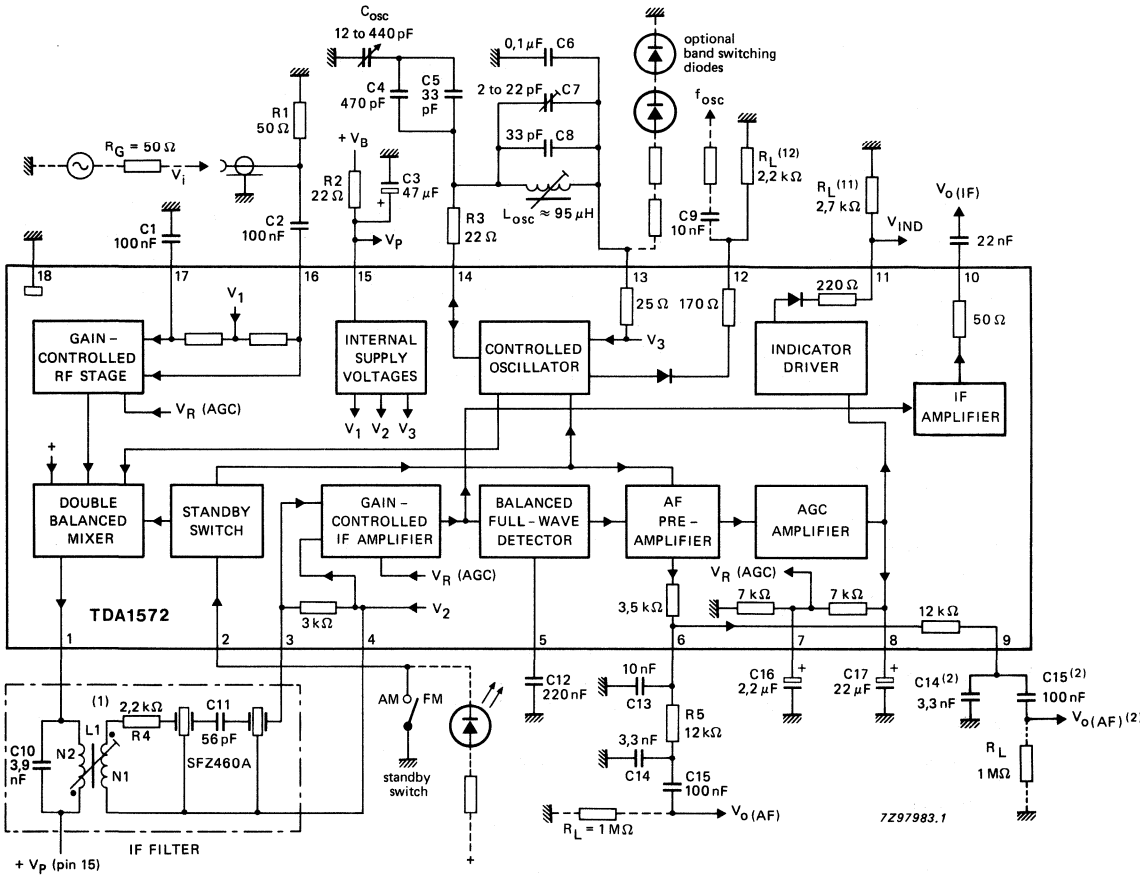
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7,5	–	18,0	V
Supply current range	I_P	15	–	30	mA
RF input voltage for (S+N)/N = 6 dB at m = 30%	$V_{i(RF)}$	–	1,5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%	$V_{i(RF)}$	–	500	–	mV
IF output voltage with V_i = 2 mV	$V_{o(IF)}$	–	230	–	mV
AF output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{o(AF)}$	–	310	–	mV
AGC range: change of V_i for 1 dB change of $V_{o(AF)}$		–	86	–	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(11)}$ = 2,7 kΩ	V_{IND}	–	2,8	–	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

(2) AF output is pin 6 is not used.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S+N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{13\text{-}18}$. An extra buffered oscillator putput (pin 12) is available for driving a synthesizer. If this is not needed, resistor $R_{L(12)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 10.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(11)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{15-18}$	–	20	V
Total power dissipation	P_{tot}	–	875	mW
Input voltage	$\|V_{16-17}\|$	–	12	V
	$-V_{16-18}$, $-V_{17-18}$	–	0,6	V
	V_{16-18}, V_{17-18}	–	V_P	V
Input current	$\|I_{16}\|$, $\|I_{18}\|$	–	200	mA
Operating ambient temperature range	T_{amb}	–40	+ 85	°C
Storage temperature range	T_{stg}	–55	+ 150	°C
Junction temperature	T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$		80	K/W

CHARACTERISTICS

$V_P = V_{15-18} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 15)	V_P	7,5	8,5	18,0	V
Supply current (pin 15)	I_P	15	23	30	mA
RF stage and mixer (pins 16 and 17)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$	Z_i	–	5,5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6,5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-15(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1,2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability: (r.m.s. value): input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,1	–	60	MHz
Oscillator amplitude (pins 13 to 14)	V	–	130	150	mV
External load impedance (pins 14 to 13)	$R_{(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation (pins 14 to 13)	$R_{(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_{15}/V_{13}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 13)	V	–	4,2	–	V
DC output current (for switching diodes) (pin 13)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{13} = 20 mA (switch to maximum load) (pin 13)	ΔV_I	–	0,3	–	V
Buffered oscillator output (pin 12)					
DC output voltage	V_O	–	0,8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p-p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2,0	–	V
IF input impedance (pins 3 to 4)	Z_i	2,4	3,0	3,9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4)	V_i	–	90	–	mV
IF output impedance (pin 10)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 10)	V_o	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 18)	G_v	–	68	–	dB
AGC range of IF stages: change of V_{3-4} for 1 dB change of $V_{o(AF)}$; $V_{3-4(ref)}$ = 75 mV	ΔV_v	–	55	–	dB
AF output voltage at $V_{3-4(IF)}$ = 50 μV	$V_{o(AF)}$	–	130	–	mV
AF output voltage at $V_{3-4(IF)}$ = 1 mV	$V_{o(AF)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2,8	3,5	4,2	kΩ

parameter	symbol	min.	typ.	max.	unit
Indicator driver (pin 11)					
Output voltage at V_i = 0 mV; R_L = 2,7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV; R_L = 2,7 kΩ	V_o	2,5	2,8	3,1	V
Load resistance	R_L	1,5	–	–	kΩ
Standby switch					
Switching threshold at; V_P = 7,5 to 18 V; T_{amb} = −40 to +80 °C					
ON-voltage	V_{2-1}	0	–	2,0	V
OFF-voltage	V_{2-1}	3,5	–	20,0	V
ON-current at V_{2-1} = 0 V	$-I_2$	–	100	200	μA
OFF-current at V_{2-1} = 20 V	$\|I_2\|$	–	–	10	μA

OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

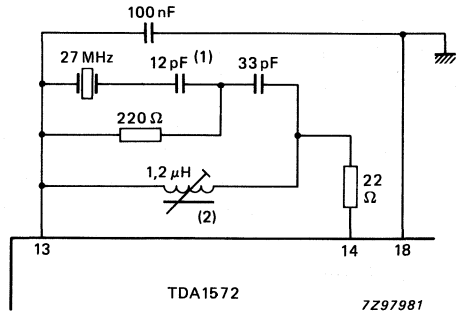
parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input required for (S+N)/N = 6 dB	V_i	–	1,5	–	μV
RF input required for (S+N)/N = 26 dB	V_i	–	15	–	μV
RF input required for (S+N)/N = 46 dB	V_i	–	150	–	μV
RF input at start of AGC	V_i	–	30	–	μV
RF large signal handling					
RF input at THD = 3%; m = 80%	V_i	–	500	–	mV
RF input at THD = 3%; m = 30%	V_i	–	700	–	mV
RF input at THD = 10%; m = 30%	V_i	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(AF)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
IF output voltage at V_i = 2 mV	$V_{o(IF)}$	180	230	290	mV
AF output voltage at V_i = 4 μV; m = 80%	$V_{o(AF)}$	–	130	–	mV
AF output voltage at V_i = 2 mV	$V_{o(AF)}$	240	310	390	mV
THD at V_i = 1 mV	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV	d_{tot}	–	1	–	%
Signal plus noise-to-noise ratio at V_i = 100 mV	(S+N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_p = 100 Hz ($SVRR = 20 \log [V_P/V_{o(AF)}]$)	RR	–	38	–	dB
a) additional AF signal at IF output	RR	–	0*	–	dB
b) add modulation at IF output (m_{ref} = 30%)	RR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	*	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	*	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

* Value to be fixed.

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; $Q_o = 80$.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

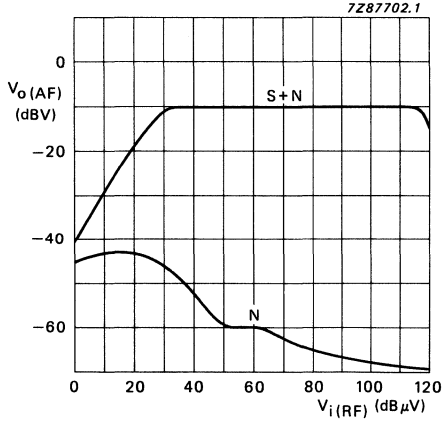


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

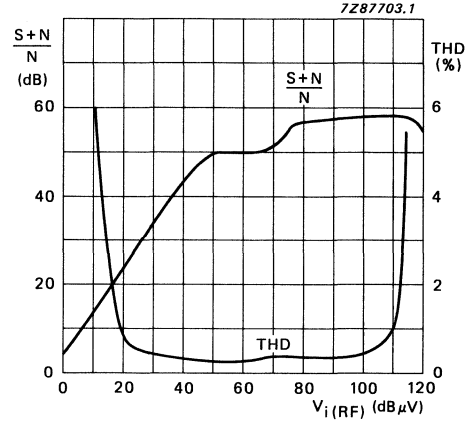


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

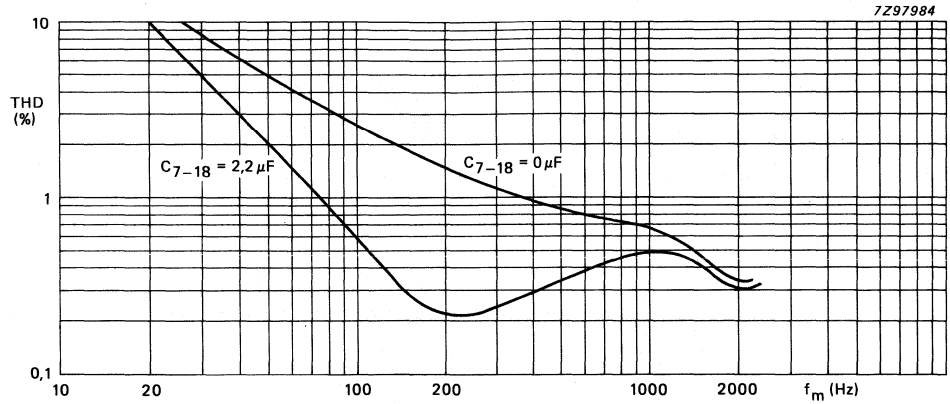


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}18(ext)}$ = 0 μF and 2,2 μF.

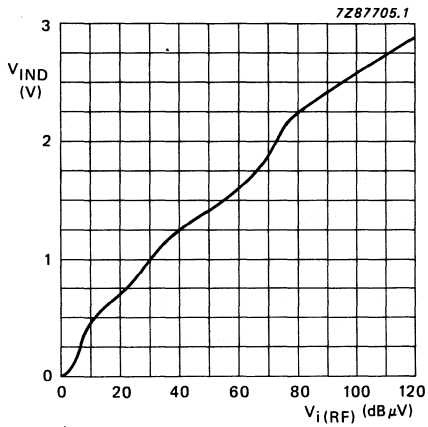


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.

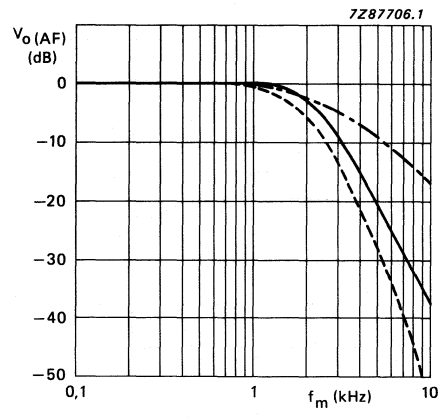


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:

——— with IF filter;
—·—·— with AF filter;
– – – – – with IF and AF filters.

APPLICATION INFORMATION (continued)

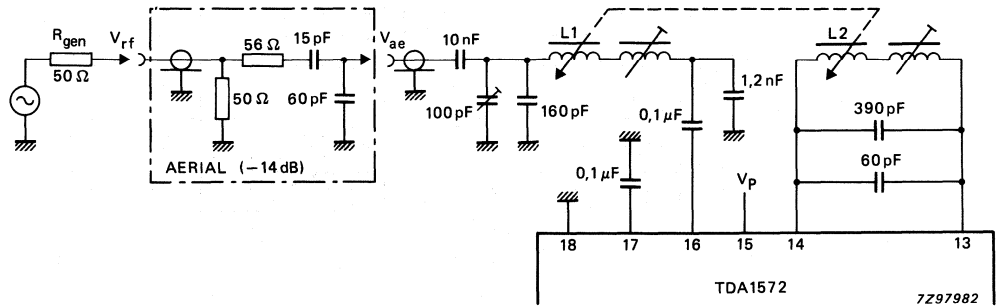


Fig. 8 Car radio application with inductive tuning.

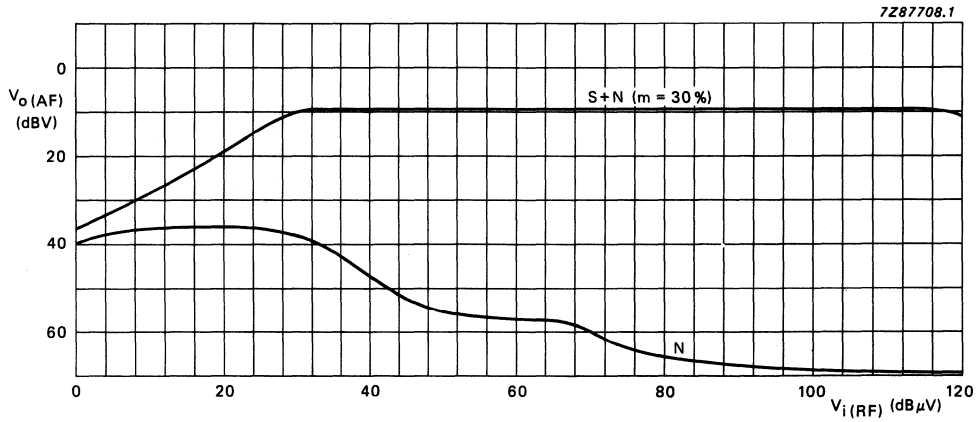


Fig. 9 AF output as a function of RF input using the circuit of Fig. 8 with that of Fig. 1.

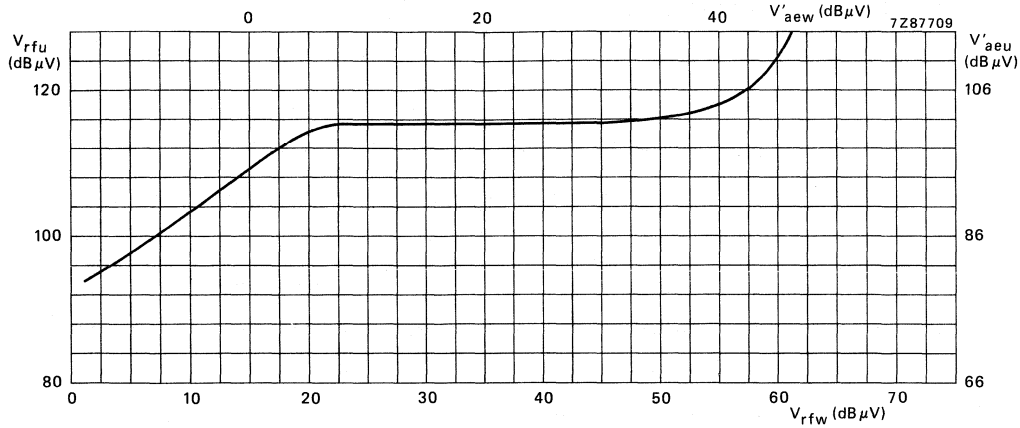


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(AF)}$/Unwanted $V_{o(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

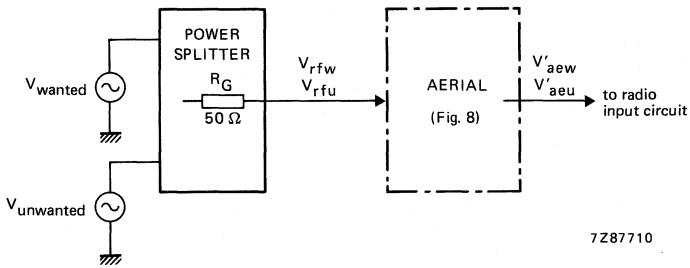


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

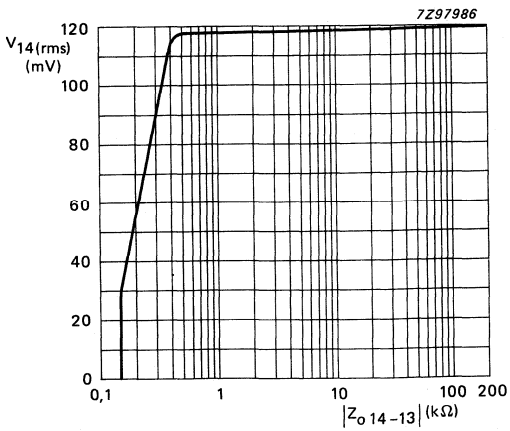


Fig. 12 Oscillator amplitude as a function of pin 13, 14 impedance in the circuit of Fig. 8.

APPLICATION INFORMATION (continued)

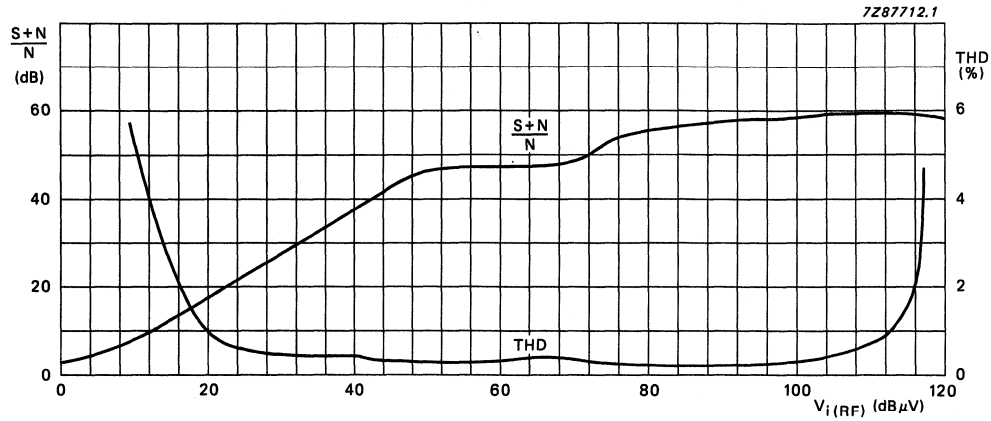


Fig. 13 Total harmonic distortion and (S + N)/N as functions of RF input using the circuit of Fig. 8 with that of Fig. 1.

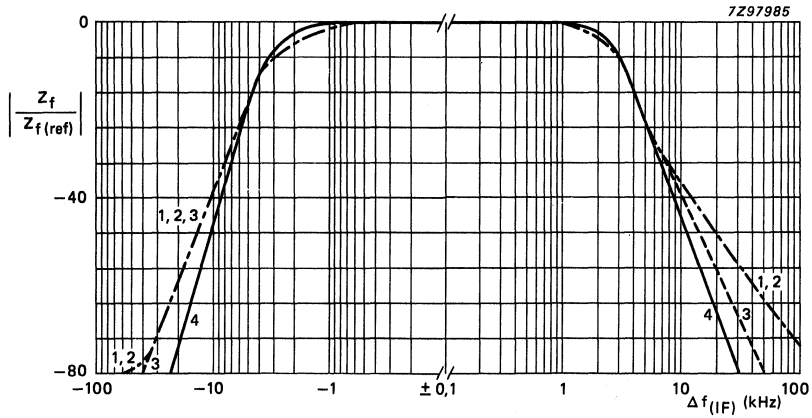


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

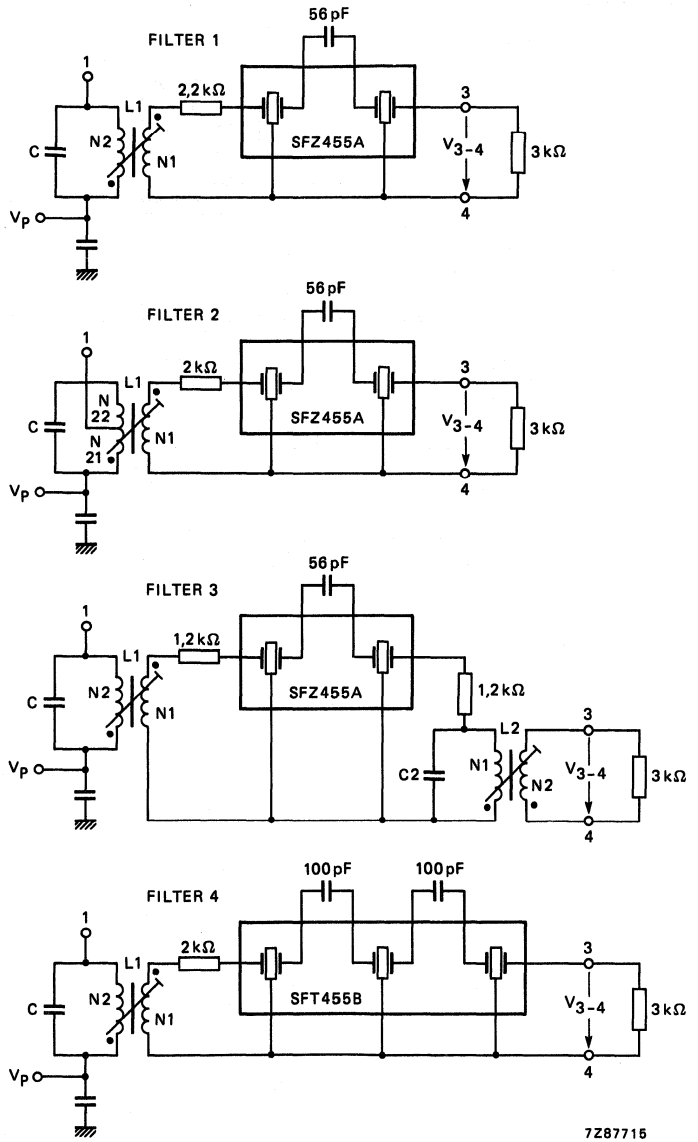


Fig. 15 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

APPLICATION INFORMATION (continued)

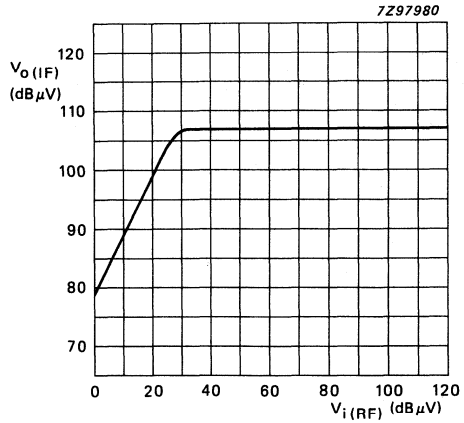
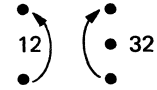
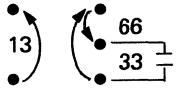
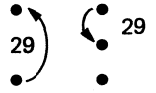


Fig. 16 IF output voltage as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz.

Table 1 Data for IF filters shown in Fig. 15. Criteria for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

AM RECEIVER

GENERAL DESCRIPTION

The TDA1572T integrated AM receiver circuit performs all the active functions and part of the filtering required of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV.

RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The controlled-voltage oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range, even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

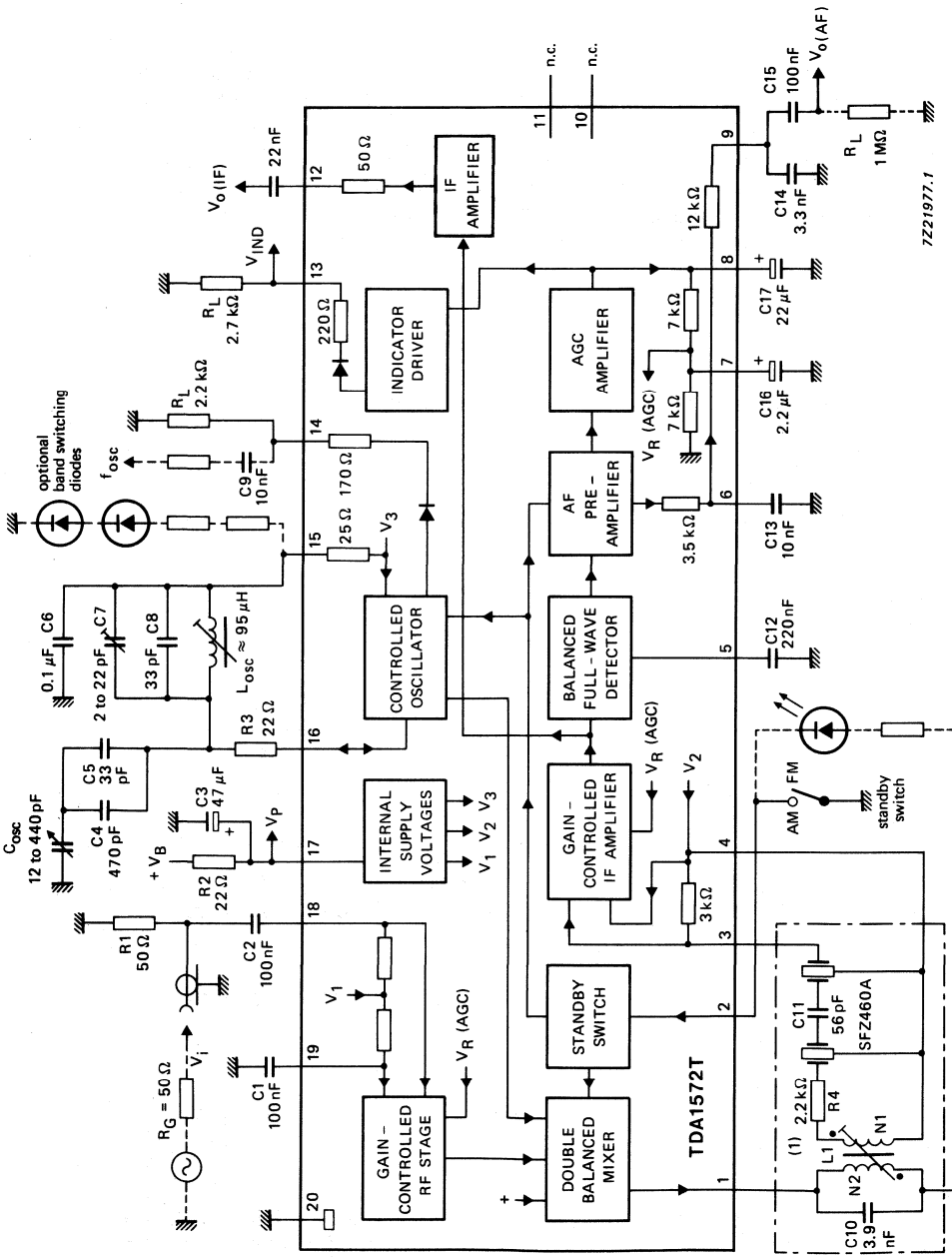
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch
- IF output for stereo demodulator and search tuning

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	8.5	14.0	V
Supply current range	V_P = 8.5 V	I_P	15	25	28	mA
RF input voltage (RMS value)						
for (S + N)/N = 6 dB	m = 30%	$V_{iFR(rms)}$	–	1.5	–	μV
for THD = 3%	m = 80%	$V_{iRF(rms)}$	–	500	–	mV
IF output voltage (RMS value)	V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage (RMS value)	V_i = 2 mV(rms); f_i = 1 MHz; m = 30%; f_m = 400 Hz	$V_{oAF(rms)}$	240	310	390	mV
AGC range						
Change of V_i for 1 dB change of V_{oAF}		ΔV_i	–	86	–	dB
Indicator driver (pin 13)						
Output voltage	V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_O = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4.8 kΩ.

Fig. 1 Block diagram and test circuits (connections shown in broken lines are not part of the test circuits).

DEVELOPMENT DATA

PINNING

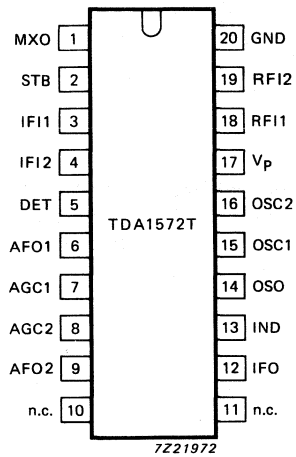


Fig.2 Pinning diagram.

1	MXO	mixer output
2	STB	standby switch
3	IFI1	IF input 1
4	IFI2	IF input 2
5	DET	detector
6	AFO1	AF output 1
7	AGC1	AGC stage 1
8	AGC2	AGC stage 2
9	AFO2	AF output 2
10	n.c.	not connected
11	n.c.	not connected
12	IFO	IF output
13	IND	indicator output
14	OSO	buffered oscillator output
15	OSC1	oscillator 1
16	OSC2	oscillator 2
17	V_P	supply voltage
18	RFI1	RF input 1
19	RFI2	RF input 2
20	GND	ground

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the (S + N)/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the IF output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{15\text{-}20}$. An extra buffered oscillator putput (pin 14) is available for driving a synthesizer. If this is not needed, resistor $R_{L(14)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network. The IF output is available at pin 12.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(13)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and AF preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 17)	$V_P = V_{17-20}$	–	16	V
Input voltage	$\|V_{18-19}\|$	–	12	V
	$-V_{18-19}$; $-V_{19-20}$	–	0.6	V
	V_{18-19}; V_{19-20}	–	V_P	V
Input current (pins 18 and 20)	$\|I_{18}\|$; $\|I_{20}\|$	–	200	mA
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Junction temperature	T_j	–	+125	°C
Electrostatic handling*				
all pins except pins 3, 6, 9, 14	V_{es}	−2000	+2000	V
pins 3, 6, 14	V_{es}	−1500	+2000	V
pin 9	V_{es}	−1000	+2000	V

DEVELOPMENT DATA

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; (5 pulses, both polarities).

CHARACTERISTICS

$V_P = V_{17-20} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig. 1; all voltages referenced to ground; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 17)	V_P	7.5	8.5	14.0	V
Supply current (pin 17)	I_P	15	25	28	mA
RF stage and mixer (pins 18 and 19)					
DC input voltage	V_I	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$ (rms)	Z_i	–	5.5	–	kΩ
RF input capacitance	C_i	–	25	–	pF
RF input impedance at $V_I > 10$ mV (rms)	Z_i	–	8	–	kΩ
RF input capacitance	C_i	–	22	–	pF
IF output impedance (pin 1)	Z_o	200	–	–	kΩ
IF output capacitance	C_o	–	6	–	pF
Conversion transconductance before start of AGC	I_1/V_i	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1 (peak-to-peak value)	$V_{1-17(p-p)}$	–	5	–	V
DC value of output current; at $V_I = 0$ V (pin 1)	I_O	–	1.2	–	mA
AGC range of input stage		–	30	–	dB
RF signal handling capability					
Input voltage (RMS value) for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0.1	–	60	MHz
Voltage amplitude (pins 15 to 16) (RMS value)	$V_{(rms)}$	80	130	150	mV
External load impedance (pins 16 to 15)	$R_{(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation (pins 16 to 15)	$R_{(ext)}$	–	–	60	Ω
Supply voltage ripple rejection at V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log [V_{17}/V_{15}]$)	SVRR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE}) (pin 15)	$V_{15\text{-}20}$	–	4.2	–	V
DC output current (for switching diodes) (pin 15)	$-I_O$	0	–	20	mA
Change of output voltage at ΔI_{15} = 20 mA (switch to maximum load) (pin 15)	ΔV_I	–	0.3	–	V
Buffered oscillator output (pin 14)					
DC output voltage	V_O	–	0.8	–	V
Output signal amplitude (peak-to-peak value)	$V_{o(p\text{-}p)}$	–	320	–	mV
Output impedance	Z_O	–	170	–	Ω
Output current (peak value)	$-I_{O(peak)}$	–	–	3	mA
IF, AGC and AF stages					
DC input voltage (pins 3 and 4)	V_I	–	2.0	–	V
IF input impedance (pins 3 to 4)	Z_i	2.4	3.0	3.9	kΩ
IF input capacitance	C_i	–	7	–	pF
IF input voltage for THD = 3% at m = 80% (pins 3 and 4) (RMS value)	$V_{iIF(rms)}$	–	90	–	mV
IF output impedance (pin 12)	Z_o	–	50	–	Ω
Unloaded IF output voltage at V_i = 10 mV (pin 12) (RMS value)	$V_{oIF(rms)}$	180	230	290	mV
Voltage gain before start of AGC (pins 3 to 4; 6 to 20)	G_v	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV(rms)	ΔV_v	–	55	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
IF, AGC and AF stages (continued)					
AF output voltage (RMS value)					
at $V_{3\text{-}4(IF)}$ = 50 μV(rms)	$V_{oAF(rms)}$	–	130	–	mV
at $V_{3\text{-}4(IF)}$ = 1 mV(rms)	$V_{oAF(rms)}$	–	310	–	mV
AF output impedance (pin 6)	$\|Z_o\|$	2.8	3.5	4.2	kΩ
AF output impedance (pin 9)	$\|Z_o\|$	12.4	15.5	18.6	kΩ
Indicator driver (pin 13)					
Output voltage at V_i = 0 mV(rms); R_L = 2.7 kΩ	V_o	–	–	140	mV
Output voltage at V_i = 500 mV(rms); R_L = 2.7 kΩ	V_o	2.5	2.8	3.1	V
Load resistance	R_L	1.5	–	–	kΩ
Output current at V_i = 500 mV(rms)	$-I_o$	–	–	2.0	mA
Output impedance at $-I_o$ = 0.5 mA	Z_o	–	220	–	Ω
Reverse output voltage at AM off	V_o	–	6	–	V
Standby switch					
Switching threshold at; V_P = 7.5 to 14 V; T_{amb} = −40 to +80 °C					
ON-voltage	$V_{2\text{-}20}$	0	–	2.0	V
OFF-voltage	$V_{2\text{-}20}$	3.5	–	20.0	V
ON-current at $V_{2\text{-}20}$ = 0 V	$-I_2$	–	100	200	μA
OFF-current at $V_{2\text{-}20}$ = 14 V	$\|I_2\|$	–	–	10	μA

DEVELOPMENT DATA

OPERATING CHARACTERISTICS

V_P = 8.5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
RF sensitivity					
RF input voltage (RMS value)					
for (S + N)/N = 6 dB	$V_{iRF(rms)}$	–	1.5	–	μV
for (S + N)/N = 26 dB	$V_{iRF(rms)}$	–	15	–	μV
for (S + N)/N = 46 dB	$V_{iRF(rms)}$	–	150	–	μV
at start of AGC	$V_{iRF(rms)}$	–	30	–	μV
RF large signal handling					
RF input voltage (RMS value)					
at THD = 3%; m = 80%	$V_{iRF(rms)}$	–	500	–	mV
at THD = 3%; m = 30%	$V_{iRF(rms)}$	–	700	–	mV
at THD = 10%; m = 30%	$V_{iRF(rms)}$	–	900	–	mV
AGC range					
Change of V_i for 1 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of V_{oAF}; $V_{i(ref)}$ = 500 mV(rms)	ΔV_i	–	91	–	dB
Output signal					
(RMS value)					
IF output voltage at V_i = 2 mV(rms)	$V_{oIF(rms)}$	180	230	290	mV
AF output voltage					
at V_i = 4 μV(rms); m = 80%	$V_{oAF(rms)}$	–	130	–	mV
at V_i = 2 mV(rms)	$V_{oAF(rms)}$	240	310	390	mV
Total harmonic distortion					
at V_i = 2 mV(rms); m = 30%	THD	–	0.5	–	%
at V_i = 2 mV(rms); m = 80%	THD	–	1.0	–	%
at V_i = 500 mV(rms); m = 30%	THD	–	1.0	–	%
Signal-to-noise ratio at V_i = 100 mV(rms)	(S + N)/N	–	58	–	dB
Supply voltage ripple rejection at V_i = 2 mV(rms) V_P = 100 mV(rms); f_p = 100 Hz ($SVRR = 20 \log[V_P/V_{oAF}]$)	SVRR	–	38	–	dB
(a) additional AF signal at IF output	SVRR	–	0*	–	dB
(b) add modulation at IF output (m_{ref} = 30%)	SVRR	–	40	–	dB

* AF signals at the IF output will be suppressed by a coupling capacitor to the demodulator and by full wave-detection in the demodulator.

OPERATING CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of IF whistles at V_i = 15 μV; m = 0% related to AF signal of m = 30%					
at $f_i \approx 2 \times f_{IF}$	α_{2IF}	–	37	–	dB
at $f_i \approx 3 \times f_{IF}$	α_{3IF}	–	44	–	dB
IF suppression at RF input;					
for symmetrical input	α_{IF}	–	40	–	dB
for asymmetrical input	α_{IF}	–	40	–	dB
Residual oscillator signal at mixer output;					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1.1	–	μA

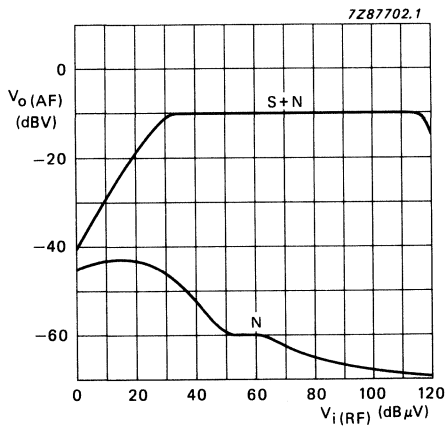


Fig. 3 AF output as a function of RF input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

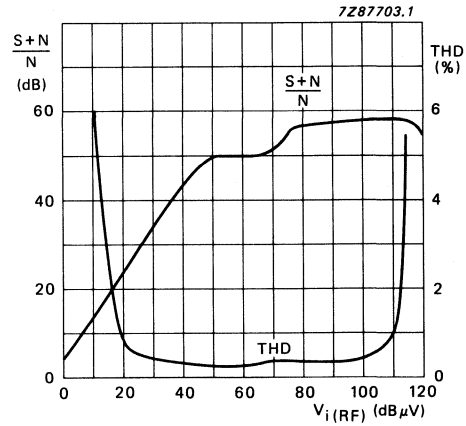


Fig. 4 Total harmonic distortion and (S + N)/N as functions of RF input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

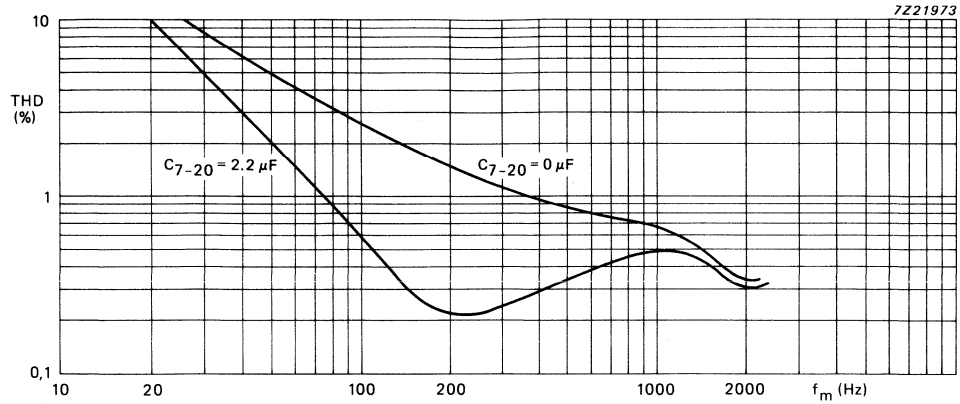


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-20(ext)}$ = 0 μF and 2.2 μF.

DEVELOPMENT DATA

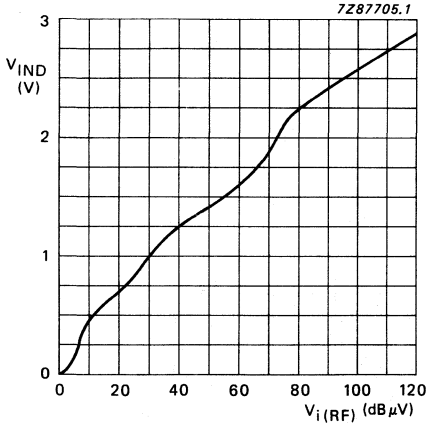
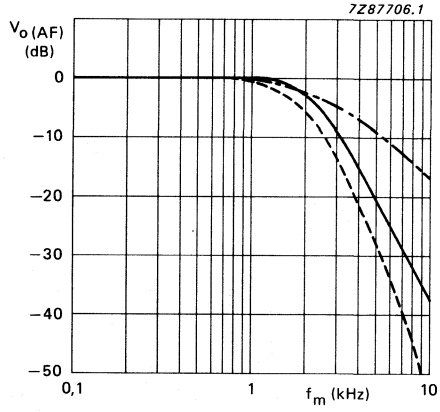


Fig. 6 Indicator driver voltage as a function of RF input in the circuit of Fig. 1.



——— with IF filter;
—·—·— with AF filter;
– – – – – with IF and AF filters.

Fig.7 Typical frequency response curves from Fig.1 showing the effect of filtering.

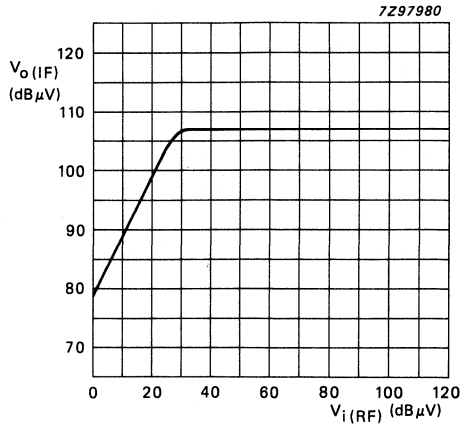


Fig.8 IF output voltage as a function of RF input in the circuit of Fig.1; f_i = 1 MHz.

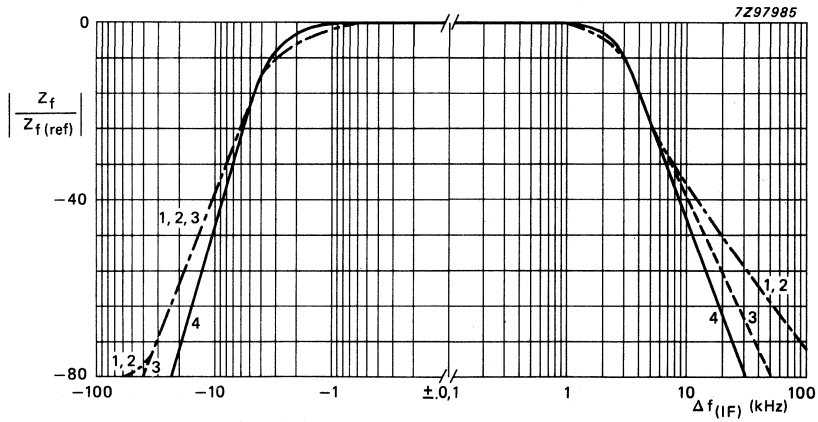


Fig.9 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.10; centre frequency = 455 kHz.

APPLICATION INFORMATION

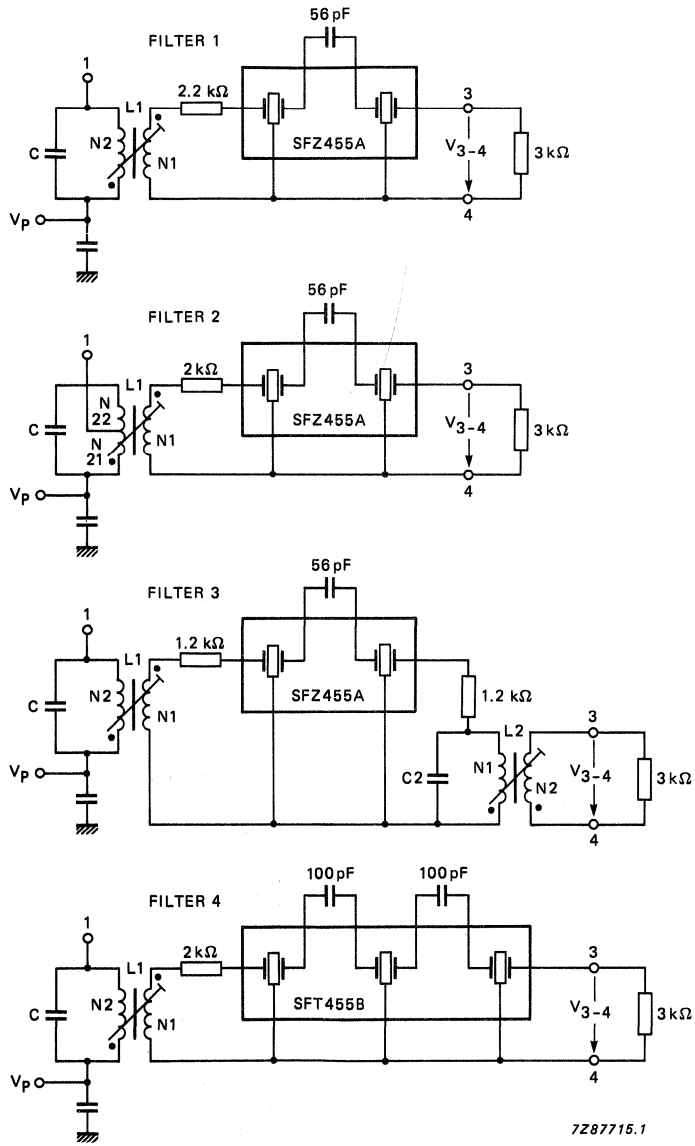


Fig. 10 IF filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

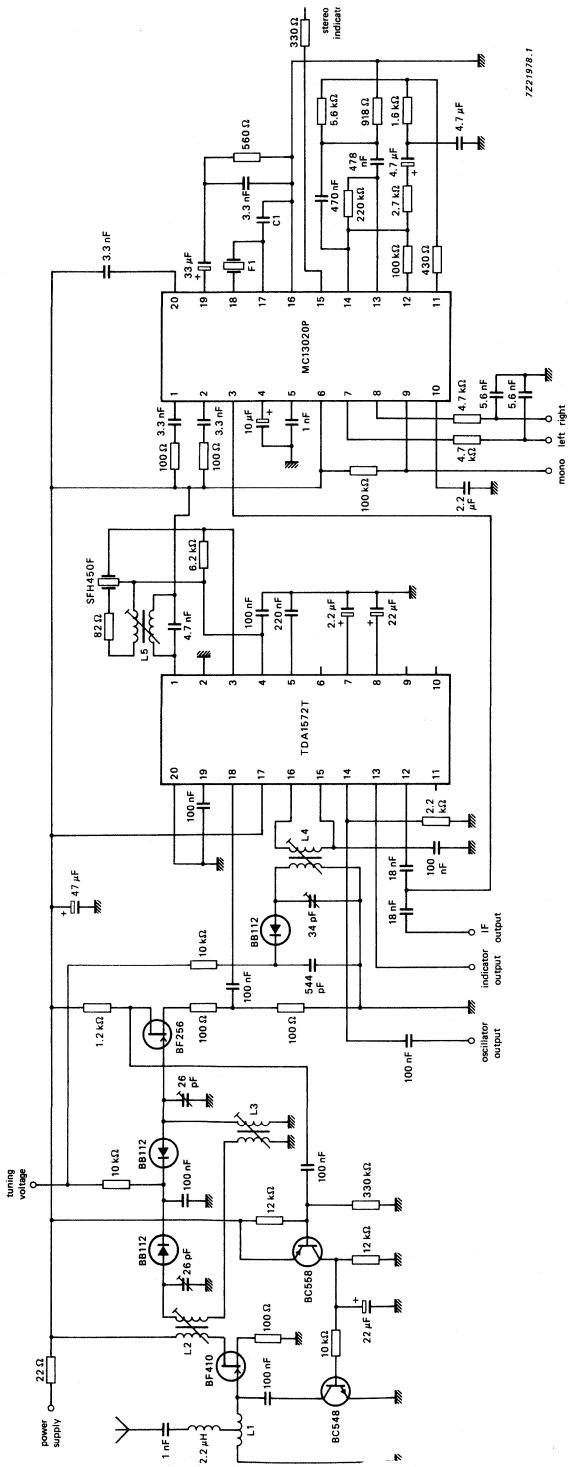


Fig.11 Application diagram.

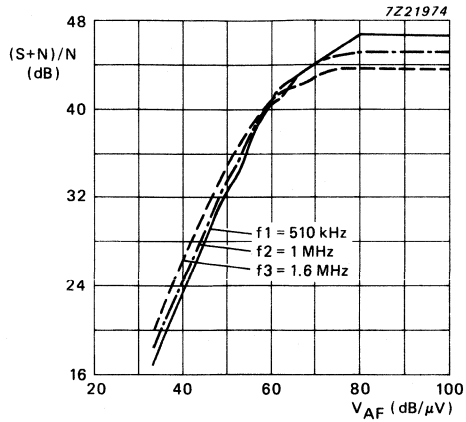


Fig.12 (S + N)/N as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

DEVELOPMENT DATA

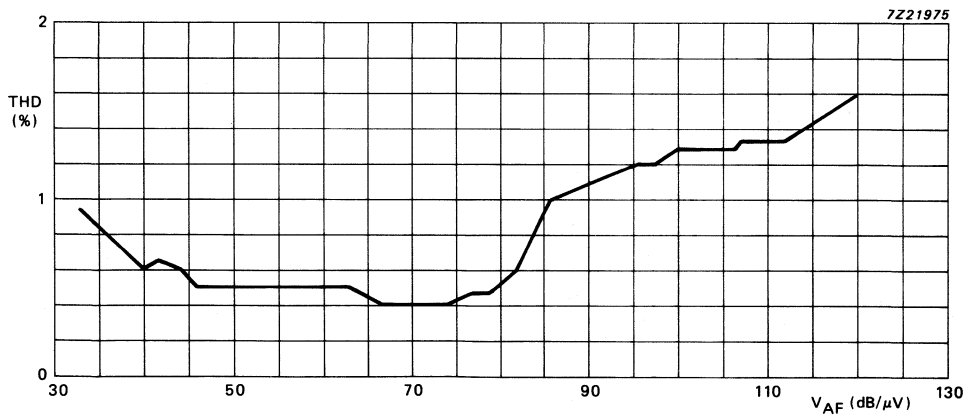


Fig.13 Total harmonic distortion (THD) as a function of input voltage; measured in the circuit of Fig.11 for AM stereo.

filter no.	1	2	3		4	5	unit
Coil data	L1	L1	L1	L2	L1	L1	
Value of C	3900	430	3900	4700	3900	4700	pF
N1 : N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	26 : 32	
Diameter of CU laminated wire	0.09	0.08	0.09	0.08	0.09	0.07	mm
Q_o	65 (typ.)	50	75	60	75	50	
Schematic* of windings	● 12 ● 32 ●	● 13 ● 66 33 ●	● 15 ● 31 ●	● 29 ● 29 ● (N1) (N2)	● 13 ● 31 ●	● 26 ● 32 ●	
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY		
Resonators							
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	SFH450F	
D (typical value)	4	4	4		6	6	dB
R_G, R_L	3	3	3		3	2	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	10	kHz
S_{9kHz}	24	24	24		38		dB
Filter data							
Z_I	4.8	3.8	4.2		4.8	1.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	20	
Z_F	0.70	0.67	0.68		0.68	0.70	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	10	kHz
S_{9kHz}	35	31	36		42		dB
S_{18kHz}	52	49	54		64		dB
S_{27kHz}	63	58	66		74		dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

Table 1 Data for IF filters shown in Fig.10 (Filter 1 to 4) and Fig.11 (Filter 5). Criteria for adjustment is IF = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). Filter 5 is used for AM stereo application with centre frequency f_0 = 450 kHz.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16 V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2-4}$	typ.	1 V
noise figure	NF	typ.	9 dB
Oscillator output voltage (pin 6)	V_{6-4}	typ.	2 V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2 mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V_{9-4}	typ.	6 V
Total harmonic distortion	THD	typ.	−15 dBC
Linear i.f. amplifier output voltage (pin 10)	V_{10-4}	typ.	4,5 V
noise figure at R_S = 300 Ω	NF	typ.	6,5 dB
Keyed a.g.c. output voltage range (pin 18)	V_{18-4}	+ 0,5 to V_P−0,3	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

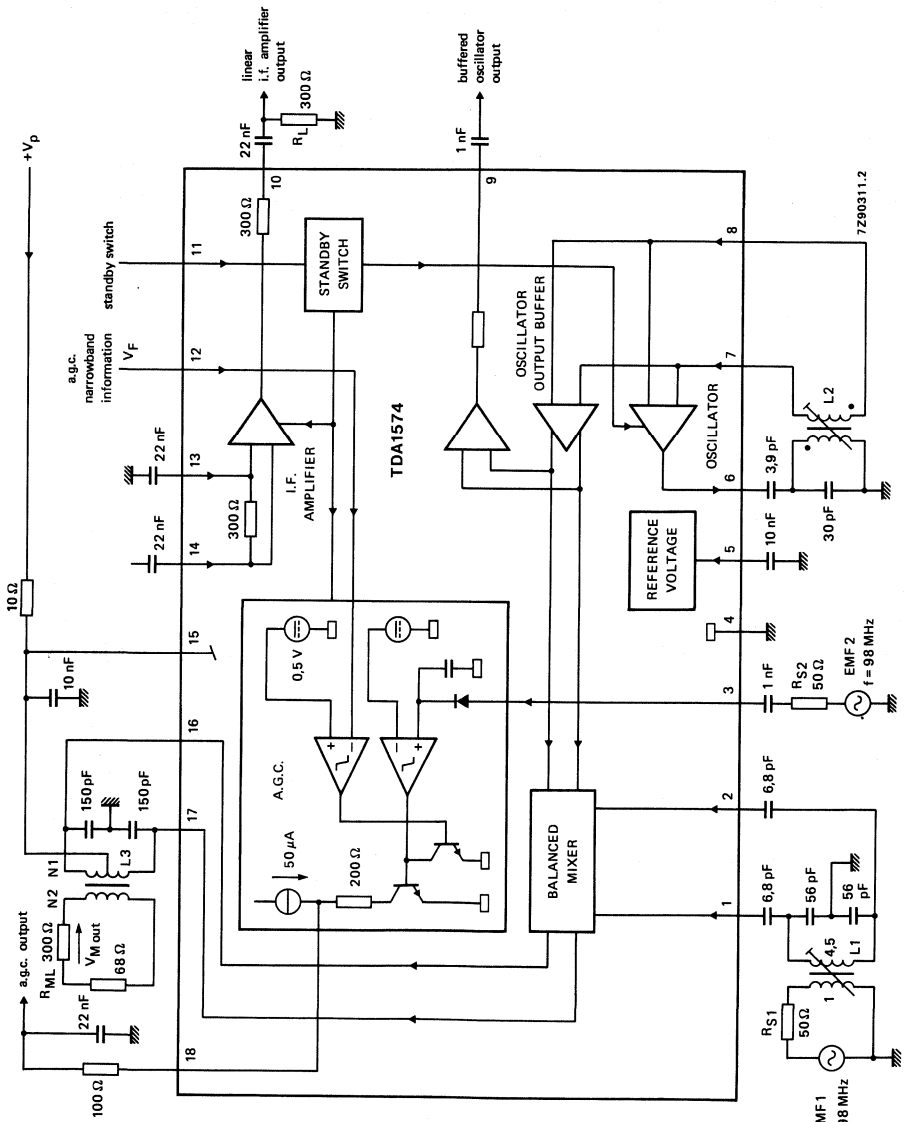


Fig. 1 Block diagram and test circuit.

Coil data

L1: TOKO MC-108, 514HNE-150014S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.
The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrowband AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\ 17-4}$	max.	35	V
Standby switch input voltage (pin 11)	V_{11-4}	max.	23	V
Reference voltage (pin 5)	V_{5-4}	max.	7	V
Field strength input voltage (pin 12)	V_{12-4}	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to +	85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15-4} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	V_{5-4}	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain $10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	–	1,3	–	V
Output voltage (pin 6)	V_{6-4}	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	V_{13-4}	–	1,2	–	V
Output voltage (pin 10)	V_{10-4}	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	R_{14-13}	240	300	360	Ω
	C_{14-13}	–	13	–	pF
Output impedance					
	R_{10-4}	240	300	360	Ω
	C_{10-4}	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10-4}}{V_{14-13}}$	G_{VIF}	27	30	–	dB
T_{amb} = −40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10-4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10-4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	V_{18-4}	0,5	–	V_P−0,3	V
A.G.C. output current					
at I_3 = ϕ or					
V_{12-4} = 450 mV; V_{18-4} = $V_P/2$	$-I_{18}$	25	50	100	μA
at V_{3-4} = 2 V and					
V_{12-4} = 1 V; V_{18-4} = V_{15-4}	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at V_{3-4} = 2 V; V_{12-4} = 550 mV	V_{18-4}	–	–	1	V
at V_{3-4} = 2 V; V_{12-4} = 450 mV	V_{18-4}	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	R_{3-4}	–	4	–	kΩ
	C_{3-4}	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at V_{12-4} = 0,7 V; $V_{18-4} = V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	V_{9-4}	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9-4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9-4(rms)}$	30	50	–	mV
D.C. output impedance	R_{9-15}	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18-4} \geqslant V_P$–3 V	V_{11-4}	0	–	2,3	V
for threshold OFF; $V_{18-4} \leqslant$ 0,5 V	V_{11-4}	3,3	–	23	V
Input current					
at ON condition; V_{11-4} = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; V_{11-4} = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	V_{11-4}	–	–	4,4	V

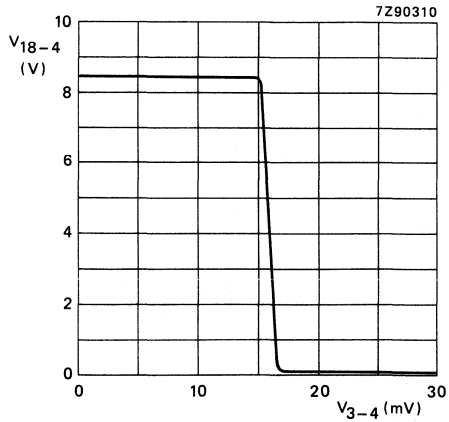


Fig. 2 Keyed a.g.c. output voltage V_{18-4} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at V_{12-4} = 0,7 V; $I_{18} = \phi$.

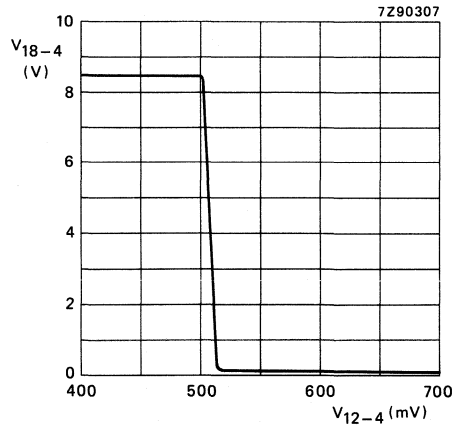


Fig. 3 Keyed a.g.c. output voltage V_{18-4} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at V_{3-4} = 2 V; $I_{18} = \phi$.

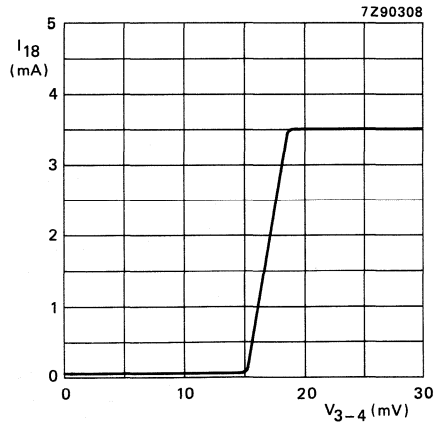


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at V_{12-4} = 0,7 V; V_{18-4} = 8,5 V.

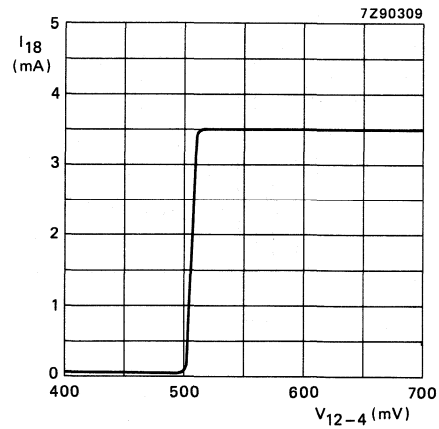


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at V_{3-4} = 2 V; V_{18-4} = 8,5 V.

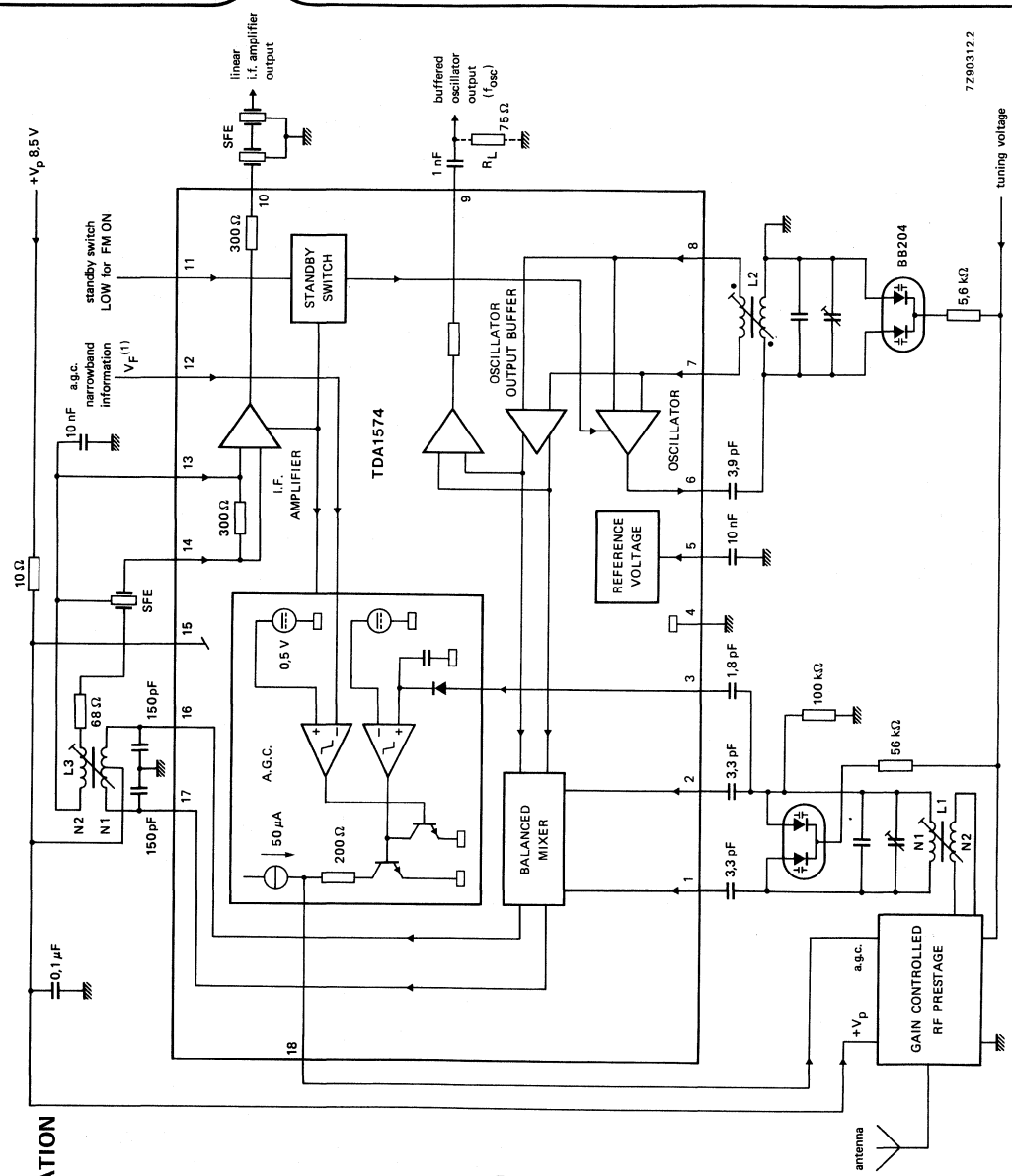


Fig. 6 TDA1574 application diagram.

APPLICATION INFORMATION

Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2: see Fig. 1
L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

INTEGRATED FM TUNER FOR RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

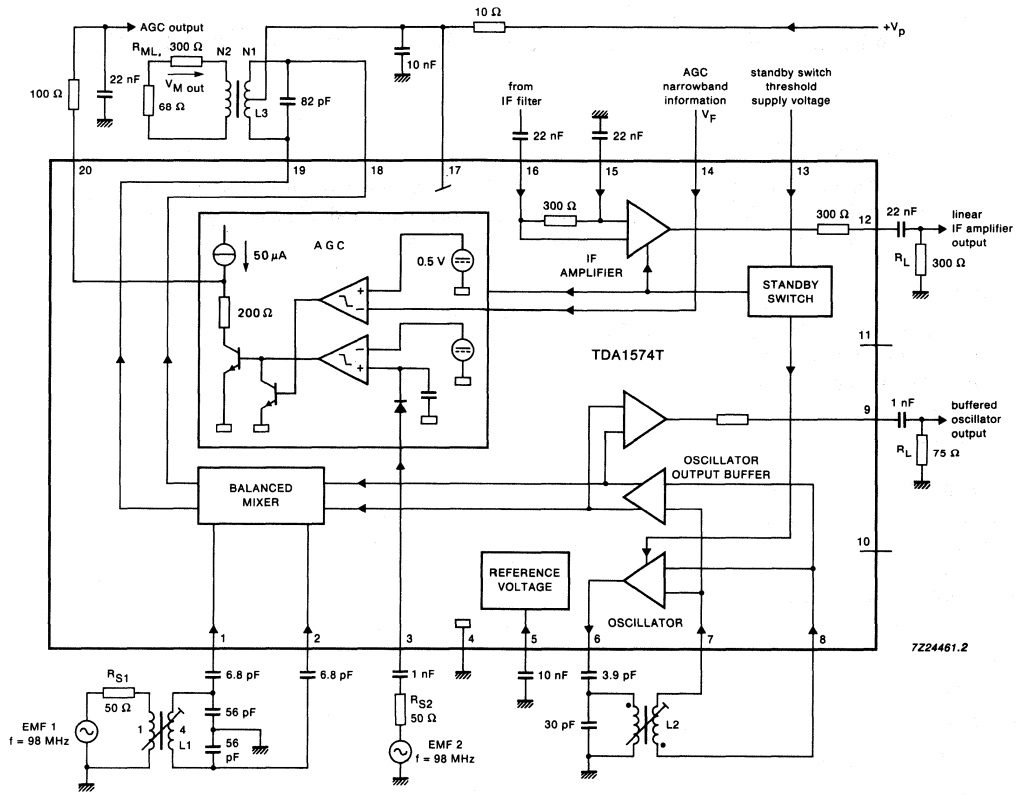
- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2\text{-}4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		$V_{6\text{-}4}$	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		$V_{9\text{-}4}$	–	6	–	V
Total harmonic distortion		THD	–	−15	–	dB
Linear IF amplifier output voltage (pin 12)		$V_{12\text{-}4}$	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		$V_{20\text{-}4}$	0.5	–	V_P−0.3	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 µH
L2: TOKO MC-111, E516HNS-200057; L = 0.08 µH
L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

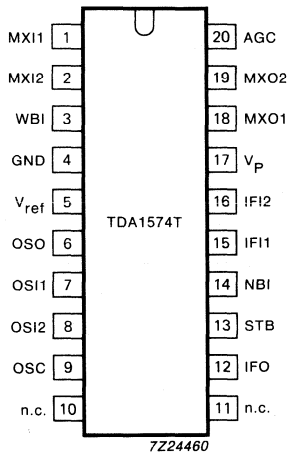


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.

The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		V_{17-4}	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19-4}$	–	35	V
Standby switch input voltage (pin 13)		V_{13-4}	–	23	V
Reference voltage (pin 5)		V_{5-4}	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j-a} = 95$ K/W

Note to the ratings

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{17-4} = 8.5$ V; $T_{amb} = 25$ °C; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$	240	300	360	Ω
		$C_{16\text{-}15}$	–	13	–	pF
Output impedance		R_{12}	240	300	360	Ω
		C_{12}	–	3	–	pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = –40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P–0.3	V
AGC output current at I_3 = 0 or V_{14} = 450 mV; V_{20} = V_P/2		$-I_{20}$	25	50	100	μA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P–0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3	–	4	–	kΩ
		C_3	–	3	–	pF

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at V_{14} = 0.7 V; $V_{20} = V_P/2$; $I_{20} = 0$		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at R_L = 75 Ω		$V_{9(rms)}$	30	50	–	mV
DC output resistance		R_{9-17}	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; R_{S1} = 50 Ω		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} = > V_P - 3$ V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} = < 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	V_{13} = 0 V	$-I_{13}$	–	–	150	μA
at OFF condition	V_{13} = 23 V	$-I_{13}$	–	–	10	μA
Input voltage	I_{13} = 0	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

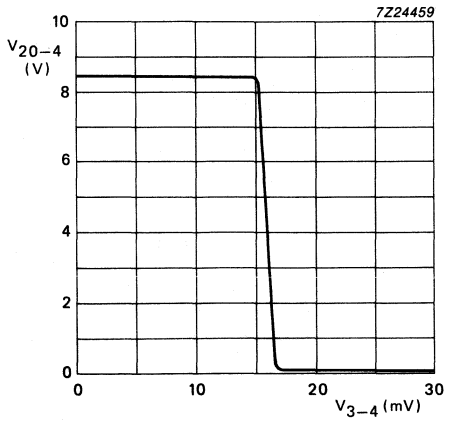


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

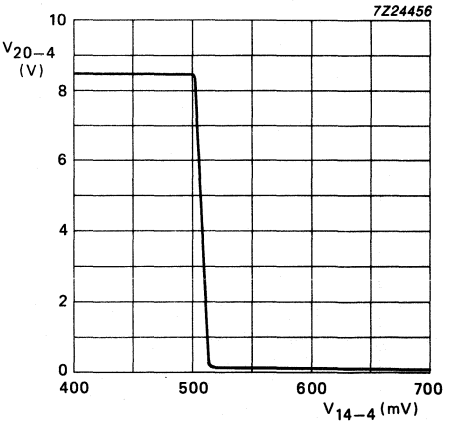


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

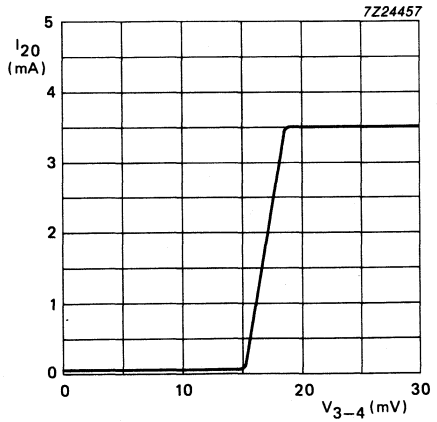


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

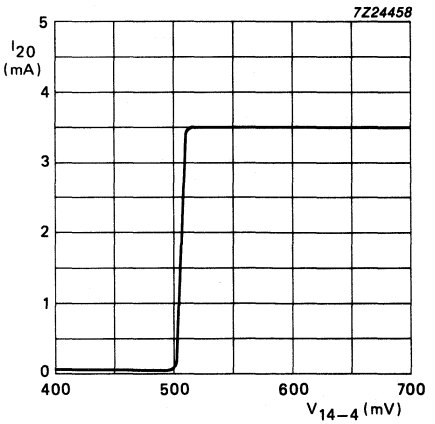
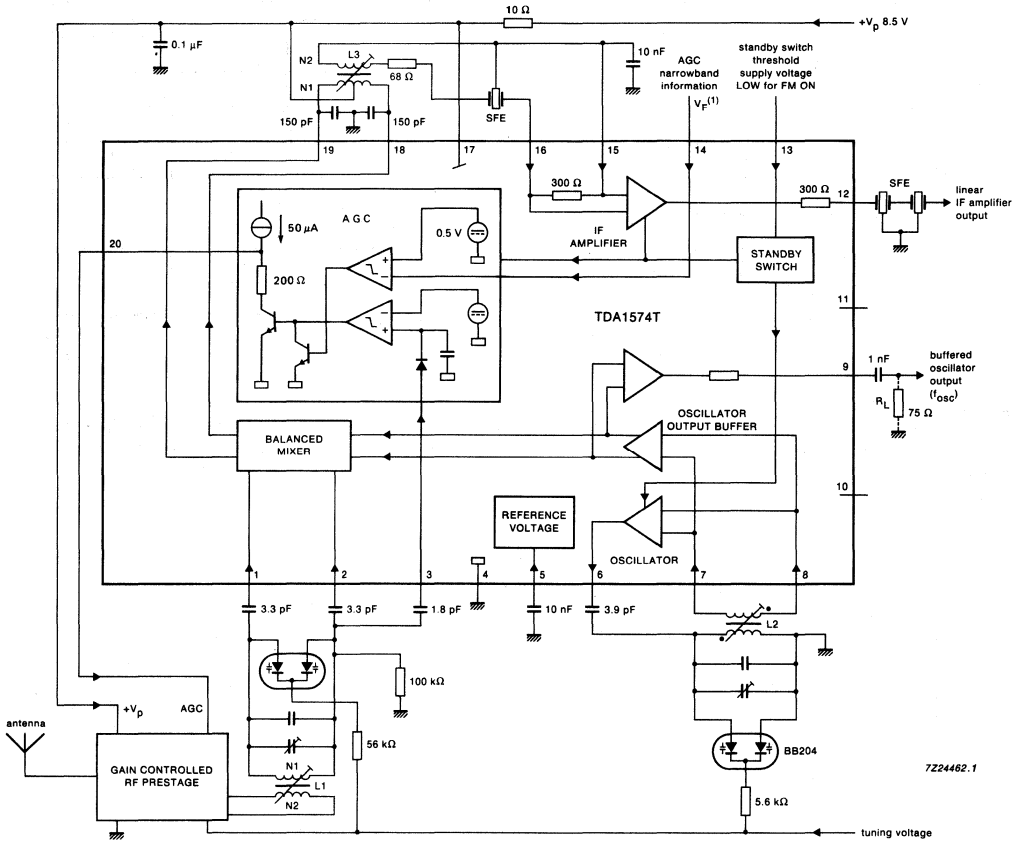


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn

L2: } see Fig.1
L3: }

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

Philips Components

Data sheet	
status	Product specification
date of issue	October, 1990

TDA1575T
FM tuner circuit

FEATURES

- Bipolar integrated FM tuner circuit, designed for use in car radios and home receivers
- Radio frequency range of 76 to 90 MHz (Japan) or 87.5 to 108 MHz (Europe, USA)
- Low noise oscillator, buffered oscillator output
- Double balanced mixer
- Internal buffered mixer driving
- Linear IF amplifier, suitable for ceramic IF filters
- Regulated reference voltage

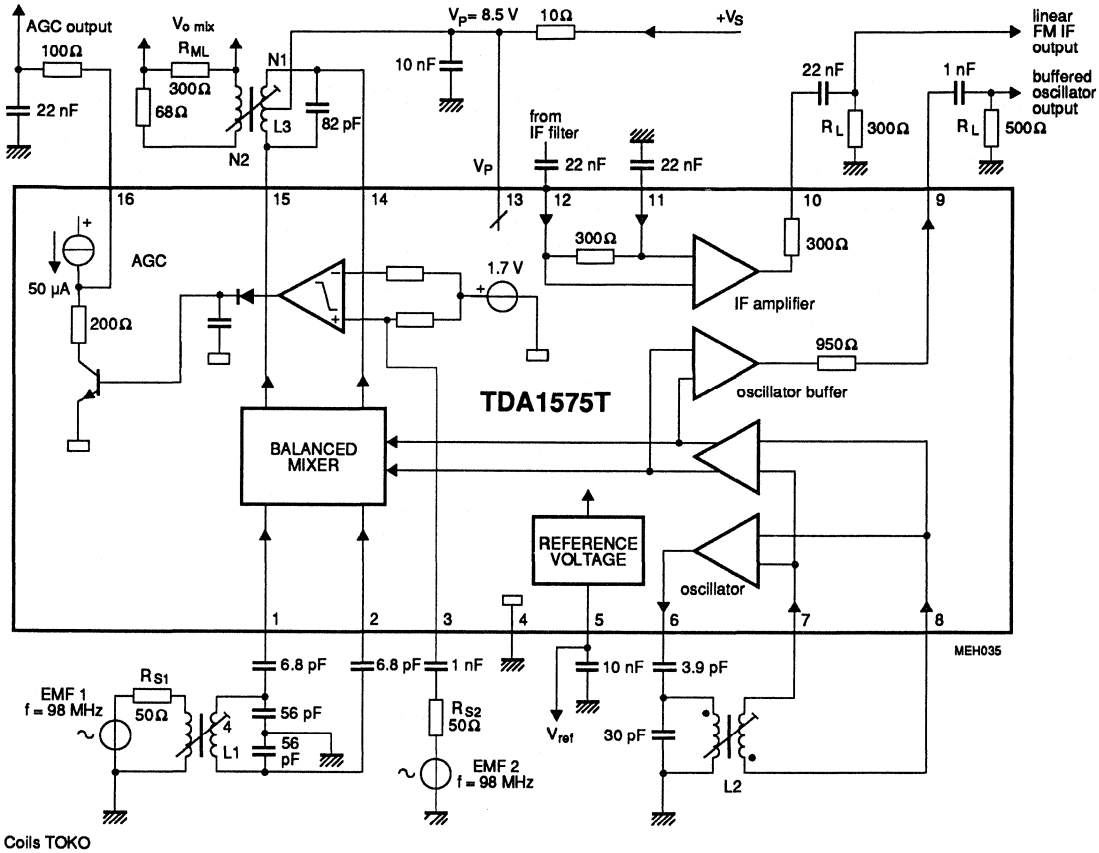
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	7	8.5	10	V
I_P	supply current, without mixer	-	23	-	mA
V_{ref}	reference voltage output	-	4.2	-	V
Z_I	mixer input impedance	-	14	-	Ω
NF	noise figure of mixer	-	9	-	dB
EMF1	3rd order intermodulation	-	115	-	dBμV
V_{osc}	oscillator buffer output signal (RMS value)	75	-	-	mV
THD	total harmonic distortion	-	–15	-	dBC
G_v	IF gain	-	30	-	dB
NF	IF noise figure	-	6.5	-	dB
Z_I	IF input impedance	-	300	-	Ω
Z_O	IF output impedance	-	300	-	Ω
EMF2	AGC wideband threshold (RMS value)	-	17	-	mV

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1575T	16	mini-pack	plastic	SOT109A

FM tuner circuit TDA1575T



Coils TOKO
L1: MC-108 514 HNE-150023 S14; L = 78 nH, N = 4 turns
L2: MC-111 E516 HNS-200057; L = 80 nH
L3: coil set 7P; N1 = 5.5 + 5.5 turns; N2 = 4 turns

Fig.1 Block diagram and test circuit.

FM tuner circuit TDA1575T

PINNING

SYMBOL	PIN	DESCRIPTION
MIXI1	1	RF input 1 to mixer
MIXI2	2	RF input 2 to mixer
AGCI	3	HF input to automatic gain control
GND	4	ground (0 V)
V_{ref}	5	reference voltage output
OSCO	6	oscillator output
OSCI1	7	oscillator input 1
OSCI2	8	oscillator input 2
LO	9	buffered oscillator output
IFO	10	linear FM IF output
IFI1	11	FM IF input 1
IFI2	12	FM IF input 2
V_P	13	supply voltage (+8.5 V)
MIXO1	14	mixer output 1
MIXO2	15	mixer output 2
AGCO	16	automatic gain control output

PIN CONFIGURATION

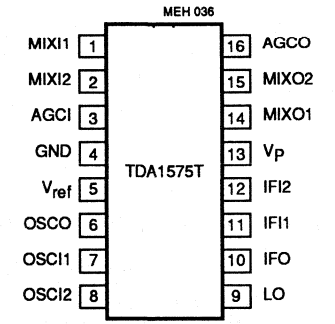


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13)	0	12	V
$V_{14, 15}$	voltage at mixer output	0	V_P	V
P_{tot}	total power dissipation	0	380	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{ESD}	electrostatic handling*			
	all pins except 3 and 10	-	±2000	V
	pin 3	-	+2000	V
		-	−1000	V
	pin 10	-	+1500	V
		-	−2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V and T_{amb} = 25 °C, measurements taken in Fig.1 with f_o = 98 MHz (EMF1) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 13)		7	8.5	10	V
I_P	supply current	without mixer	16	23	30	mA
V_{ref}	reference voltage (pin 5)	$I_5 \leq 3$ mA	3.9	4.2	4.4	V
Mixer		EMF1 = 98 MHz				
I_{14+15}	mixer supply current (pins 14 and 15)		-	4	-	mA
$V_{1,2}$	DC voltage input (pins 1 and 2)		-	1	-	V
$Z_{1,2}$	input impedance		-	14	-	Ω
$V_{14,15}$	DC output voltage (pins 14 and 15)		4	-	10	V
$C_{14,15}$	output capacitance		-	13	-	pF
G_P	conversion power gain	note 1	-	14	-	dB
EMF1 $_{IP3}$	3rd order intercept point		-	115	-	dBμV
NF	noise figure total noise figure	 including transforming network	- -	9 11	- -	dB dB
Oscillator		f_{osc} = 108.7 MHz				
$V_{7,8}$	DC input voltage (pins 7 and 8)		-	1.3	-	V
V_6	DC output voltage (pin 6)		-	2.0	-	V
Δf	residual FM at pin 6	f = 300 to 15000 Hz; de-emphasis 50 μs	-	2.2	-	Hz
Oscillator buffered output (pin 9)						
V_o	output signal (RMS value)	R_L = 500 Ω; C_L = 2 pF	75	-	-	mV
V_9	DC output voltage		-	6	-	V
R_9	DC output resistor		-	950	-	Ω
THD	total harmonic distortion		-	–15	-	dBC
f_S	spurious frequencies	EMF1 = 2 V; R_S = 50Ω f_{osc} = 108.7 MHz	-	–37	-	dBC
Automatic gain control (AGC)		f_i = 98 MHz				
R_3	input resistance (pin 3)		-	4	-	kΩ
C_3	input capacitance		-	3	-	pF
V_{16}	AGC output swing (DC)	Fig.3 and 4	0.5	-	V_P–0.3	V
I_{16}	output current at I_3 = 0 output current at U_3 = 2 V	V_{16} = 1/2 V_P V_{16} = 7 to 10 V	–25 2	–50 -	–150 5	μA mA
EMF2	threshold (RMS value), see figures 4 and 5	I_{16} = 0; V_{16} = 1/2 V_P	-	17	-	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linear IF amplifier		IF = 10.7 MHz				
$V_{11, 12}$	DC input voltage (pins 11 and 12)		-	1.25	-	V
Z_{12-11}	input impedance		240	300	360	Ω
C_{12-11}	input capacitance		-	13	-	pF
V_{10}	DC output voltage (pin 10)		-	4.4	-	V
Z_{10}	output impedance		240	300	360	Ω
C_{10}	output capacitance		-	3	-	pF
V_o	output signal (RMS value)	−1 dB compression	-	-	650	mV
G_v	IF voltage gain (20 log (V_{10-4} / V_{12-11}))		27	30	-	dB
ΔG_v	IF voltage gain deviation	T_{amb} = −40 to +85 °C	-	0	-	dB
NF	noise figure	R_S = 300 Ω	-	6.5	-	dB

Note to the characteristics

1. $G_P = 10 \log (4V_{o\ mix} \times 10{,}7\ MHz) / (EMF2 \times 98\ MHz)^2 \times (R_{S1} / R_{ML})$

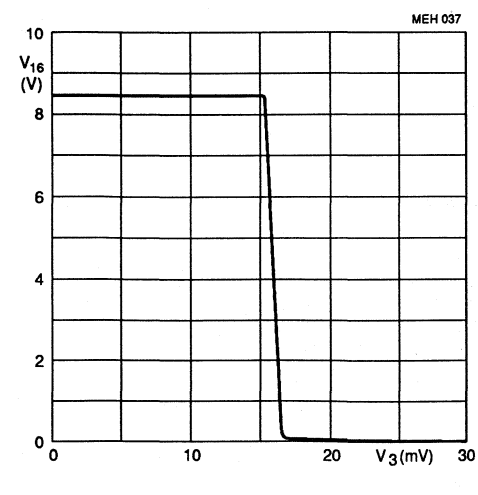


Fig.3 AGC output voltage V_{16} as a function of $V_{i\ 3\ (rms)}$ at I_{16} = 0, measured in test circuit Fig.1.

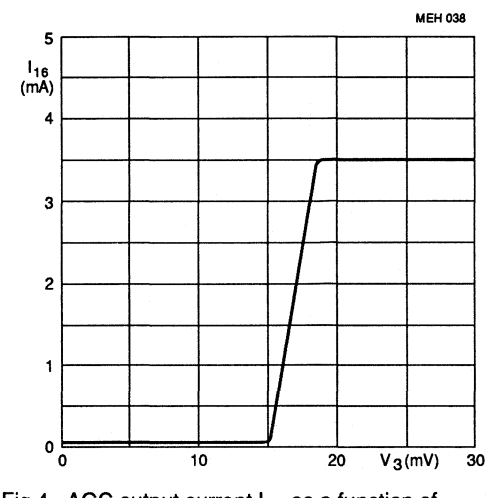


Fig.4 AGC output current I_{16} as a function of $V_{i\ 3\ (rms)}$ at V_{16} = 8.5 V, measured in test circuit Fig.1.

APPLICATION INFORMATION

Operating characteristics

Measurements taken with figure 6, according to "Amtsblatt 69, Kapitel 5.1.1. (Eingangs-Störfestigkeit). Measurements are shown in figure 7.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage (range in brackets)		(7)	8.5	(10)	V
I_S	total supply current			37		mA
f_{RF}	tuning range of RF input		87.5	-	108	MHz
V_{tune}	tuning voltage of RF input		1	-	7	V
G	gain (20 log $V_{o\ IF}$ / V_{ant})		-	43	-	dB
$V_{i\ ant}$	input sensivity	S/N = 26 dB; R_{ant} = 150 Ω	-	3	-	µV
IR	image rejection	f = 98 MHz	-	58	-	dB
RSS	repeat spot suppression	f = 98 MHz; $V_{i\ ant}$ = 10 µV	-	95	-	dB
DBS	double beat suppression	f1 = 93 MHz; f2 = 98 MHz				
	DBS1	f_{tune} = 88 MHz	-	82	-	dB
	DBS2	f_{tune} = 103 MHz	-	73	-	dB
	DBS3	f_{tune} = 90.15 MHz	-	88	-	dB
CBS	continous beat suppression	f1 = 90 MHz; f2 = 100.7 MHz				
		f_{tune} = 95 MHz	-	87	-	dB

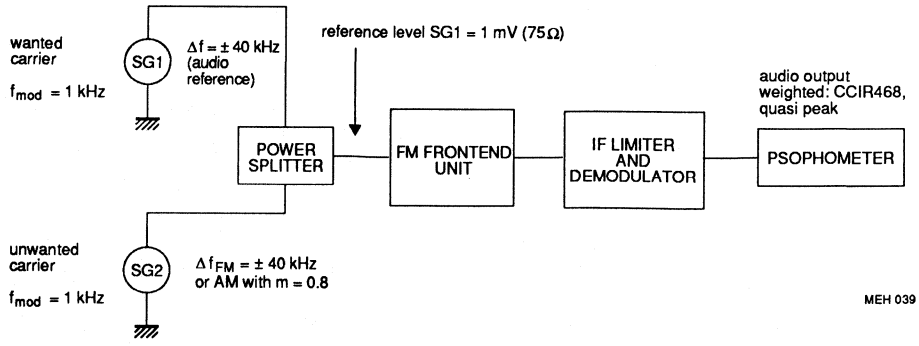


Fig.5 Set-up for "Amtsblatt" measurments.

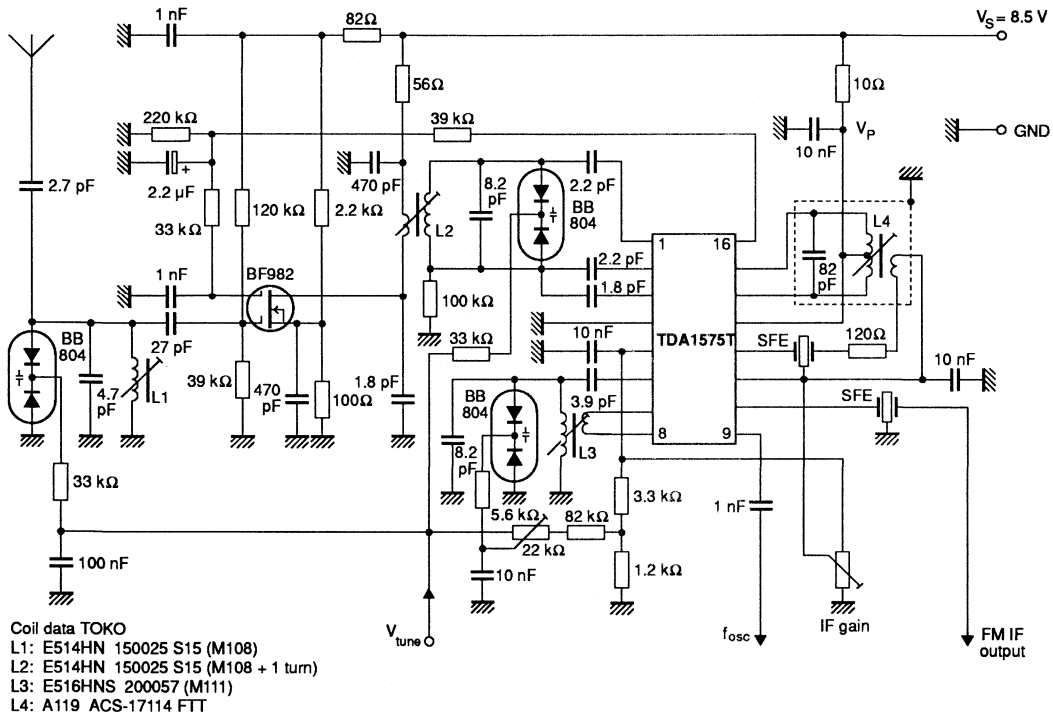
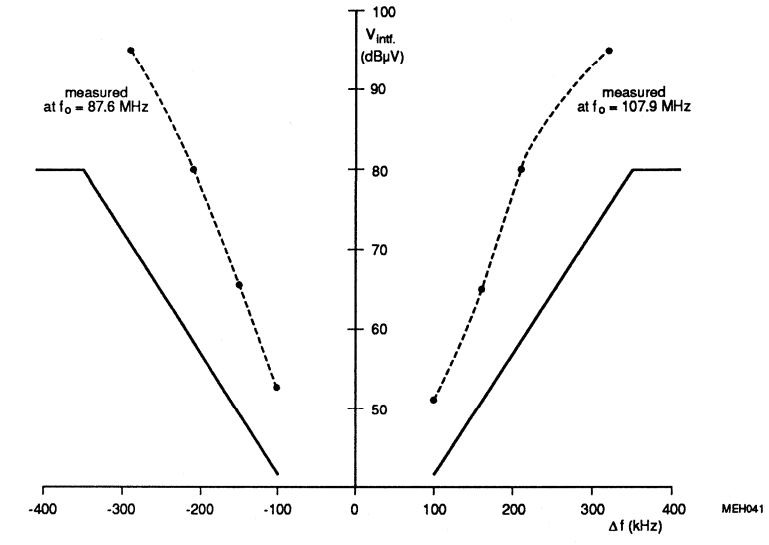


Fig.6 Application circuit of a FM-Tuner with TDA1575T and FET-preamplifier.



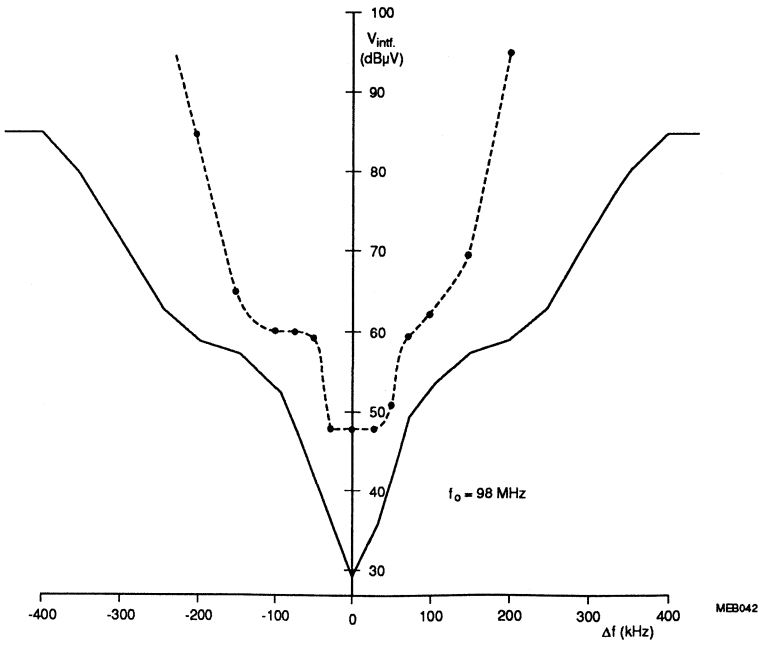


Fig.7 Interference level V_{intf} as a function of detuning for S/N = 26 dB; interference-carrier AM-modulated according to "Amtsblatt 69".

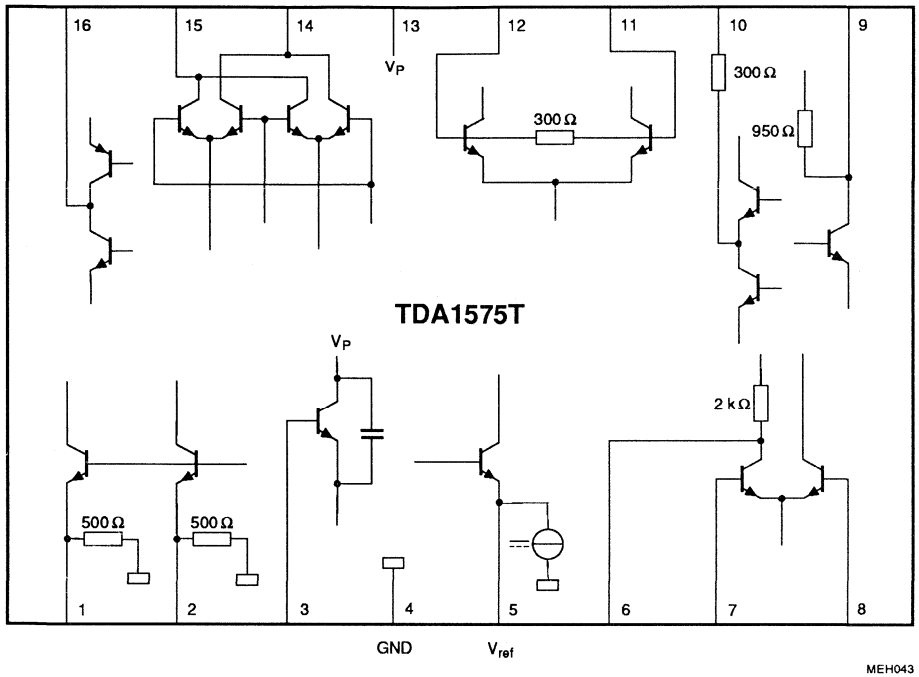


Fig.8 Internal circuits.

DECODER FOR TRAFFIC WARNING (VWF) RADIO TRANSMISSIONS

GENERAL DESCRIPTION

The TDA1579 decoder is for radio transmissions having 57 kHz amplitude-modulated subcarriers as used in the German 'Verkehrs Warnfunk' (VWF) traffic warning system.

Features

- Selective subcarrier amplifier (57 kHz) with gain control
- Transmitter identification signal (SK) decoder
- Area identification signal (BK) and announcement identification signal (DK) active filtering
- BK and DK decoders (Schmitt trigger with switched hysteresis)
- BK and DK switch-on/switch-off delay circuits
- Driver output for SK indicator (LED)
- SK and BK control outputs

QUICK REFERENCE DATA

Measured in Fig. 1 at V_{iSK} = 8 mV; f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	7.5	8.5	12	V
Supply current		I_P	–	6	–	mA
Nominal input voltage	at f = 57 kHz	V_{iSK}	–	8	–	mV
Input impedance	at f ≤ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Control level	–3 dB	V_{iSK}	–	2.4	–	mV
Input voltage	peak-to-peak value	$V_{i(p-p)}$	2	–	–	V
SK switch-on threshold level		m_{BKon}	–	42	–	%
SK switch hysteresis		Δm_{BK}	–	3.5	–	dB
SK switch-on delay		t_{dSKon}	–	150	–	ms
SK switch-off delay		t_{dSKoff}	–	750	–	ms
DK switch-on threshold level		m_{DKon}	–	13	–	%
DK switch hysteresis		Δm_{DK}	–	3.6	–	dB
DK switch-on delay		t_{dDKon}	–	750	–	ms
DK switch-off delay		t_{dDKoff}	–	750	–	ms
Ambient operating temperature range		T_{amb}	–30	–	+ 80	°C

PACKAGE OUTLINES

TDA1579: 18-lead DIL; plastic (SOT102).
TDA1579T: 20-lead mini-pack; plastic (SO20; SOT163A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
All pin numbers in this table apply to TDA1579; for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	$V_P = V_{7\text{-}18}$	–	–	18	V
Switch output voltage	pin 1	$V_{1\text{-}18}$	–	–	23	V
	pins 2 or 3	$V_{2;3\text{-}18}$	–	–	18	V
	pins 1, 2 or 3	$-V_{1;2;3\text{-}18}$	–	–	0.5	V
Switch output current	pin 1	I_1	–	–	50	mA
	pins 2 or 3	$I_{2;3}$	–	–	5	mA
	pins 1, 2 or 3	$-I_{1;2;3}$	–	–	10	mA
Signal input voltage	pin 13	$V_{13\text{-}18}$	–	–	V_P	
	pin 13	$-V_{13\text{-}18}$	–	–	0.5	V
Signal input current	pin 13	$-I_{13}$	–	–	10	mA
Total power dissipation		P_{tot}	–	–	800	mW
Storage temperature range		T_{stg}	−55	–	+ 150	°C
Operating ambient temperature range		T_{amb}	−30	–	+ 80	°C

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; measured at nominal input signal: V_{iSK} = 8 mV, f = 57 kHz amplitude modulated with f_m = 34.95 Hz and m = 60% for 'BK-traffic area C' signal; or with f_m = 125 Hz and m = 30% for DK signal.
All pin numbers in this table apply to TDA1579, for TDA1579T refer to Fig. 1.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 7	V_P	7.5	–	12	V
Supply current	pin 7	I_P	–	6	10	mA
SK amplifier/decoder						
Input impedance	f ⩽ 57 kHz	$\|Z_i\|$	100	–	–	kΩ
Input voltage (peak-to-peak value)		$V_{i(p\text{-}p)}$	2	–	–	V
Input voltage at start of gain control	V_{o9BK} = −3 dB	V_{iSK}	–	2.4*	–	mV
Voltage gain	V_{9BK}/V_{13SK}	$G_{v9\text{-}13}$	–	44*	–	dB

* Selectable by $R_{12\text{-}8}$ or $Z_{10\text{-}8}$.

parameter	conditions	symbol	min.	typ.	max.	unit
SK amplifier/decoder (continued)						
Gain spread		$\pm \Delta G_{v9\text{-}13}$	–	–	2	dB
Gain control range		ΔG_v	40	–	–	dB
Controlled output voltage		V_{o9BK}	–	440	–	mV
		V_{o9DK}	–	220	–	mV
BK circuit						
Switch-on threshold level	pin 3 high-Z	V_{o5BKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{o5BKon}}{V_{o5BKoff}}$	3	3.5	4	dB
BK switch threshold level for BK-off (SK-off) (typ. value = $0.21V_{8\text{-}18}$)	pin 3 conducting	$V_{4\text{-}18off}$	0.8	0.88	0.97	V
SK output (pin 3)						
allowable load current		I_3	–	–	1.5	mA
saturation voltage	I_3 = 1.5 mA	$V_{3\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_3 < 5\ \mu A$	$V_{3\text{-}18}$	18	–	–	V
Indicator driver (pin 1)						
allowable load current		I_1	–	–	40	mA
saturation voltage	I_1 = 20 mA	$V_{1\text{-}18sat}$	–	–	0.8	V
rejection voltage	$I_1 < 10\ \mu A$	$V_{1\text{-}18}$	23	–	–	V
DK circuit						
Switch-on threshold level	pin 2 high-Z	V_{15DKon}	600	670	750	mV
Switch hysteresis		$\frac{V_{15DKon}}{V_{15DKoff}}$	3.1	3.6	4.1	dB
DK switch threshold level for DK-off (Schmitt trigger output) (typ. value = 1 x V_{BE})	pin 2 conducting	$V_{16\text{-}18off}$	–	0.6	–	V
DK output (pin 2)						
allowable load current		I_2	–	–	1.5	mA
saturation voltage	I_2 = 1.5 mA	$V_{2\text{-}18sat}$	–	–	0.35	V
rejection voltage	$I_2 < 5\ \mu A$	$V_{2\text{-}18}$	18	–	–	V
BK and DK filter amplifiers						
Open loop gain	f = 100 Hz	G_o	84	–	–	dB
Current gain		G_i	120	–	–	dB
Input bias current		$\pm I_i$	–	–	50	nA
Output offset voltage	$R_{5\text{-}6} = R_{14\text{-}15}$ = 680 kΩ	$\pm V_{o5\text{-}8}$ / $\pm V_{15\text{-}8}$	–	–	50	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BK and DK filter amplifiers (continued)						
Available output current		$\pm I_o$	1	–	–	mA
Output resistance		R_o	–	2	3.5	kΩ
Allowable load capacitance		C_L	–	–	50	pF
Internal reference voltage						
Output voltage (typ. value = 0.5 V_P)		$V_{8\text{-}18}$	4.0	4.25	4.5	V
Internal resistance of voltage source		R_8	–	–	5	Ω
Available output current		$-I_8$	2	–	–	mA
		$+I_8$	0.6	–	–	mA
Output short-circuit current (typ. value = V_P/1 kΩ)		$-I_{8sc}$	–	8	–	mA
Reference current source						
Reference voltage (typ. value = $V_{8\text{-}18}-V_{BE}$)		$V_{17\text{-}18}$	–	3.6	–	V
Internal biasing resistor		R_{i17}	–	5	–	kΩ
Allowable range of external reference resistor		$R_{17\text{-}18}$	180	–	270	kΩ

APPLICATION INFORMATION (Fig. 1)

parameter	symbol		application	unit
SK switch-on threshold level at m_{BK} = 60%	V_{iSKon}	typ.	1.8	mV
SK switch-on threshold level at V_{iSK} = 8 mV	m_{BKon}	typ.	32	%
SK switch hysteresis	$\frac{m_{BKon}}{m_{BKoff}}$	>	3.0	dB
		typ.	3.5	dB
		<	4.0	dB
SK switch-on delay (note 1)	t_{dSKon}	typ.	95	ms
		<	130	ms
SK switch-off delay (note 2)	t_{dSKoff}	>	380	ms
		typ.	500	ms
		<	620	ms
DK switch-on threshold level at m_{DK} = 30%	V_{iDKon}	typ.	1.5	mV
DK switch-on threshold level at V_{iDK} = 8 mV	m_{DKon}	typ.	13	%
DK switch hysteresis	$\frac{m_{DKon}}{m_{DKoff}}$	>	3.1	dB
		typ.	3.6	dB
		<	4.1	dB
DK switch-on delay (note 1)	t_{dDKon}	typ.	750	ms
		<	1000	ms
DK switch-off delay (note 2)	t_{dDKoff}	>	600	ms
		typ.	750	ms
		<	1000	ms

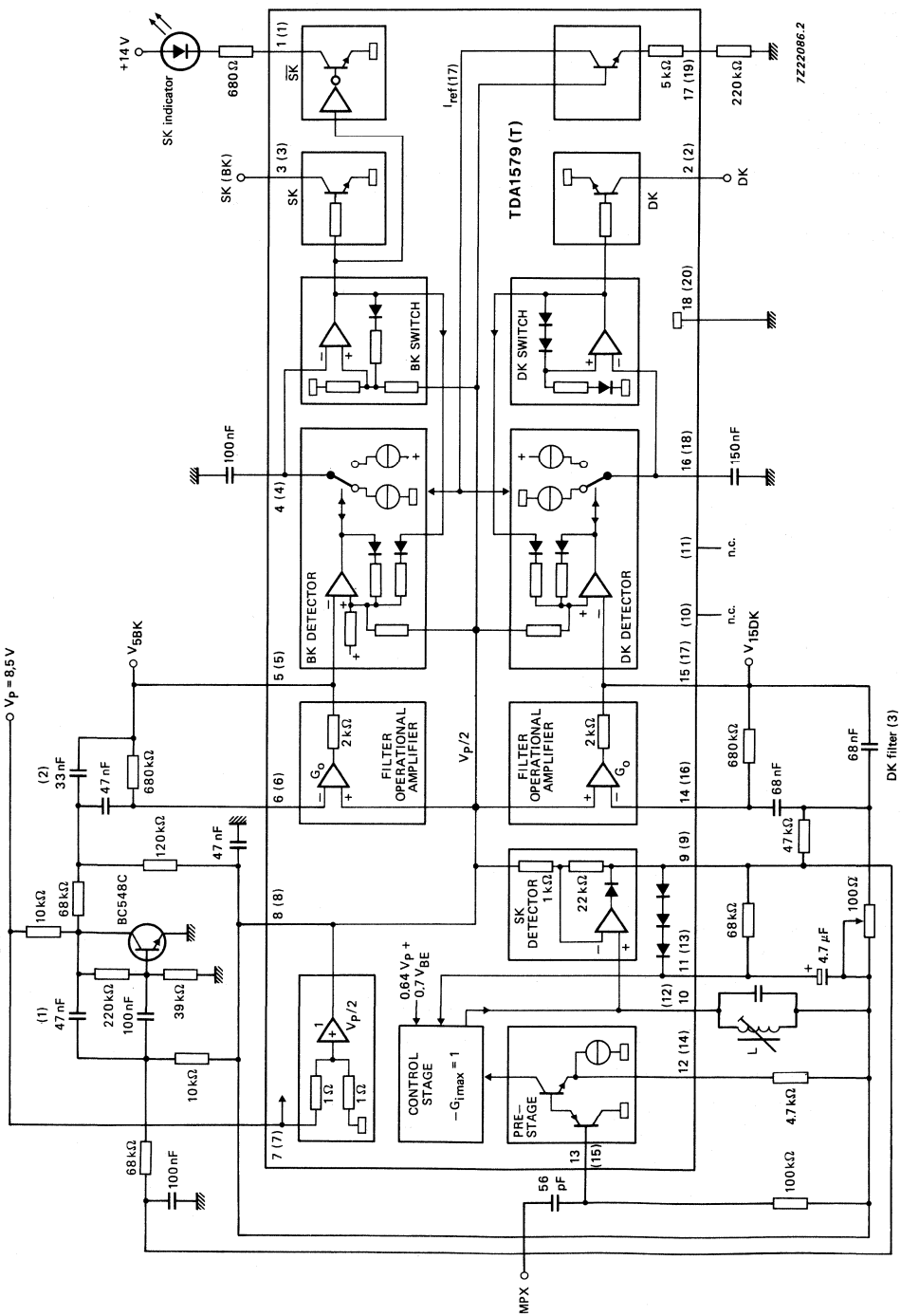
Notes

1. **Sequence for measuring switch-on delay times** (t_{don})
   a) Nominal BK or DK input signal at pin 13: $V_{i(p-p)}$ = 8 mV; f = 57 kHz; modulation-on.
   b) Pin 4 of the BK detector (pin 16 of the DK detector) is switched to ground to cause a low signal at the SK output at pin 3 (DK output at pin 2).
   c) t_{don} commences when the ground connection is removed from pin 4 (pin 16) as the positive-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{don} ends when the positive-going edge of the SK output arrives at pin 13 (DK at pin 2).
2. **Sequence for measuring switch-off delay times** (t_{doff})
   a) Nominal operating conditions as in note 1.
   b) t_{doff} commences when the input is switched off as the negative-going V_{oBK} signal at pin 5 (V_{oDK} signal at pin 15) crosses zero.

   t_{doff} ends when the negative-going edge of the SK output arrives at pin 3 (DK at pin 2).

APPLICATION INFORMATION (continued)



L = 2.36 mH; Q_L = 70; C = 3.3 nF; f_o = 57 kHz.
Pin numbers in parentheses are for TDA1579T, other pin numbers are for TDA1579.

Fig. 1 Application diagram.

(1) f_o = 55 Hz; Q = 1.9
(2) f_o = 24 Hz; Q = 1.9
(3) f_o = 125 Hz

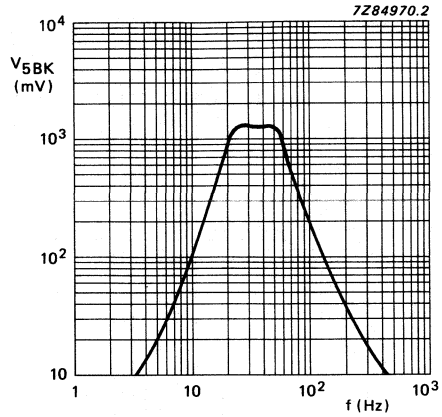


Fig. 2 BK signal voltage at pin 5 as a function of frequency.

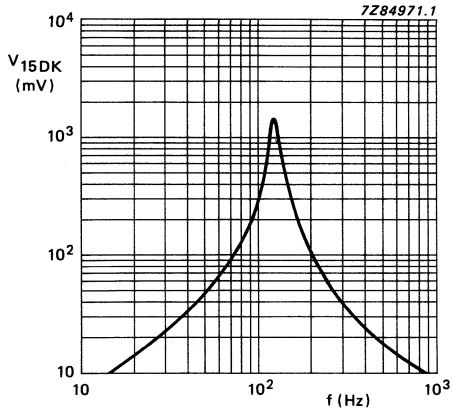


Fig. 3 DK signal voltage at pin 15 as a function of frequency: f_o = 125 Hz; Q ≈ 18.

APPLICATION INFORMATION (continued)

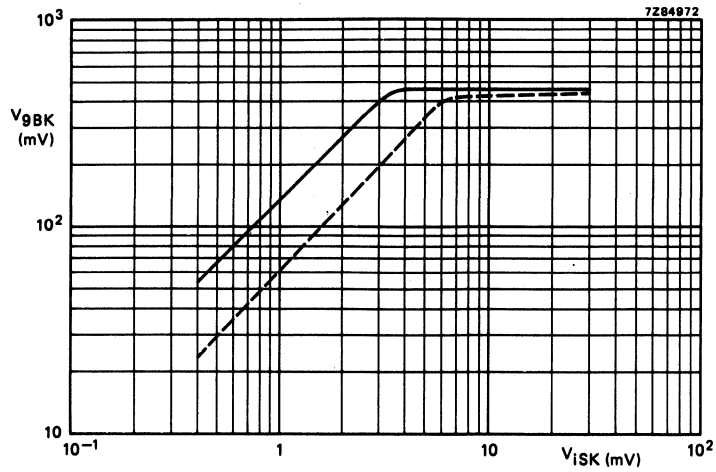


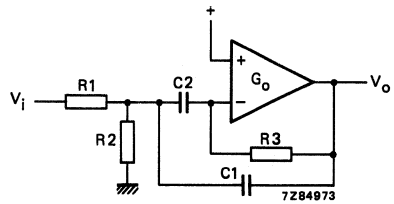
Fig. 4 Control characteristic of the SK amplifier at V_P = 8.5 V, m_{BK} = 60% and Q_L = 70.

FILTER INFORMATION

Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = - \frac{\frac{p}{R1 \cdot C1}}{p^2 + p \frac{C1 + C2}{R3 \cdot C1 \cdot C2} + \frac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}$$, in which $p = j\omega$ and $G_v = \frac{V_o}{V_i}$.



	general equation	C1 = C2 = C	C1 = C2 = C R2 << R1
Resonance frequency $\omega_r =$	$\frac{1}{\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$	$\frac{1}{C\sqrt{\frac{R1 \cdot R2}{R1 + R2} \cdot R3}}$	$\frac{1}{C\sqrt{R2 \cdot R3}}$
Gain at $\omega = \omega_r$ $-G_{vr} =$	$\frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$	$\frac{1}{2} \cdot \frac{R3}{R1}$
Quality $Q =$	$\sqrt{\frac{C1 \cdot C2}{C1 + C2}} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2}\sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$	$\frac{1}{2} \cdot \frac{R3}{R2}$

Recommended components

C1, C2 and R1, R2, R3	metallized polycarbonate film (MKC) capacitors; ± 5% metal film (MR) resistors; ± 2%
or	
C1, C2 and R1, R2, R3	metallized polyester film (MKT) capacitors; ± 5% carbon film (CR) resistors; ± 2%

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA1591(T)
PLL stereo decoder and noise blanker

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz)
- Mono/stereo switching, dependent on pilot signal
- Analog control of mono/stereo change over (stereo blend, SNC)
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis (High Cut Control input, HCC)
- Applicable as source selector for AM/FM/cassette switching
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking
- Noise blanking at MPX-demodulator outputs
- Internal voltage stabilization

GENERAL DESCRIPTION

The TDA1591(T) is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications. The device operates in a power supply range of 7.5 to 12 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)	7.5	10	12	V
I_P	supply current	-	12	-	mA
V_o	audio output signal (RMS value)	-	900	-	mV
THD	total harmonic distortion	-	0.1	0.3	%
S/N	signal-to-noise ratio	-	76	-	dB
α	channel separation	-	40	-	dB
V_{trigg}	interference voltage trigger level	-	10	-	mV

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1591	20	DIL	plastic	SOT146
TDA1591T	20	mini-pack	plastic	SOT163A

PLL stereo decoder and noise blanker

TDA1591(T)

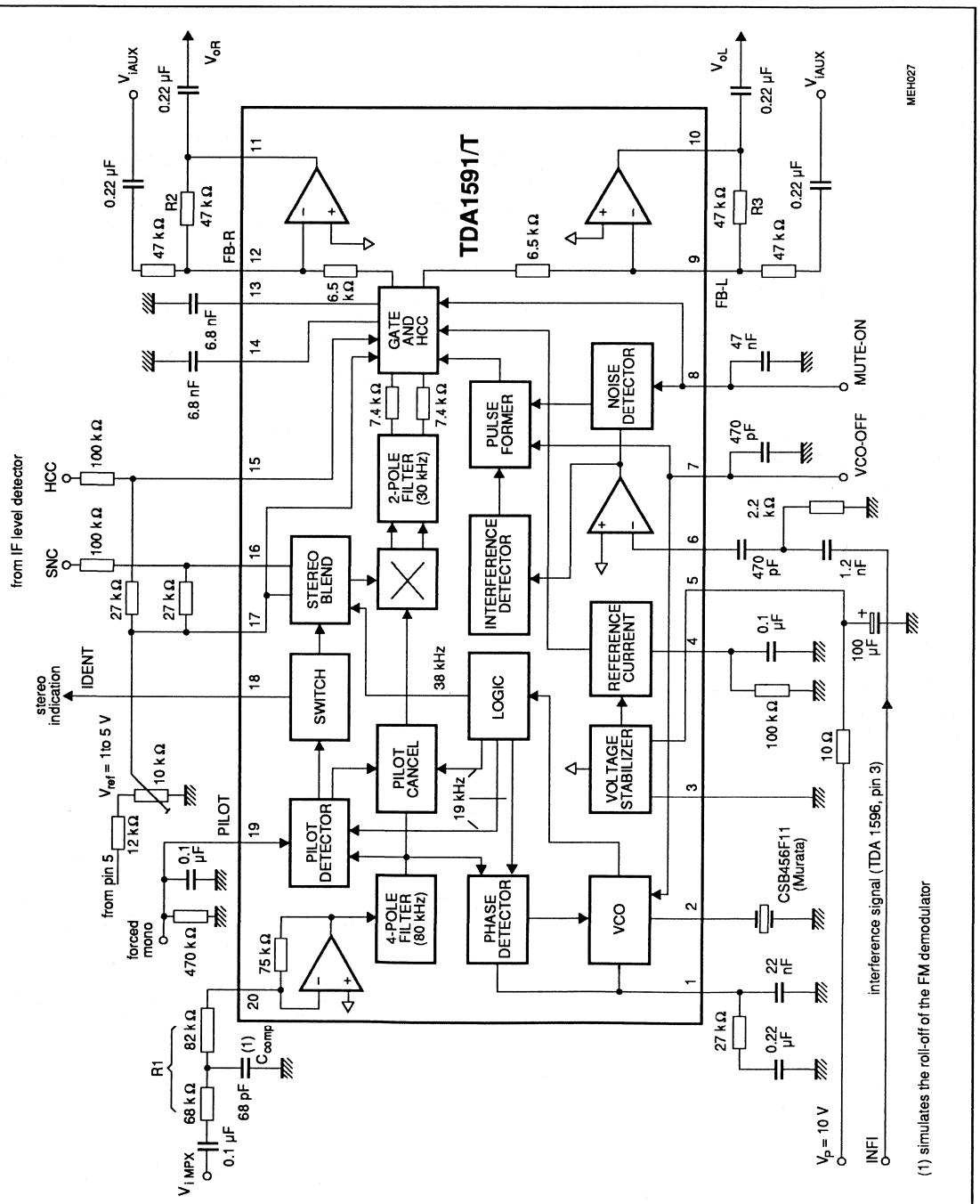


Fig.1 Block diagram, test and application circuit.

PLL stereo decoder and noise blanker

TDA1591(T)

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase-locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{ref}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant, VCO off
NDET	8	noise detector time constant, mute on
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	High Cut Control input for de-emphasis control
SNC	16	stereo blend input (Stereo Noise Controller)
V_{ref}	17	externally-applied reference voltage of 1 to 5 V
IDENT	18	identification output (High = pilot existing, stereo)
PILOT	19	pilot detector level (forced mono input)
V_{iMPX}	20	MPX input signal from IF demodulator

PIN CONFIGURATION

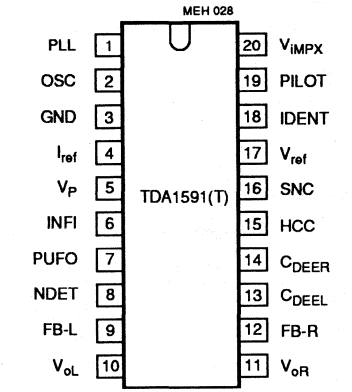


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

By changing the value of the input resistor R1 the MPX input can be adapted to the level of the FM demodulator output (Fig.3). The total gain of the stereo decoder is applicable by variation of the feedback resistors R2 and R3 (Fig.1 and 4).

In mute and VCO-OFF position the output amplifier can be used for cassette playback, AM-stereo purpose or other signal sources.

The Stereo Noise Controller SNC provides a smooth mono to stereo take over (Fig.5).

For High Cut Control (HCC), dependent on an analog input signal, the de-emphasis time constant can be changed to higher values (Fig.7 and 8).

The noise blanking facility is achieved by gating the stereo decoder output signal.

The interference detector generates a gating pulse preferable forced by the level detector voltage of the IF part.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	0	13.2	V
P_{tot}	total power dissipation	0	0.25	W
T_{stg}	storage temperatur range	–55	150	°C
T_{amb}	operating ambient temperatur range	–40	+85	°C
V_{ESD}	electrostatic handling* for all pins	-	±800	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

PLL stereo decoder and noise blanker

TDA1591(T)

CHARACTERISTICS

V_P = 10 V, T_{amb} = 25 °C, input signal $V_{i\ MPX\ (p\text{-}p)}$ = 1.7 V; m = 100 % (deviation Δf = ±75 kHz, f_{mod} = 1 kHz), de-emphasis 50 µs and serial resistor at input R1 = 150 kΩ; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 5)		7.5	10	12	V
I_P	supply current		-	12	-	mA
Stereo decoder						
V_i	MPX input signal at pin 20 (peak-to-peak value)		-	1.7	-	V
ΔV_i	overdrive margin of MPX input signal	THD = 1%	3	-	-	dB
V_o	AF mono output signal at pins 10 and 11 (RMS value)	without pilot	-	900	-	mV
ΔV_o	overdrive margin of output signal	THD = 1%	3	-	-	dB
$V_{10\text{-}11}/V_o$	difference of output voltage levels		-	-	1	dB
$V_{10,11}$	DC output voltage (pins 10 and 11)		3.3	3.8	4.3	V
$R_{10,11}$	output resistance		-	130	-	Ω
α	channel separation, see Fig.6	pin 16 open-circuit	-	40	-	dB
THD	total harmonic distortion		-	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 to 16000 Hz	-	76	-	dB
α_{19}	pilot signal suppression	f = 19 kHz	-	50	-	dB
α_{38}	subcarrier suppression	f = 38 kHz	-	50	-	dB
α_{57}		f = 57 kHz	-	46	-	dB
α_{76}		f = 76 kHz	-	60	-	dB
α_2	intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz, note 1	-	60	-	dB
α_3		f_{mod} = 13 kHz	-	58	-	dB
$\alpha_{57\ VF}$	traffic radio (VWF)	f = 57 kHz, note 2	-	70	-	dB
α_{67}	SCA (subsidiary communications authorization)	f = 67 kHz, note 3	70	-	-	dB
α_{114}	ACI (adjacent channel interference)	f = 114 kHz, note 4	-	80	-	dB
α_{190}		f = 190 kHz	-	70	-	dB
RR	ripple rejection with ripple on V_P	f = 100 Hz $V_{ripple\ (rms)}$ = 100 mV	-	35	-	dB
VCO (pin 2)						
f_{osc}	oscillator frequency (ceramic resonator)		-	456	-	kHz
f_{osc}	frequency range of free running oscillator		452	-	460	kHz
$\Delta f/f$	capture and holding range		-	1	-	%
V_7	VCO-OFF voltage (pin 7)		0	-	0.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mono/stereo control (pins 16, 17 and 19)						
$V_{i\ pil}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)					
	for stereo on		-	24	30	mV
	for stereo off		8	20	-	mV
H	hysteresis of pilot threshold voltage		-	2	-	dB
V_{19}	switching voltage for external mono control (pin 19)		0	-	1	V
V_{ref}	reference input voltage range (pin 17)		1	-	5	V
V_{16-17}	control voltage for channel separation due to pin 17 (V_{ref}), see Fig.5	α = 6 dB	-	–85	-	mV
		α = 26 dB	-	–32	-	mV
	pilot indicator logic level output					
V_{18}	LOW voltage (pin 18)	I_{18} = –1 mA	-	250	400	mV
I_{18}	HIGH current	V_{18} = 10 V	-	-	1	µA
Muting (pin 8)						
V_8	mute attenuation (pin 8)	V_8 < 0.4 V	-	80	-	dB
		V_8 > 4 V	-	-	0.2	dB
$V_{10, 11}$	DC offset voltage	after muting	-	-	±500	mV
High Cut Control HCC (pin 15)						
T_{deem}	control range of de-emphasis	(Fig.7 and 8)				
	for European standard	C_{deem} = 6.8 nF	-	50	150	µs
	for US standard	C_{deem} = 10 nF	-	75	225	µs
V_{15-17}	control voltage (pin 15 due to pin 17) in both standards	lower value T_{deem}	-	0	-	mV
		upper value T_{deem}	-	–300	-	mV
Noise interference detector						
V_{trigg}	trigger threshold (pin 6)	f_{int} = 120 kHz				
		$V_{8\ (DC)}$ = 7.7 V	-	10	-	mV
		$V_{8\ (DC)}$ = 6.7 V	-	100	-	mV
ΔV_8	voltage offset as a function of V_{trigg}	$V_{6\ trigg}$ = 10 mV	-	200	-	mV
		$V_{6\ trigg}$ = 100 mV	-	2.3	-	V
T_{suppr}	AF suppression time, pulse with		-	40	-	µs
$I_{13,14}$	input offset current (pins 13 and 14)	during AF suppression time	-	20	-	nA

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})} \quad ; \quad f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})} \quad ; \quad f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with 91% mono signal; f_{mod}= 10 kHz or 13 kHz; 9% pilot signal

2. Traffic radio (V.F.) suppression

$$\alpha_{57}\ (VF) = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

measured with 91% stereo signal; f_{mod}= 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 kHz; f_{mod}= 23 Hz AM, m = 0.6).

3. SCA (Subsidiary Communication Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})} \quad ; \quad f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with 81% mono signal; f_{mod}= 1 kHz; 9% pilot signal;
10% SCA subcarrier (f_s = 67 kHz, unmodulated).

4. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})} \quad ; \quad f_s = 110\text{ kHz} - (3 \times 38\text{ kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})} \quad ; \quad f_s = 186\text{ kHz} - (5 \times 38\text{ kHz})$$

measured with 90% mono signal; f_{mod}= 1 kHz; 9% pilot signal; 1% spurious signal
(f_s = 110 kHz or 186 kHz, unmodulated).

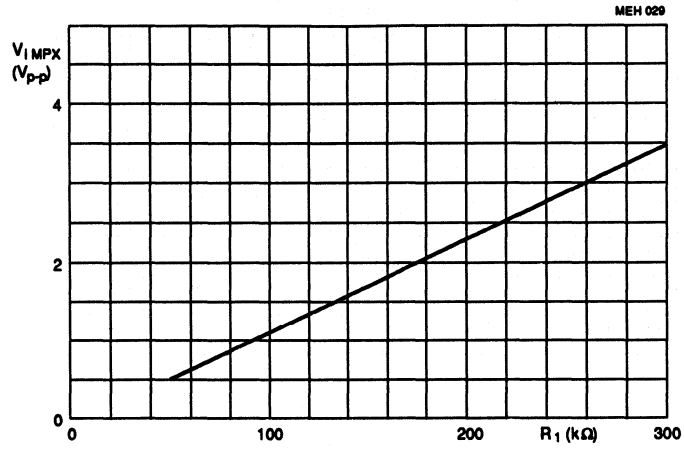


Fig.3 Input signal as a function of serial input resistor R1.

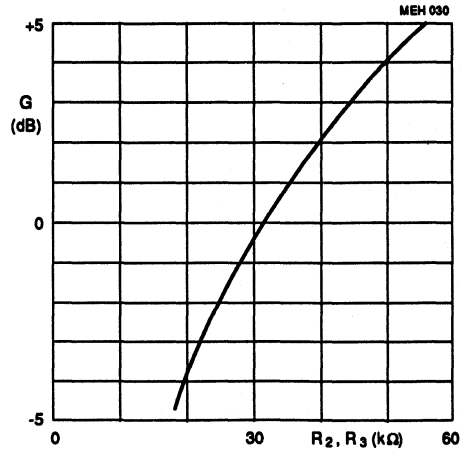


Fig.4 Over all signal gain as a function of feedback resistors R2 and R3 (R1 = 150 kΩ).

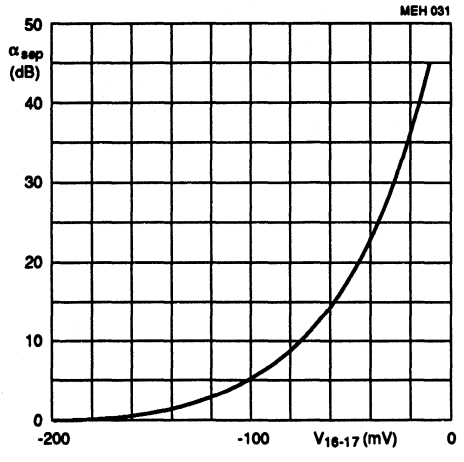


Fig.5 Stereo blend characteristic (SNC).

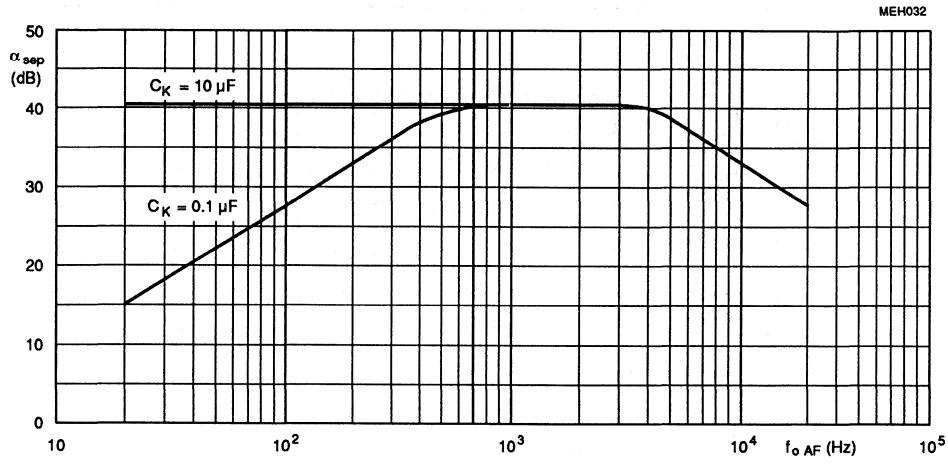


Fig.6 Channel separation as a function of audio frequency.

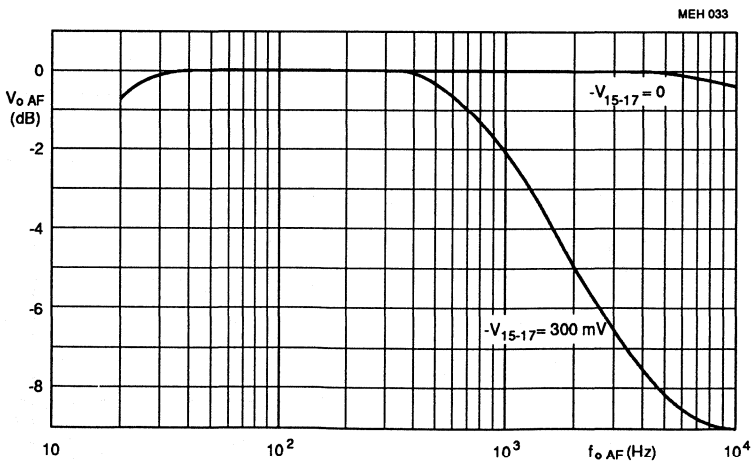


Fig.7 High Cut Control (HCC) as a function of audio frequency.

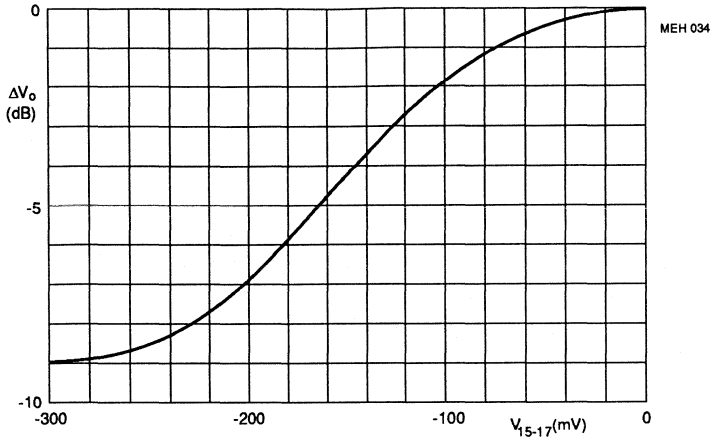


Fig.8 High Cut Control (HCC) at f_{mod} = 10 kHz.

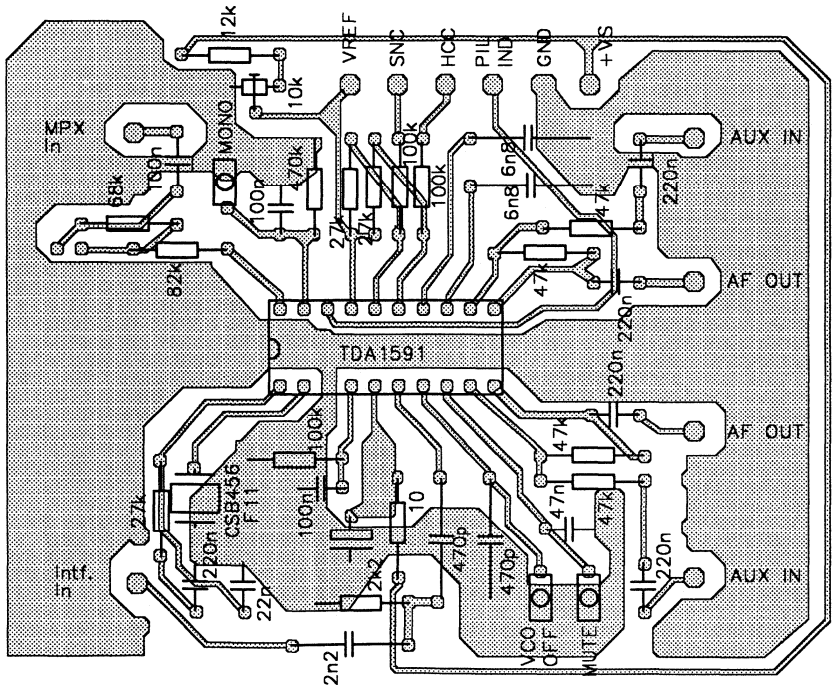


Fig.9 TDA1591(T) testboard (component side).

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

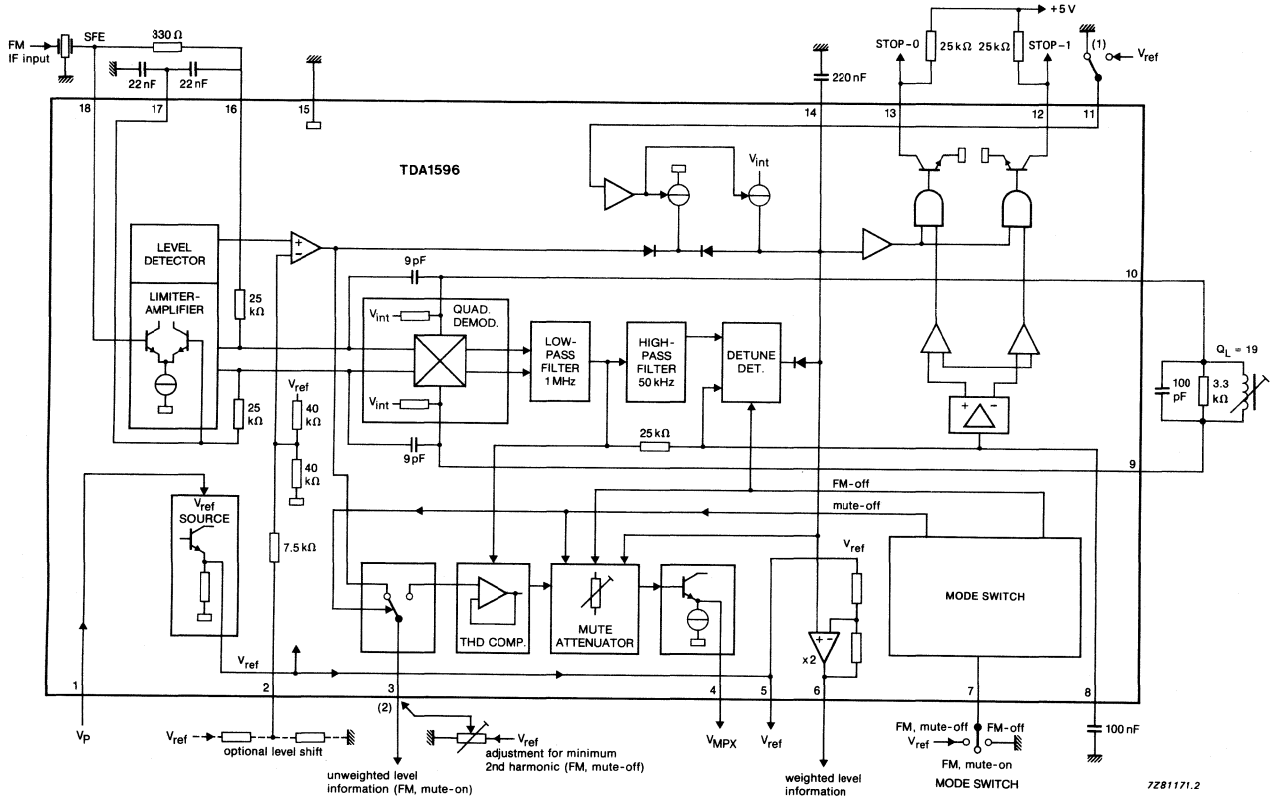
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{18(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{18(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

SEE ALSO DATA SHEET FOR TDA1596T

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.

(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

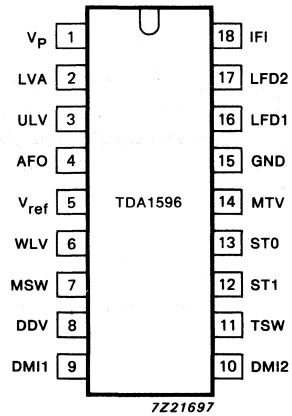


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	DMI1	demodulator input 1
10	DMI2	demodulator input 2
11	TSW	tau switch
12	ST1	stop pulse output 1
13	ST0	stop pulse output 0
14	MTV	mute voltage
15	GND	ground
16	LFD1	IF limiter feedback 1
17	LFD2	IF limiter feedback 2
18	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 9 and 10 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 14 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 14. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 13 and 12 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 12 and 13 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-15}$	−0.3	+ 16	V
Reference voltage range (pin 5)	V_{5-15}	−0.3	+ 10	V
Level adjustment range (pin 2)	V_{2-15}	−0.3	+ 10	V
Mode switch voltage range (pin 7)	V_{7-15}	−0.3	+ 16	V
Control input voltage range (pin 11)	V_{11-15}	−0.3	+ 6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-15}	−0.3	+ 16	V
Tuning-stop output voltage range				
STOP-0 (pin 13)	V_{13-15}	−0.3	+ 16	V
STOP-1 (pin 12)	V_{12-15}	−0.3	+ 16	V
Tuning-stop output current				
STOP-0 (pin 13)	I_{13}	−	2	mA
STOP-1 (pin 12)	I_{12}	−	2	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+ 2000	V
pin 5	V_{es}	−2000	+ 900	V
pin 6	V_{es}	−2000	+ 1600	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-15} = 8.5$ V; $V_I = V_{18(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 9, 10 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 15); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{9-10}	25	40	55	kΩ
	C_{9-10}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{9, 10(p-p)} \leqslant 100\ \mu V$; $V_{18(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-15}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 14)					
at $V_{18(rms)} \leqslant 5\ \mu V$	V_{14}	–	2.0	–	V
at $V_{18(rms)} = 1$ mV	V_{14}	–	3.45	–	V
Output impedance (pin 14)	R_{14-15}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-15}	15	–	–	kΩ
Internal muting (Fig. 4)					
Internal attenuation of signals ± 22.5 kHz $\leqslant$ detuning $\leqslant \pm 80$ kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{14} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{14} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{14} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 14)					
Pin 11 connected to ground *					
charge current	$+I_{14}$	–	8	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Pin 11 connected to V_{ref}					
charge current	$+I_{14}$	–	100	–	μA
discharge current	$-I_{14}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 18) (Fig. 5):					
$V_{18(rms)} \leqslant 5\ \mu V$; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{18(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range $V_{18(rms)} \geqslant 50\ \mu V$ to $V_{18(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{18}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 6) at input voltage $V_{18(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning = for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ± 200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{18(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 7)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{18(rms)} \leqslant 5\ \mu V$	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{18(rms)} \leqslant 5\ \mu V$	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 11 to ground is only allowed for measuring the current at pin 14. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 8 and 9)					
Stop-0: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{13} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{13} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{18(rms)}$ = 10 mV					
for $V_{12} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{12} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 18)					
input voltage (RMS value) for $V_{12} = V_{13} \geqslant 3.5$ V	$V_{18(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{12} = V_{13} \leqslant 0.3$ V	$V_{18(rms)}$	–	–	50	μV
Output voltage when $I_{12} = I_{13}$ = 1 mA	$V_{12, 13}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 10)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}15} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\|I_7\|$	–	–	2.5	μA
Output voltage with $R_{3\text{-}15}$ = 10 kΩ; $C_{3\text{-}15} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{18} = \leqslant 5$ μV; I_3 = 500 μA	$R_{3\text{-}15}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	$0.9\,V_5$	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}15}$	1	–	–	MΩ
Reference voltage source					
Output voltage at I_5 = −1 mA	V_5	3.3	3.7	4.1	V
Output impedance at I_5 = −1 mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_{18(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{18(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 11)	$V_{18(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 12) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 13)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{18(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{18} = 300 μV to 100 mV (Fig. 14)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

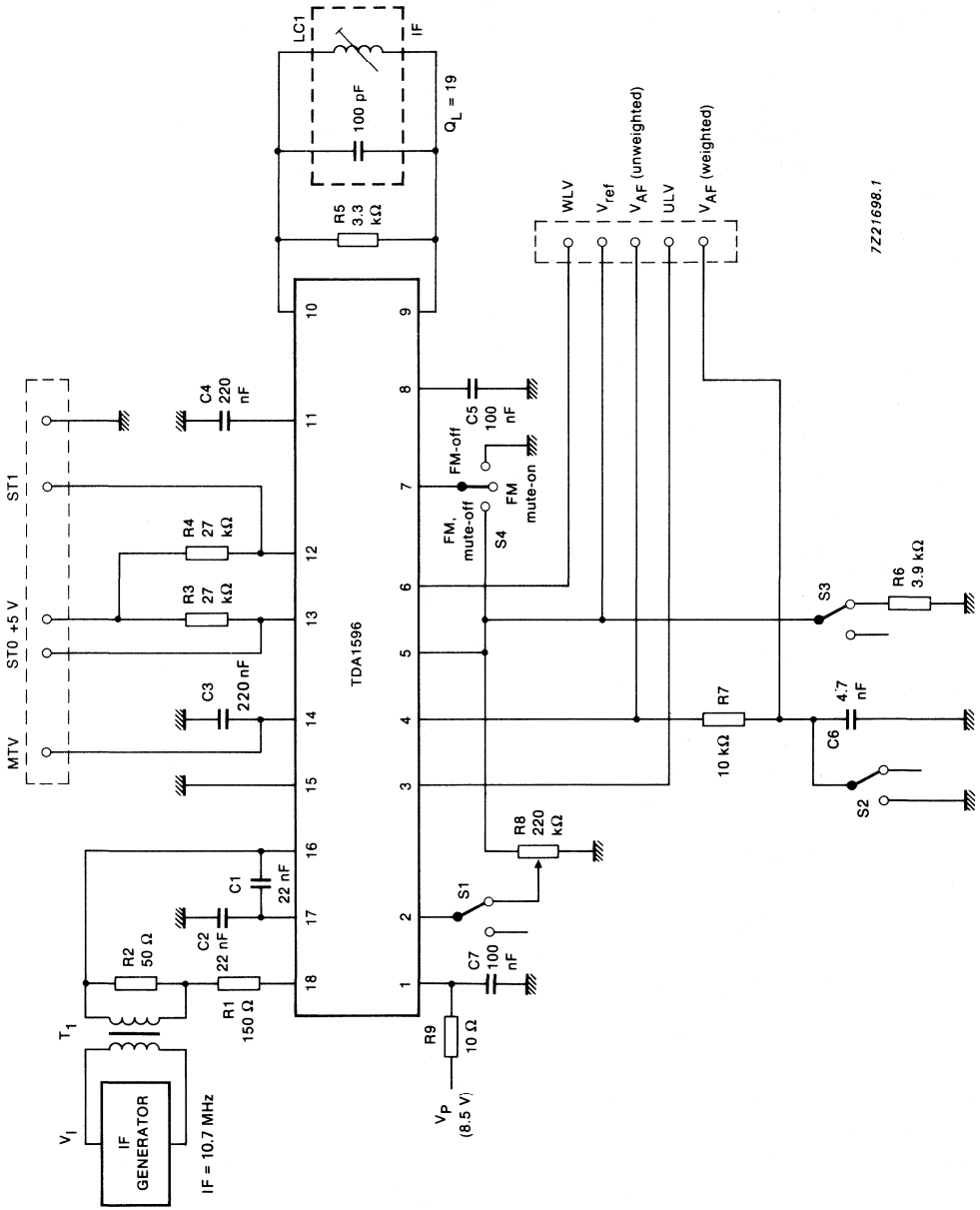


Fig. 3 Test circuit.

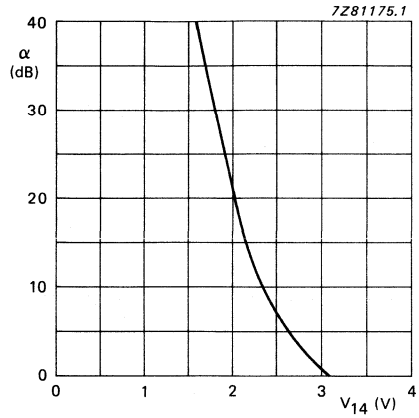


Fig. 4 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 14) and mute attenuation, $I_2 = I_7 = 0$ mA.

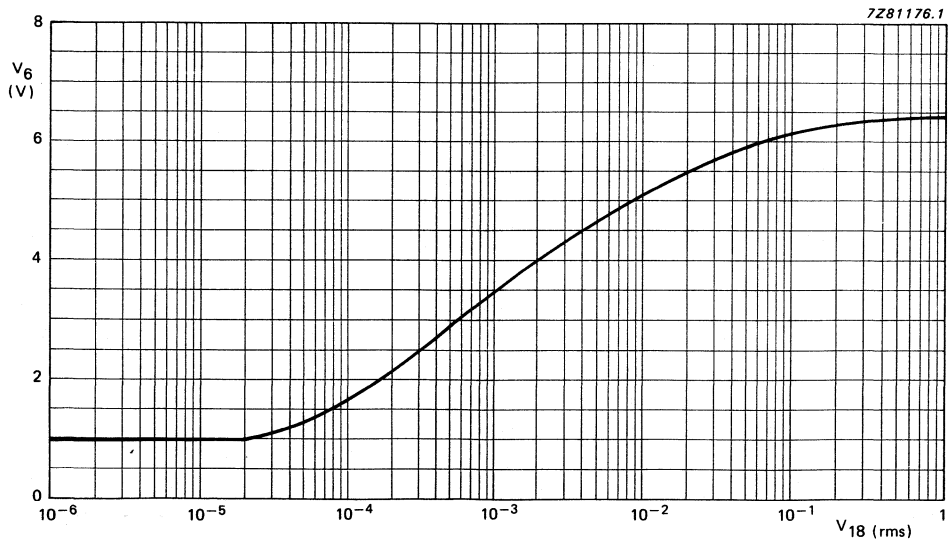


Fig. 5 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 18); $R_{6\text{-}15} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

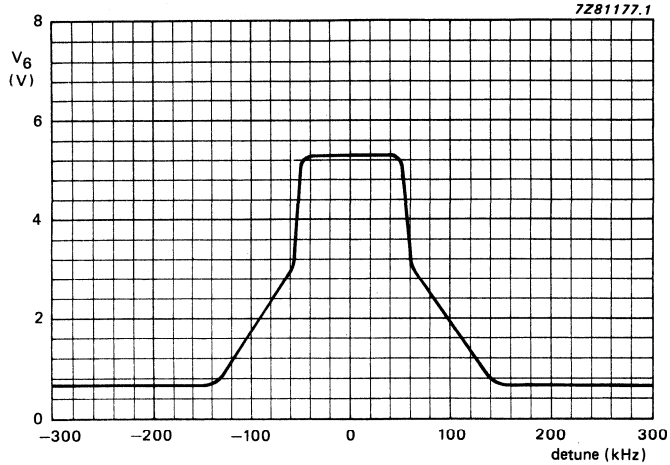


Fig. 6 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{18} = 10\ mV$.

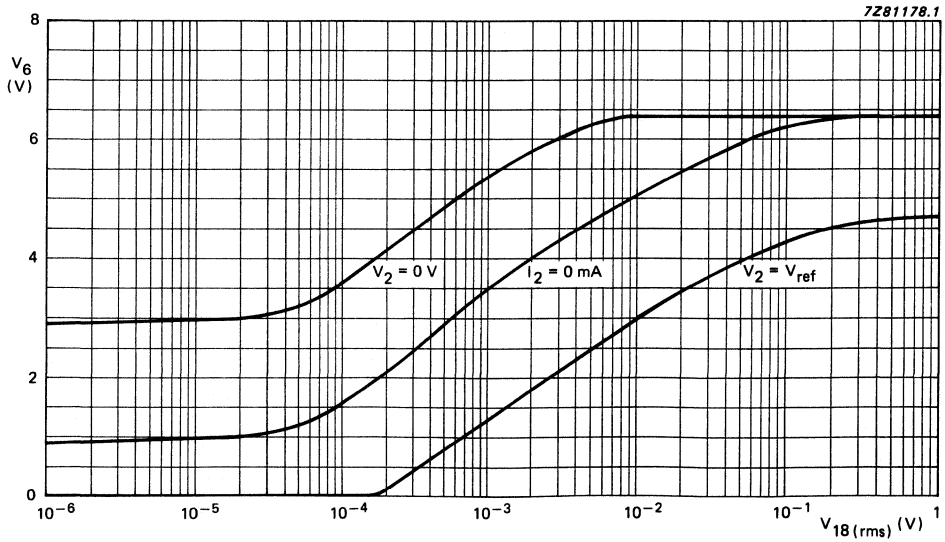
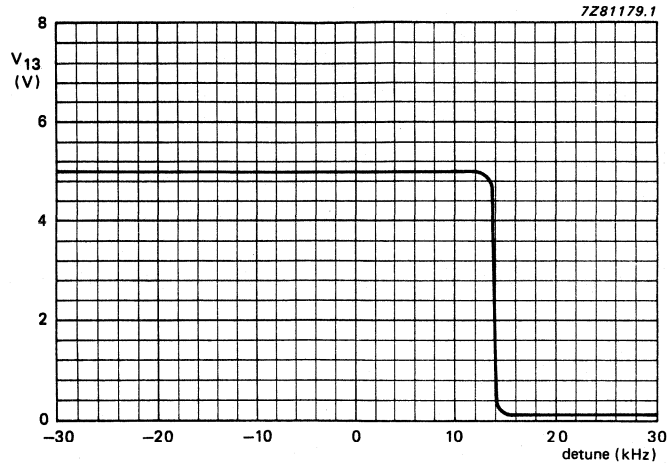
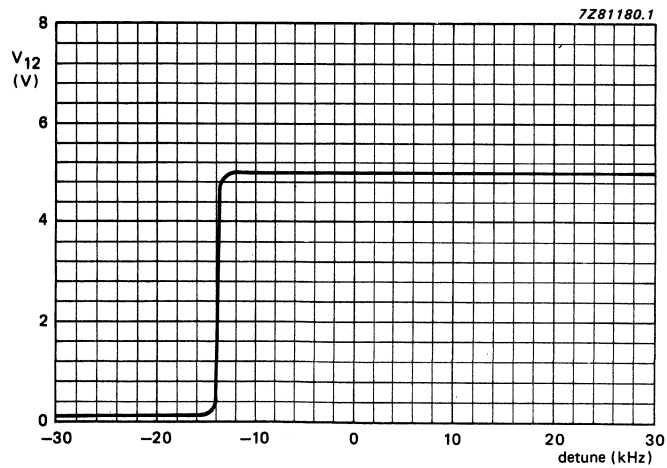


Fig. 7 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}15} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1

Fig. 8 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{18} = 10 mV.

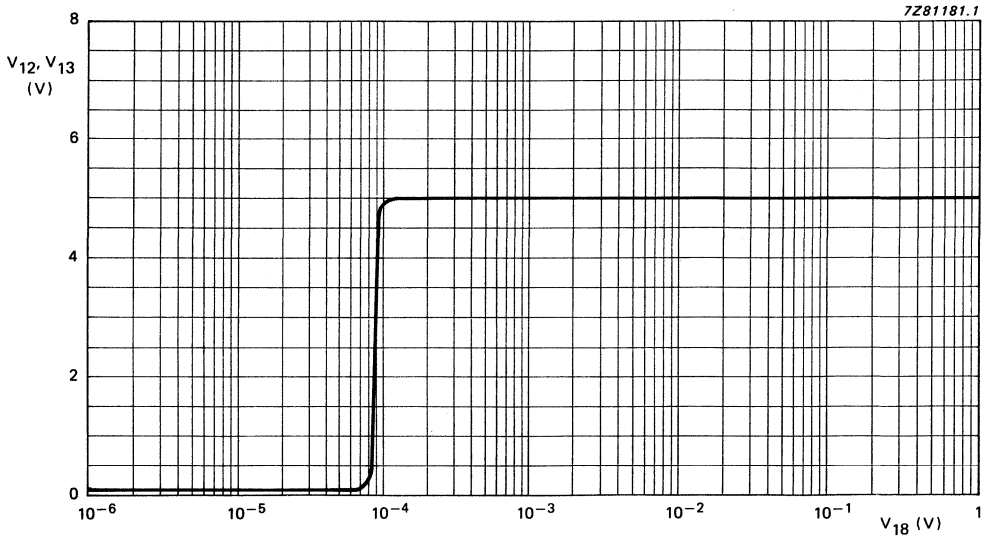


Fig. 9 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 18.

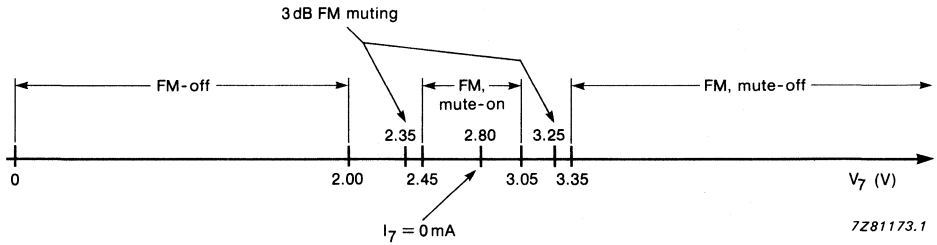
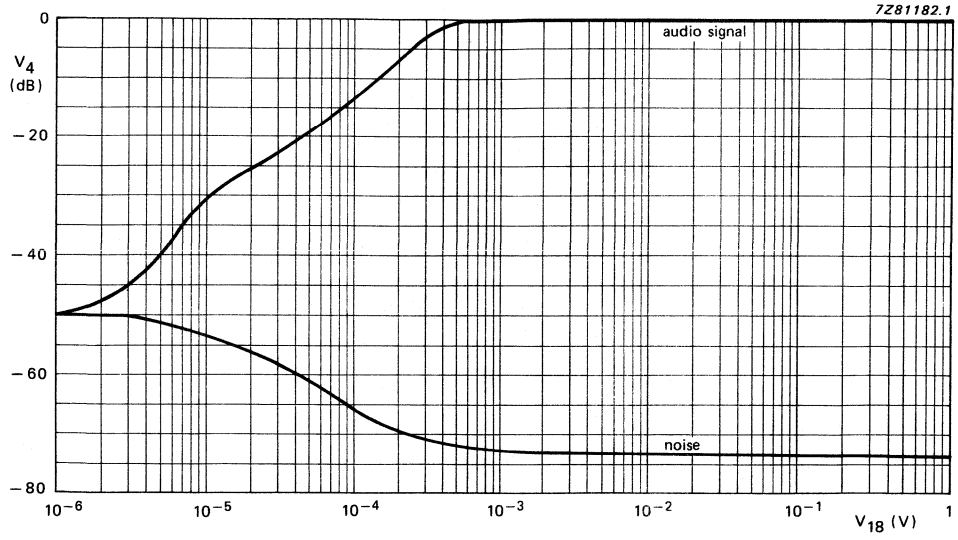
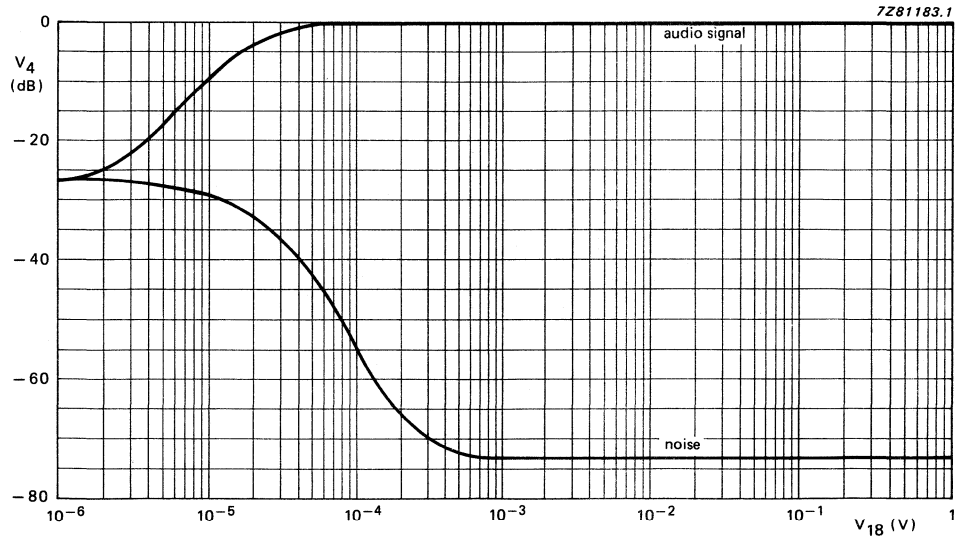


Fig. 10 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 11 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 18; measured with 50 μs de-emphasis.

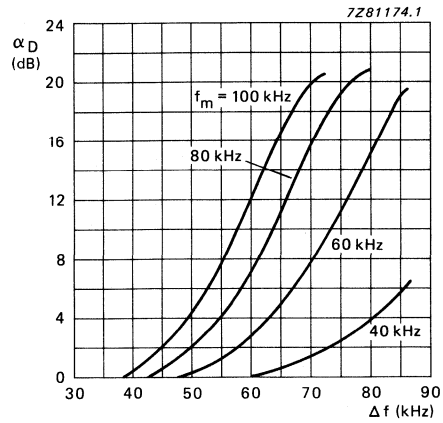


Fig. 12 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

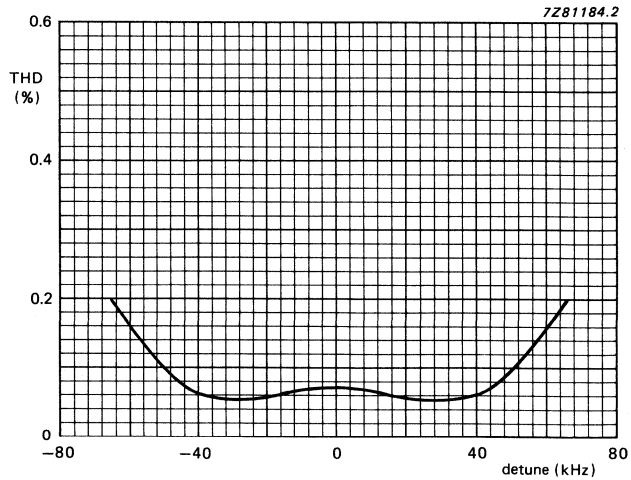
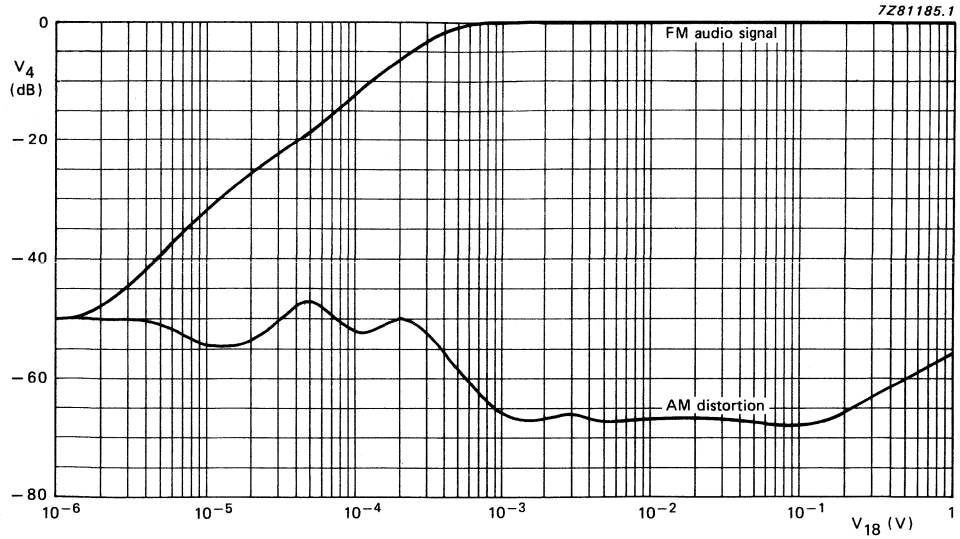
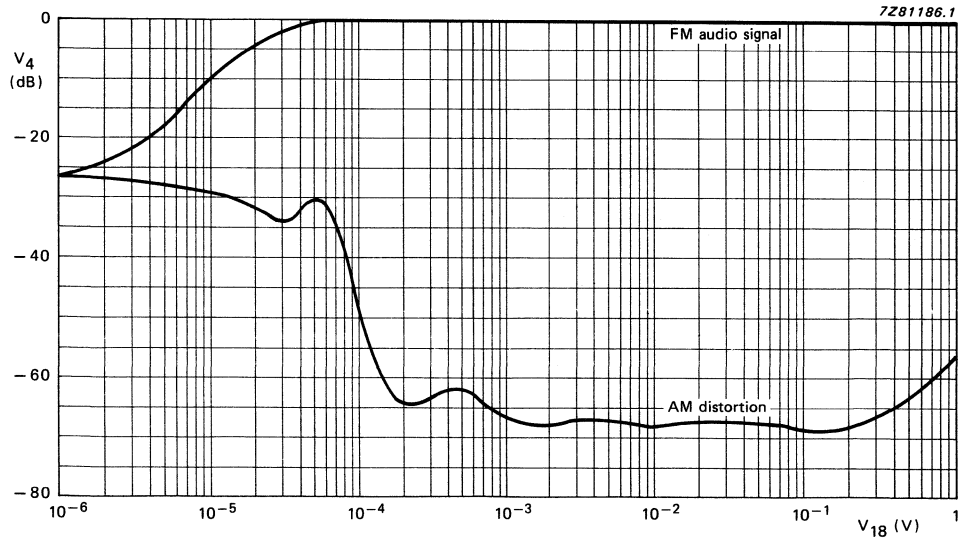


Fig. 13 THD as a function of detuning; mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{18(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 14 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

IF AMPLIFIER/DEMODULATOR FOR FM RADIO RECEIVERS

GENERAL DESCRIPTION

The TDA1596T provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receiver circuits.

Features

- Simulates behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend and field strength indication control voltage
- Three-state mode switch for FM, mute-on / FM, mute-off / FM-off
- Internal compensation of AF signal total harmonic distortion (THD)
- Two open collector stop pulse outputs for microcomputer tuning control (can be one stop pulse output by wired-ANDing)
- Internal reference voltage source
- Built-in hum and ripple rejection circuits

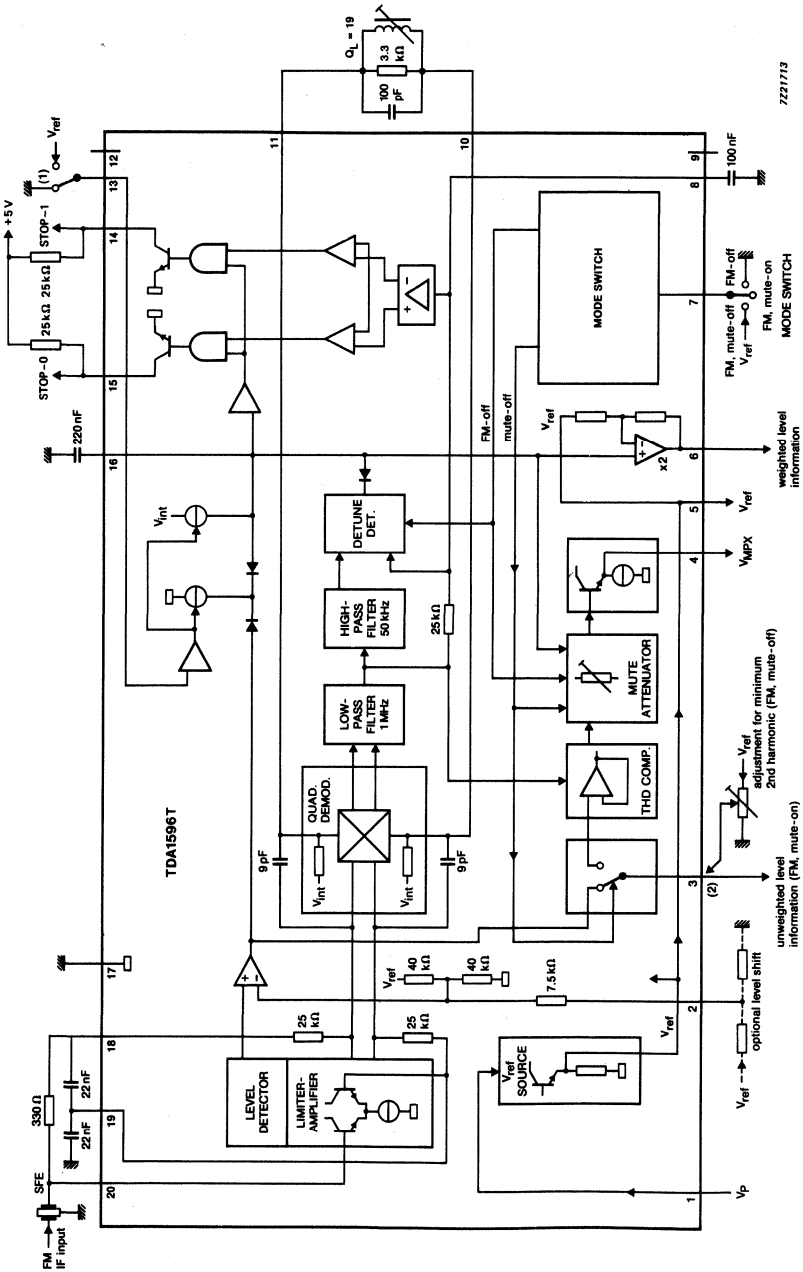
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)		V_P	7.5	8.5	12.0	V
Supply current (pin 1)	V_P = 8.5 V; $I_2 = I_7$ = 0 mA	I_P	–	20	26	mA
AF output voltage (RMS value)	$V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Signal-to-noise ratio	$V_{20(rms)}$ = 10 mV; f_m = 400 Hz; Δf = 75 kHz	S/N	–	82	–	dB
Total harmonic distortion	$V_{20(rms)}$ = 10 mV; f_m = 1 kHz; I_7 = 0 mA; Δf = 75 kHz; FM mute on; without de-emphasis; without detuning	THD	–	0.1	0.3	%
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C

SEE ALSO DATA SHEET FOR TDA1596

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).



(1) Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.
(2) In the FM, mute-on condition the unweighted level detector output is available from pin 3. In the FM, mute-off condition the variable resistor at pin 3 can be adjusted for minimum 2nd harmonic distortion at pin 4.

Fig. 1 Block diagram and application circuit.

PINNING

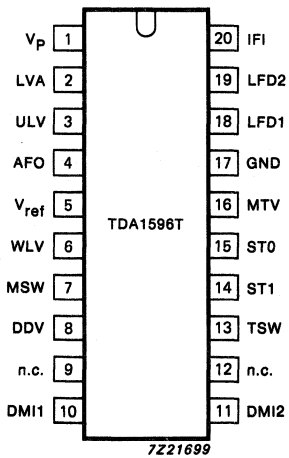


Fig. 2 Pinning diagram.

1	V_P	supply voltage
2	LVA	level voltage adjustment
3	ULV	unweighted level output/K2 adjustment
4	AF0	AF output
5	V_{ref}	reference voltage output
6	WLV	weighted level voltage output
7	MSW	mode switch
8	DDV	detune detector voltage
9	n.c.	not connected
10	DMI1	demodulator input 1
11	DMI2	demodulator input 2
12	n.c.	not connected
13	TSW	tau switch
14	ST1	stop pulse output 1
15	ST0	stop pulse output 0
16	MTV	mute voltage
17	GND	ground
18	LFD1	IF limiter feedback 1
19	LFD2	IF limiter feedback 2
20	IFI	IF input

FUNCTIONAL DESCRIPTION

Limiter-amplifier

This has five stages of IF amplification using balanced differential limiter-amplifiers with emitter-follower coupling. Decoupling of the stages from the voltage supply lines and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

FM demodulator

The demodulator is fully balanced and comprises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter-amplifier output, and the other via an external 90° phase-shifting network. The demodulator has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

THD compensation

This circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator circuit between pins 10 and 11 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum THD, instead the adjustment criterium is for a symmetrical stop pulse.

Mute attenuator and AF output

The control voltage for the mute attenuator at pin 16 is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor at pin 16. The AF signal is passed via the mute attenuator to the output at pin 4.

A weighted control voltage, available from pin 6, is obtained from the mute attenuator control voltage via a buffer-amplifier which introduces an additional voltage shift and gain.

Level detector

The level detector generates a voltage output which is proportional to the field strength of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM, mute-on condition.

Tuning-stop outputs

The open collector outputs STOP-0 and STOP-1 (from pins 15 and 14 respectively) are voltages derived from the detuning level and the field strength of the input signal. If only one tuning-stop output is required, pins 14 and 15 may be tied together.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-17}$	−0.3	+16	V
Reference voltage range (pin 5)	V_{5-17}	−0.3	+10	V
Level adjustment range (pin 2)	V_{2-17}	−0.3	+10	V
Mode switch voltage range (pin 7)	V_{7-17}	−0.3	V_P	V
Control input voltage range (pin 13)	V_{13-17}	−	+6	V
THD compensation/unweighted field strength voltage range (pin 3)	V_{3-17}	−0.3	V_P	V
Tuning-stop output voltage range				
STOP-0 (pin 15)	V_{15-17}	−0.3	V_P	V
STOP-1 (pin 14)	V_{14-17}	−0.3	V_P	V
Tuning-stop output current				
STOP-0 (pin 15)	I_{15}	−	2	mA
STOP-1 (pin 14)	I_{14}	−	2	mA
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−40	+85	°C
Electrostatic handling*				
all pins except pins 5 and 6	V_{es}	−2000	+2000	V
pin 5	V_{es}	−2000	+900	V
pin 6	V_{es}	−2000	+1600	V

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a\ (max.)} = 95$ K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

f = 10.7 MHz; $V_P = V_{1-17} = 8.5$ V; $V_I = V_{20(rms)} = 1$ mV; $T_{amb} = 25$ °C; measured in the circuit of Fig. 3; tuned circuit at pins 10, 11 aligned for symmetrical stop pulses; all voltages are referred to ground (pin 17), unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_1$	7.5	8.5	12.0	V
Supply current at $I_2 = I_7 = 0$ mA	I_1	–	20	26	mA
FM demodulator					
Input impedance	R_{10-11}	25	40	55	kΩ
	C_{10-11}	–	6	–	pF
DC output voltage (no-signal condition) at $V_{10,\ 11(p-p)} \leqslant 100\ \mu V$; $V_{20(rms)} \leqslant 5\ \mu V$	V_4	2.75	3.10	3.45	V
Output impedance	R_{4-17}	–	400	–	Ω
Mute attenuator control voltage					
Control voltage (pin 16)					
at $V_{20(rms)} \leqslant 5\ \mu V$	V_{16}	–	2.0	–	V
at $V_{20(rms)} = 1$ mV	V_{16}	–	3.45	–	V
Output impedance (pin 16)	R_{10-17}	–	–	2.0	MΩ
Level shift input (pin 2)					
internal bias voltage at $I_2 = 0$ mA	V_2	–	1.4	–	V
input impedance	R_{2-17}	15	–	–	kΩ
Internal muting (Fig. 6)					
Internal attenuation of signals ± 22.5 kHz ⩽ detuning ⩽ ± 80 kHz $A = 20\log[\Delta V_4(\text{FM mute-off})/\Delta V_4(\text{FM})]$					
at $V_{16} \geqslant 1\ V_5$	A	–	0	–	dB
at $V_{16} = 0.77\ V_5$	A	1.5	3.0	4.5	dB
at $V_{16} = 0.55\ V_5$	A	–	20	–	dB

parameter	symbol	min.	typ.	max.	unit
Attack and decay (pin 16)					
Pin 13 connected to ground *					
charge current	$+I_{16}$	–	8	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Pin 13 connected to V_{ref}					
charge current	$+I_{16}$	–	100	–	μA
discharge current	$-I_{16}$	–	120	–	μA
Level detector					
Dependence of output voltage on temperature	$\frac{\Delta V_6}{V_6 \Delta T}$	–	3.3	–	mV/VK
Output impedance	R_6	–	–	500	Ω
Dependence of output voltage (pin 6) on input voltage (pin 20) (Fig. 7):					
$V_{20(rms)} \leqslant 5$ μV; $I_2 = I_7 = 0$ mA	V_6	0.1	0.7	1.3	V
$V_{20(rms)} = 1$ mV; $I_2 = I_7 = 0$ mA	V_6	3.0	3.6	4.2	V
Slope of output voltage (pin 6) for input voltage range					
$V_{20(rms)} \geqslant 50$ μV to $V_{20(rms)} \leqslant 50$ mV	$\frac{\Delta V_6}{20 \Delta \log V_{20}}$	1.4	1.7	2.0	V/20 dB
Dependence of output voltage (pin 6) on detuning (Fig. 8) at input voltage $V_{20(rms)} = 10$ mV:					
detuning $\leqslant \pm 45$ kHz	ΔV_6	–	–	0.2	V
detuning for $V_6 = 1.8$ V	$\pm \Delta f$	90	–	160	kHz
detuning = ±200 kHz	V_6	0.5	0.7	0.9	V
Slope of output voltage with detuning = 125 ± 20 kHz at $V_{20(rms)} = 10$ mV	$\lvert \Delta V_6 / \Delta f \rvert$	–	35	–	mV/kHz
Level shift control (pin 2) (Fig. 9)					
adjustment range	$\pm \Delta V_6$	1.6	2.0	–	V
adjustment gain	$-(\Delta V_6 / \Delta V_2)$	–	1.7	–	V
output voltage at $V_2 = V_5$; $V_{20(rms)} \leqslant 5$ μV	V_6	–	–	0.3	V
Low-pass filter at pin 8					
Output voltage at $I_7 = 0$ mA; $V_{20(rms)} \leqslant 5$ μV	V_8	–	2.2	–	V
Internal resistance	$R_{8(int)}$	12	25	50	kΩ

* Connecting pin 13 to ground is only allowed for measuring the current at pin 16. It is not for use in application.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning-stop detector (Figs 10 and 11)					
Stop-0: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{15} \geqslant 3.5$ V	$+\Delta f$	–	–	10	kHz
for $V_{15} \leqslant 0.3$ V	$+\Delta f$	18	–	–	kHz
Stop-1: detuning at $V_{20(rms)}$ = 10 mV					
for $V_{14} \geqslant 3.5$ V	$-\Delta f$	–	–	10	kHz
for $V_{14} \leqslant 0.3$ V	$-\Delta f$	18	–	–	kHz
Dependence of STOP-0, STOP-1 on input voltage (pin 20)					
input voltage (RMS value) for $V_{14} = V_{15} \geqslant 3.5$ V	$V_{20(rms)}$	250	–	–	μV
input voltage (RMS value) for $V_{14} = V_{15} \leqslant 0.3$ V	$V_{20(rms)}$	–	–	50	μV
Output voltage when $I_{14} = I_{15}$ = 1 mA	$V_{14, 15}$	–	–	0.3	V
Mode switch and pin 3 (Fig. 12)					
FM-off position					
Control voltage for 60 dB muting depth	V_7	–	–	1.4	V
FM, mute-on position (pin 3 = output)					
Internal bias voltage at $R_{7\text{-}17} \geqslant 10$ MΩ	V_7	–	2.8	–	V
Input current	$\|I_7\|$	–	–	2.5	μA
Output voltage with $R_{3\text{-}17}$ = 10 kΩ; $C_{3\text{-}17} \geqslant 1$ nF*	V_3	–	2	–	V
Output impedance for $V_{20} = \leqslant 5$ μV; I_3 = 500 μA	$R_{3\text{-}17}$	–	–	100	Ω
FM, mute-off position (pin 3 = input)					
Control voltage	V_7	$0.9\,V_5$	–	–	V
Input current at $V_7 = V_5$	I_7	–	–	15	μA
Input resistance	$R_{3\text{-}17}$	1	–	–	MΩ
Reference voltage source					
Output voltage at I_5 = −1 mA	V_5	3.3	3.7	4.1	V
Output impedance at I_5 = −1 mA	$\Delta V_5/\Delta I_5$	–	40	80	Ω
Temperature coefficient	TC	–	3.3	–	mV/K

* Without input voltage.

OPERATING CHARACTERISTICS

f = 10.7 MHz; $V_I = V_{20(rms)}$ = 1 mV; deviation (Δf) = 22.5 kHz; modulation frequency (f_m) = 400 Hz; de-emphasis (pin 4) = 50 μs; test circuit as per Fig. 3; tuned circuit (Q_L = 19) aligned for symmetrical stop pulses; T_{amb} = + 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
AF output voltage (RMS value) at $V_{20(rms)}$ = 10 mV	$V_{4(rms)}$	180	200	220	mV
Start of limiting (FM, mute-off); (RMS value) (Fig. 13)	$V_{20(rms)}$	14	22	35	μV
Dependence of signal-to-noise ratio (in noise frequency band 250 Hz to 15 kHz, unweighted) on input voltage					
for S/N = 26 dB	$V_{18(rms)}$	–	15	–	μV
for S/N = 46 dB	$V_{18(rms)}$	–	60	–	μV
at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz	S/N	–	82	–	dB
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; without detuning; without de-emphasis; I_7 = 0 mA	THD	–	0.1	0.3	%
Dynamic mute attenuation (Fig. 14) $\alpha_D = 20\log \frac{V_4 \text{ (FM mute-off)}}{V_4 \text{ (FM, mute-on)}}$ with f_m = 100 kHz; Δf = 75 kHz	α_D	–	16	–	dB
Slope of attenuation curve	$\alpha_D \Delta f$	–	0.8	–	dB/kHz
THD (FM, mute-on) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; detuning $\leqslant \pm$ 25 kHz without de-emphasis; I_7 = 0 mA (Fig. 15)	THD	–	–	0.6	%
THD (FM, mute-off and compensated via pin 3) at $V_{20(rms)}$ = 10 mV; Δf = 75 kHz; f_m = 1 kHz; $V_7 = V_5$	THD	–	0.07	0.25	%
Voltage range at pin 3 for THD compensation	V_3	0	–	V_5	V
AM suppression (FM, mute-off) with amplitude modulation at 30%; input voltage range V_{20} = 300 μV to 100 mV (Fig. 16)		–	65	–	dB
Power supply ripple rejection = 20log [$\Delta V_1/\Delta V_4$]		33	36	–	dB
Mute attenuation (FM-off) = 20log [$V_{4(FM\text{-}on}/V_{4(FM\text{-}off)}$]		60	–	–	dB

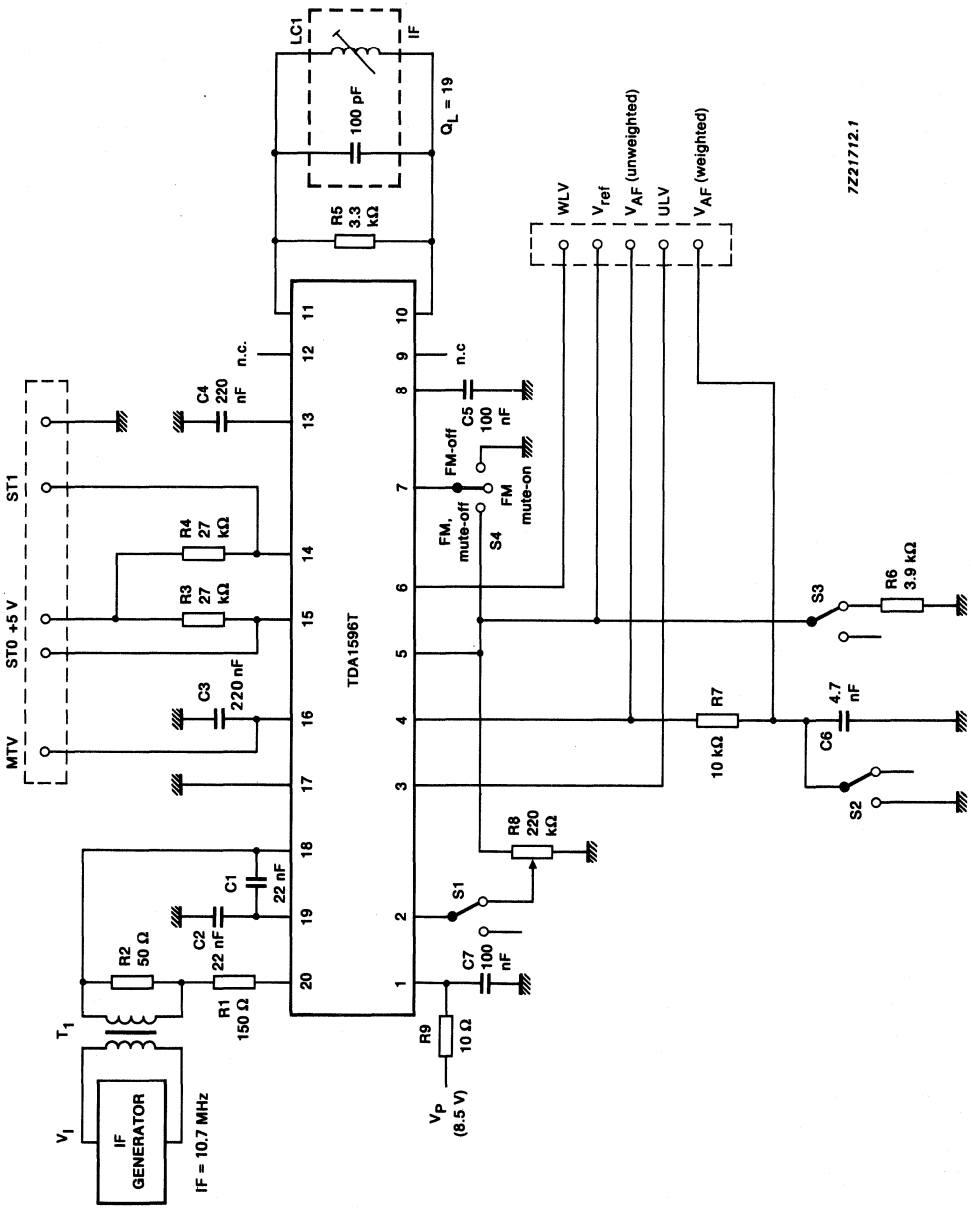


Fig. 3 Test circuit.

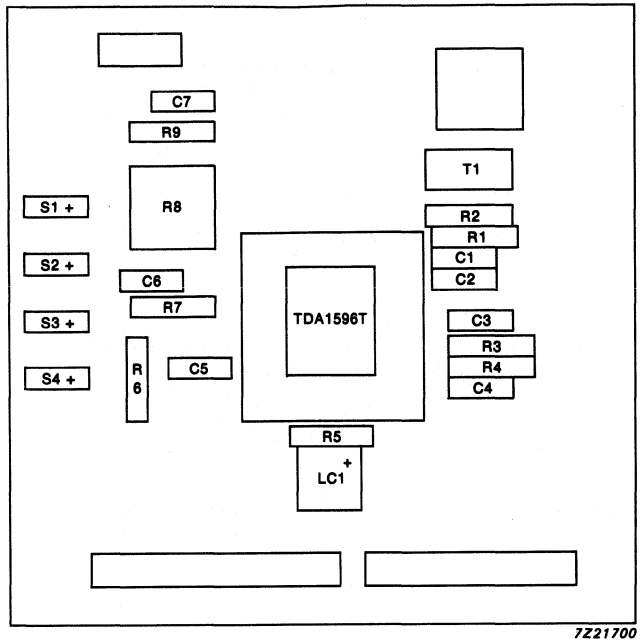


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

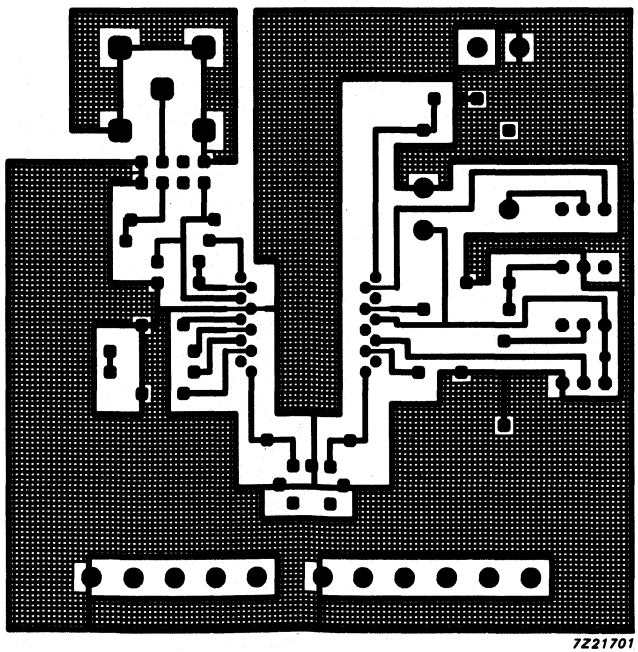


Fig. 5 Printed-circuit board showing track side.

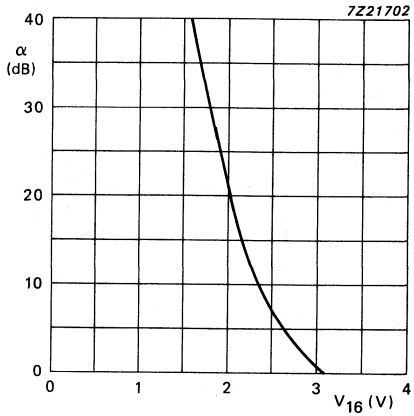


Fig. 6 Typical curve of internal attenuation showing the relationship between the mute attenuator control voltage (pin 16) and mute attenuation; $I2 = I7 = 0$ mA.

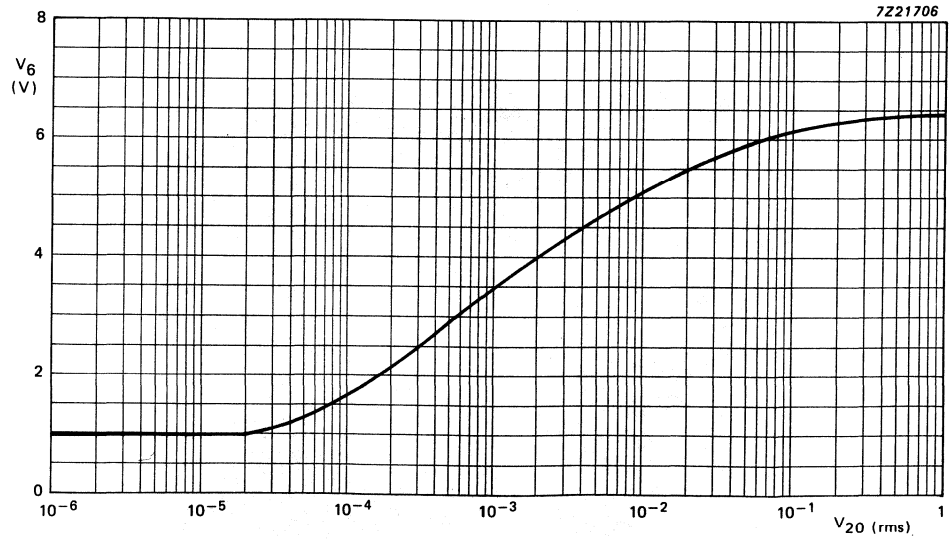


Fig. 7 Weighted field strength output voltage (pin 6) as a function of input voltage (pin 20); $R_{6\text{-}17} \geqslant 10$ kΩ; $I_2 = I_7 = 0$ mA.

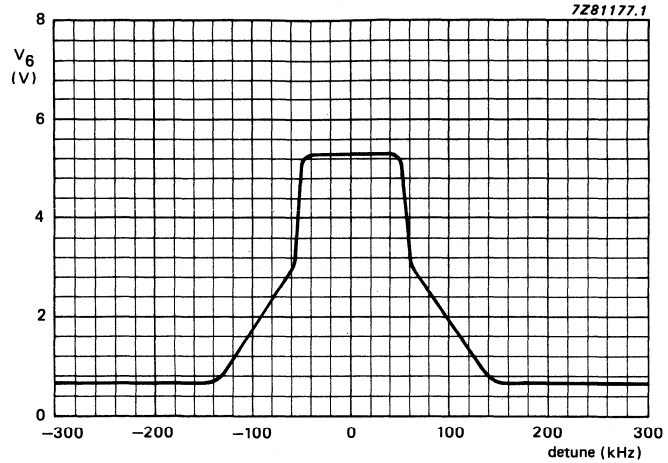


Fig. 8 Weighted field strength output voltage (pin 6) as a function of detuning; $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_2 = I_7 = 0\ mA$; $V_{20} = 10\ mV$.

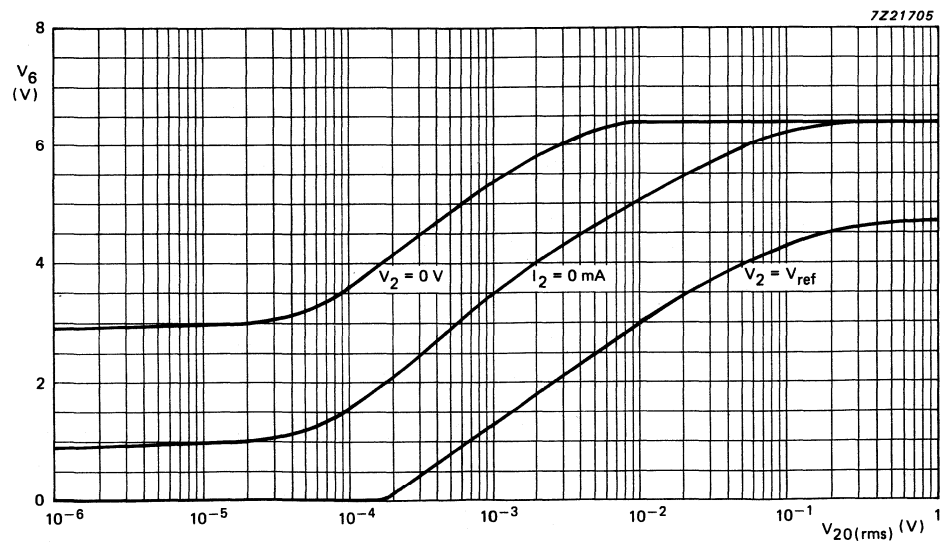
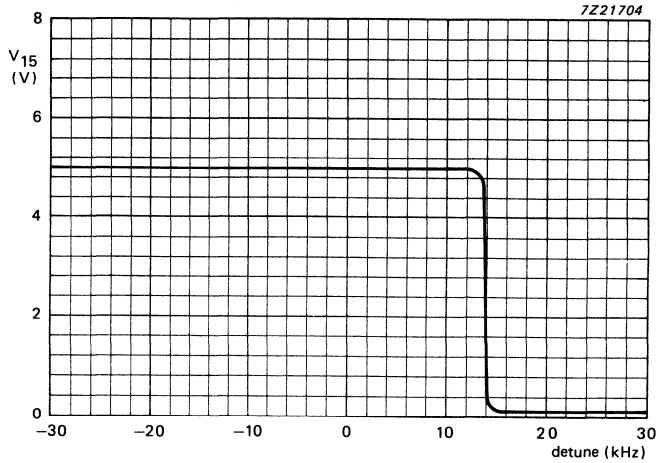
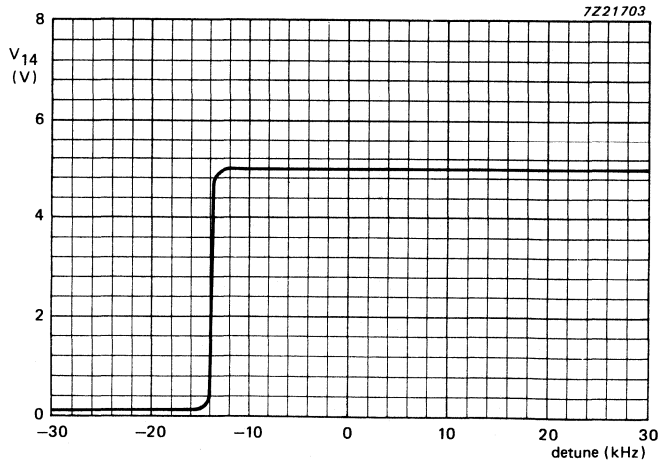


Fig. 9 Adjustment range of weighted field strength output voltage (pin 6) with level shift control (pin 2); $R_{6\text{-}17} \geqslant 10\ k\Omega$; $I_7 = 0\ mA$.



(a) STOP-0.



(b) STOP-1.

Fig. 10 STOP-0 and STOP-1 output voltages as a function of detuning, measured at V_{20} = 10 mV.

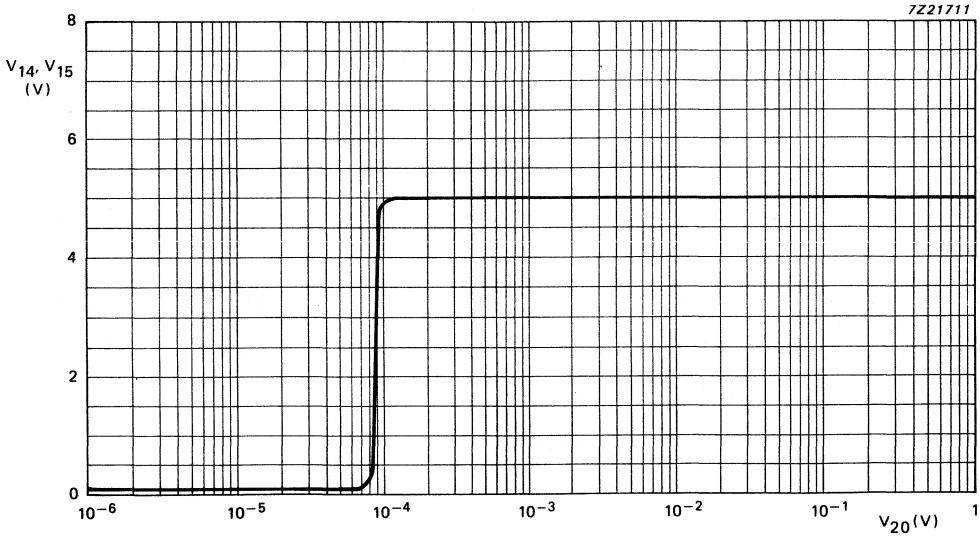


Fig. 11 STOP-0 or STOP-1 output voltages as a function of input voltage at pin 20.

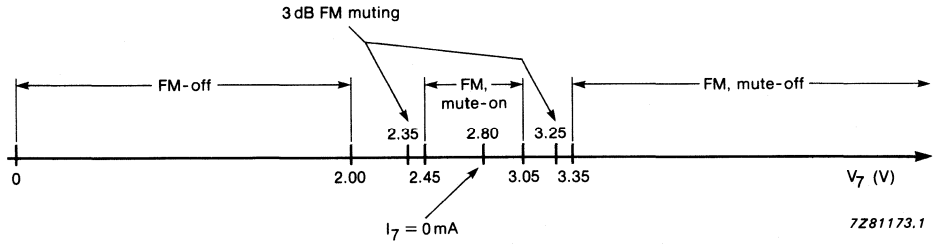
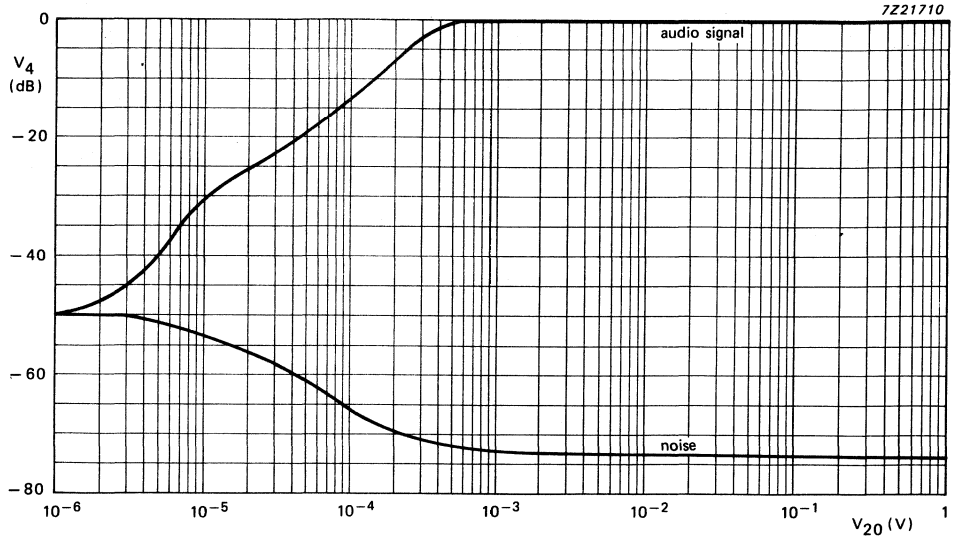
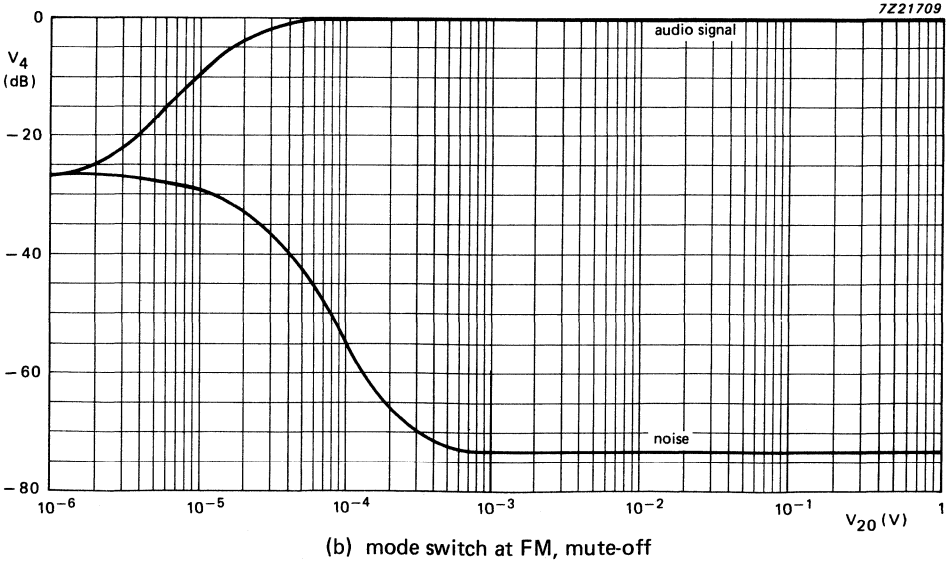


Fig. 12 Switch levels at pin 7.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 13 Audio signal (Δf = 22.5 kHz; f_m = 1 kHz) and noise as functions of input voltage at pin 20; measured with 50 μs de-emphasis.

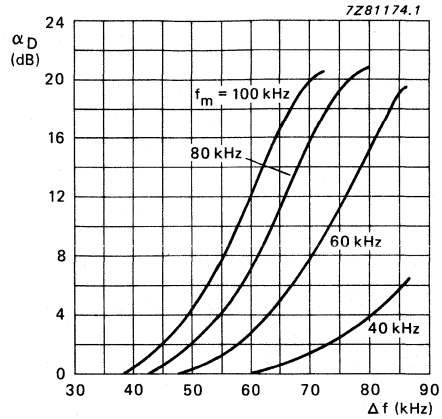


Fig. 14 Dynamic mute attenuation as a function of frequency deviation for modulation frequencies of 40, 60, 80 and 100 kHz.

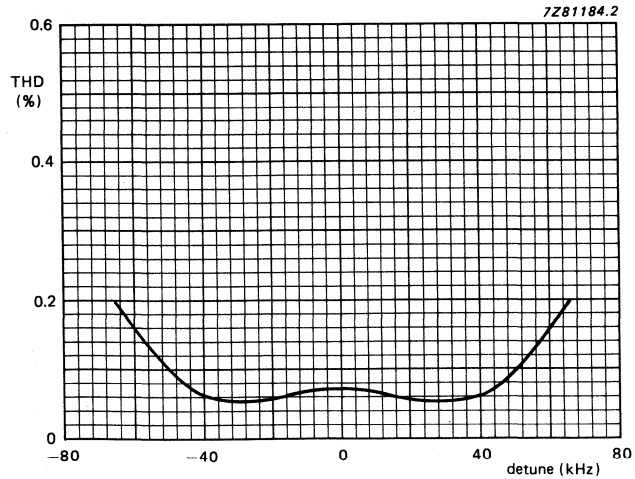
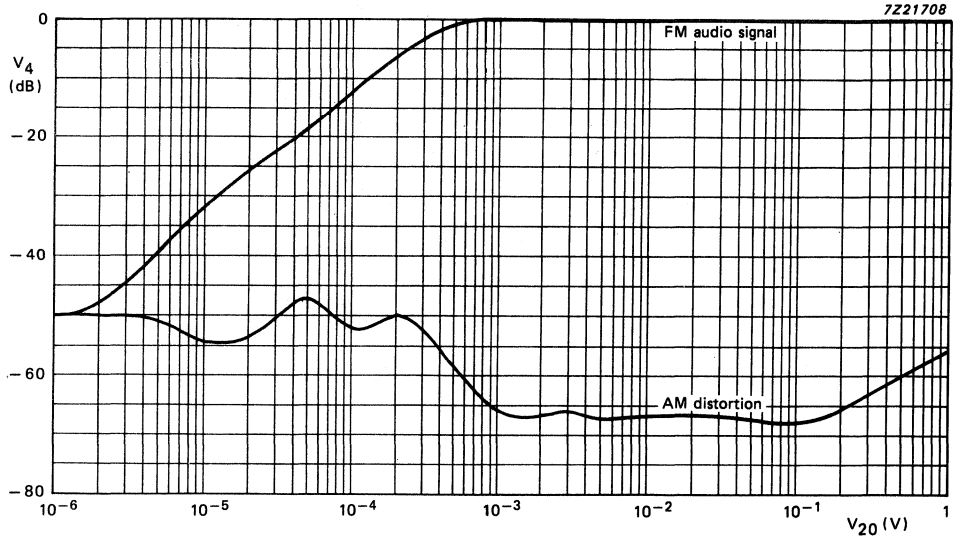
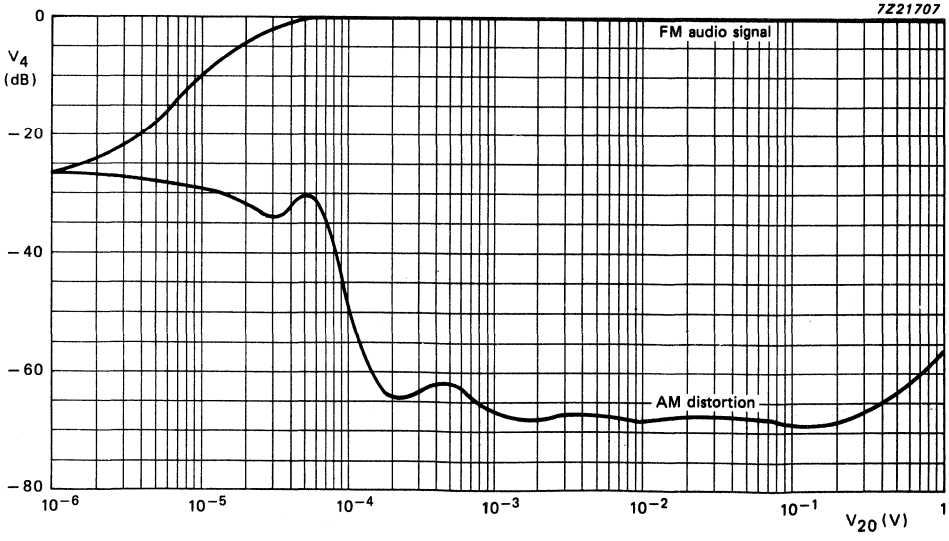


Fig. 15 THD as a function of detuning, mode switch at FM, mute-on position; Δf = 75 kHz; f_m = 1 kHz; $V_{20(rms)}$ = 10 mV.



(a) mode switch at FM, mute-on



(b) mode switch at FM, mute-off

Fig. 16 Typical curves showing AM suppression for an input signal having frequency modulation at Δf = 22.5 kHz and f_m = 1 kHz, and amplitude modulation of 30% at a frequency of 400 Hz; de-emphasis time = 50 μs and bandwidth = 250 Hz to 15 kHz.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991

TDA1599
IF amplifier/demodulator for FM radio receivers

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits

QUICK REFERENCE DATA (note 1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	-	20	26	mA
V_i	IF input sensivity for limiting on pin20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; Δf = ±75 kHz)	-	82	-	dB
THD	total harmonic distortion (f_m = 1 kHz; Δf = ±75 kHz)	-	0.1	0.3	%
	with K2-adjustment and FM-MUTE-OFF	-	0.07	0.25	%
T_{amb}	operating ambient temperature range	−40	-	+85	°C

Note 1 to quick reference data
All pin numbers in the whole data sheet referred to the SO-version TDA1599T unless otherwise specified.

GENERAL DESCRIPTION

The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receivers circuits.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599T	20	mini-pack	plastic	SOT163A
TDA1599	18	DIL	plastic	SOT102

IF amplifier/demodulator for FM radio receivers

TDA1599

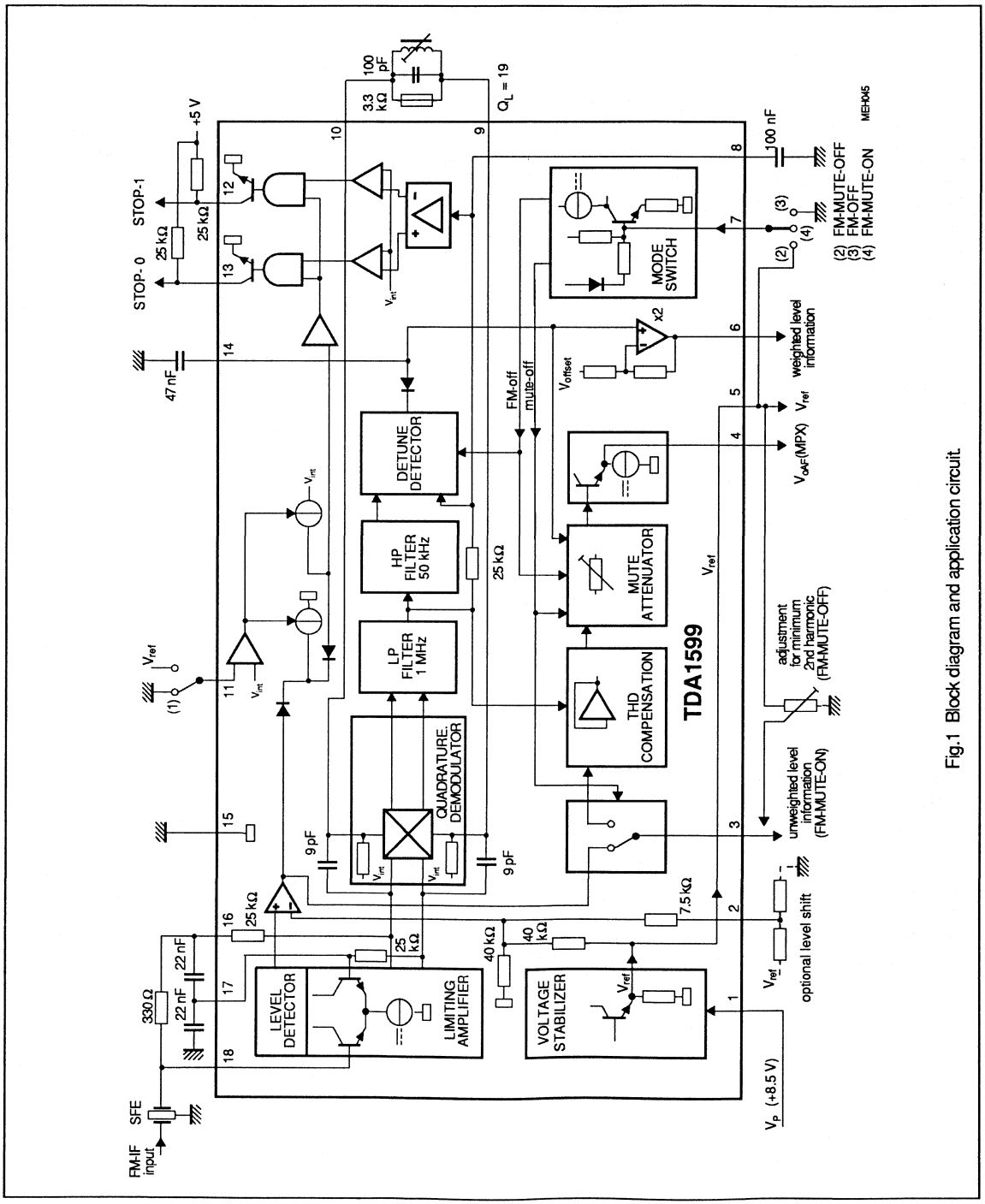


Fig.1 Block diagram and application circuit.

IF amplifier/demodulator for FM radio receivers

TDA1599

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage (+8.5 V)
LVA	2	level adjustment for stop condition
ULV	3	unweighted level output / K2 adjustment
V_{oAF}	4	audio frequency output (MPX signal)
V_{ref}	5	reference voltage output
WLV	6	weighted level output
MODE	7	mode switch input
DDV	8	detune detector voltage
DEMI1	9	demodulator input 1
DEMI2	10	demodulator input 2
TSW	11	tau switch input
ST1	12	STOP-1, stop pulse output 1
ST0	13	STOP-0, stop pulse output 0
MUTE	14	muting voltage
GND	15	ground (0 V)
LFB1	16	IF limiter feedback 1
LFB2	17	IF limiter feedback 2
V_{iIF}	18	IF signal input

PIN CONFIGURATION

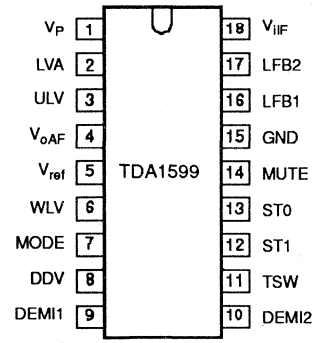


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling. Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter amplifier output, and the other via an external 90 degrees shase shifting network. The demodulater has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

The THD compensation circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator resonant circuit between pins 9 and 10 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum distortion, instead the adjustment criterium is for a symmetrical stop pulse.

The control voltage for the mute attenuator (pin 14) is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor on pin 14. The AF signal is passed via the mute attenuator to the output (pin4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier which introduces an additional voltage shift and gain.

The level detector generates a voltage output which is proportional to the amplitude of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM-MUTE-ON condition.

The open collector tuning stop outputs STOP-0 and STOP-1 (from pins 13 and 12 respectively) are voltages derived from detuning and level of the input signal. If only one tuning-stop output is required, pins 12 and 13 may be tied together.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.3	16	V
$V_{2, 5}$	voltage at pins 2 and 5	–0.3	10	V
V_n	voltage at pins 3, 7, 12 and 13	–0.3	V_P	V
V_{11}	voltage on pin 11	-	6	V
$I_{12, 13}$	current at pins 12 and 13	-	2	mA
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
V_{ESD}	electrostatic handling*			
	all pins except 5 and 6	-	±2000	V
	pin 5	-	+900	V
			–2000	V
	pin 6	-	+1500	V
			–2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	80	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

IF amplifier/demodulator for FM radio receivers

TDA1599

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; $V_{i\,(rms)}$= 10 mV on pin 18; de-emphasis of 50 µs; tuned circuit at pins 9 and 10 aligned for symmetrical stop pulses; measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	-	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		-	0	-	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{ref}$	-	-	V
	input voltage for FM-OFF	AF attenuation >60 dB	-	-	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 9 and 10		25	40	55	kΩ
C_i	demodulator input capacitance between pins 9 and 10		-	6	-	pF
AF output (pin 4)						
R_o	output resistance		-	400	-	Ω
V_4	DC output level	$V_{iIF\,(rms)} \leq 5$ µV on pin 18	2.75	3.1	3.45	V
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 13, see Fig.10				
	for $V_{13} \geq 3.5$ V		-	-	+14.0	kHz
	for $V_{13} \leq 0.3$ V		+22.0	-	-	kHz
Δf	detuning frequency for STOP 1	on pin 12, see Fig.9				
	for $V_{12} \geq 3.5$ V		-	-	−14.0	kHz
	for $V_{12} \leq 0.3$ V		−22.0	-	-	kHz
V_{18}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.8				
		$V_{12,\,13} \geq 3.5$ V	250	-	-	µV
		$V_{12,\,13} \leq 0.3$ V	-	-	50	µV
$V_{12,\,13}$	output voltage	$I_{12,\,13}$ = 1 mA	-	-	0.3	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	I_5 = −1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = −1 mA	-	40	80	Ω
TC	temperature coefficient		-	3.3	-	mV/VK

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External muting						
V_{14}	muting voltage at $I_2 = 0$, see Fig.11	$V_{18\ (rms)} \leq 5\ \mu V$	1.45	1.75	2.05	V
		$V_{18\ (rms)} = 1\ mV$	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 $\mu V \leq V_{18} \leq 100$ mV)					
	20 $\Delta \log V_{18}$ = 20 dB($\Delta V_{14} / \Delta \log V_{18}$)		-	0.85	-	V/dec
Internal mute, $\alpha = 20 \log (\Delta V_{4\ (FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\ (FM\text{-}MUTE\text{-}ON)})$						
α	mute voltage	$V_{14} \geq V_{ref}$	-	0	-	dB
		$V_{14} = 0.77\ V_{ref}$	1.5	-	4.5	dB
		$V_{14} = 0.55\ V_{ref}$	-	20	-	dB
I_{14}	current for capacitor on pin 14					
	charge current	$V_{11} = 0$ V	-	–8	-	µA
	discharge current	$V_{11} = 0$ V	-	+120	-	µA
	charge current	$V_{11} = V_{ref}$	-	–100	-	µA
	discharge current	$V_{11} = V_{ref}$	-	+120	-	µA
Level detector						
R_6	output resistance		-	-	500	Ω
V_6	output voltage at $I_2 = 0$, see Fig.13	$V_{18\ (rms)} \leq 5\ \mu V$	0.1	-	1.1	V
		$V_{18\ (rms)} = 1$ mV	3.5	-	4.7	V
	output voltage at detuning	±200 kHz detuning	1.2	1.5	1.8	V
ΔV_6	output voltage at detuning	±45 kHz detuning	-	-	0.2	V
TC	temperature coefficient		-	3.3	-	mV/VK
Δf	detuning frequency, see Fig.12	$V_6 = 1.8$ V	90	-	160	kHz
S	steepness of control voltage (slope: 50 $\mu V \leq V_{18} \leq 50$ mV)					
	20 $\Delta \log V_{18}$ = 20 dB ($\Delta V_6 / \Delta \log V_{18}$)		1.4	1.7	2.0	V/dec
$\Delta V_6 / \Delta f$	slope of output voltage at detuning	Δf = 125 ±20 kHz	-	35	-	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm \Delta V_6 / V_{ref}$	0.42	0.5	-	V/V
	gain	$-\Delta V_6 / \Delta V_2$	-	1.7	-	V/V
	range by pin 2	$\pm \Delta V_{14} / V_{ref}$	0.21	0.25	-	V/V
	gain	$-\Delta V_{14} / \Delta V_2$	-	0.85	-	V/V
Power supply ripple rejection		f = 1 kHz				
RR_{1000}	20 log $\Delta V_1 / \Delta V_4$	$V_{R\ (rms)} = 50$ mV	33	36	-	dB

IF amplifier/demodulator for FM radio receivers

TDA1599

OPERATING CHARACTERISTICS

V_P = 7.5 to 12 V; T_{amb} = 25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; $V_{i\ (rms)}$= 10 mV at pin 18; de-emphasis of 50 µs; tuned circuit at pins 9 and 10 aligned for symmetrical stop pulses; measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator		V_2 = 1 V				
V_i	input signal for start of limiting (–3 dB) (RMS value, pin 18)	$V_7 = V_{ref}$; FM-MUTE-OFF	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{ref}$	-	15	-	µV
	S/N = 46 dB	$V_7 = V_{ref}$	-	60	-	µV
S/N	signal-to-noise ratio	deviation ±75 kHz	-	82	-	dB
V_o	AF output signal (RMS value, pin 4)		180	200	220	mV
THD	total harmonic distortion without de-emphasis	deviation ±75 kHz; f_m = 1 kHz, I_7 = 0				
	without detuning		-	0.1	0.3	%
	±25 kHz detuning		-	-	0.6	%
	compensated via pin 3	$V_7 = V_{ref}$	-	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4\ (V_3 = 0) - V_4\ (V_3 = V_{ref})$)		10	-	-	mV
α_{AM}	AM suppression on pin 4	$V_7 = V_{ref}$, m = 30 %				
	$V_{i\ (rms)}$ = 0.3 to 1000 mV (RMS value)	on pin 18	46	55	-	dB
	$V_{i\ (rms)}$ = 1 to 300 mV (RMS value)	on pin 18	60	65	-	dB
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 13, see Fig.10				
	for $V_{13} \geq 3.5$ V		-	-	+14.0	kHz
	for $V_{13} \leq 0.3$ V		+22.0	-	-	kHz
Δf	detuning frequency for STOP 1	on pin 12, see Fig.9				
	for $V_{12} \geq 3.5$ V		-	-	–14.0	kHz
	for $V_{12} \leq 0.3$ V		–22.0	-	-	kHz
V_{18}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.8				
		$V_{12,\ 13} \geq 3.5$ V	250	-	-	µV
		$V_{12,\ 13} \leq 0.3$ V	-	-	50	µV
Dynamic mute attenuation, $\alpha = 20 \log (\Delta V_{4\ (FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\ (FM\text{-}MUTE\text{-}ON)})$						
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz V_2 = 1 V	-	14	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Level detector		$I_7 = 0$				
V_6	output voltage	$V_{18\,(rms)} \leq 5\ \mu V$	0.1	-	1.1	V
		$V_{18\,(rms)} = 1\ mV$	3.5	-	4.7	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	$I_5 = -1\ mA$	3.3	3.7	4.1	V
Operation with AM-IF						
Level and stop information (on pins 6, 11, 12, 13 and 14) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonant circuit is provided for demodulator (Fig.17).						

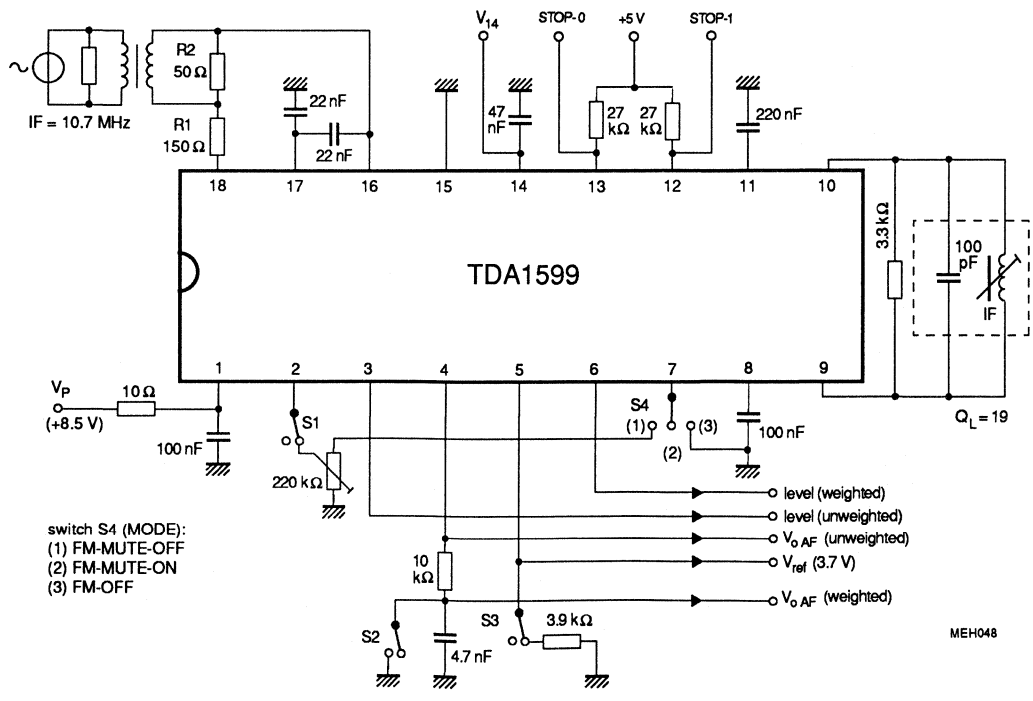
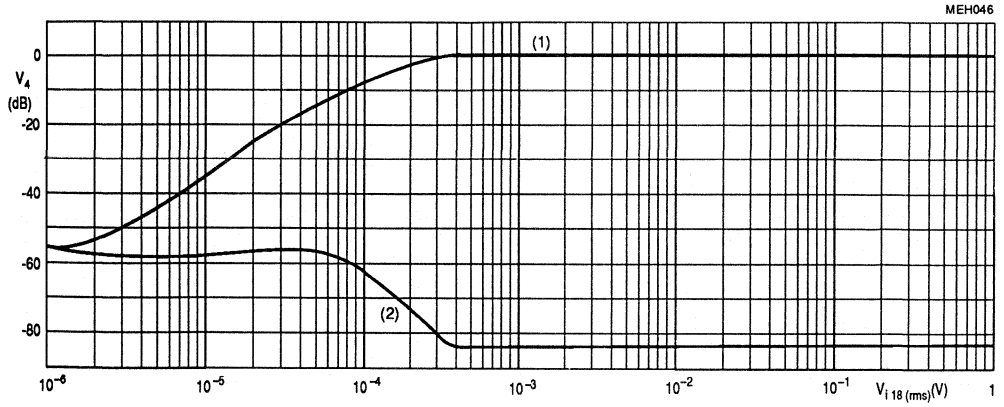
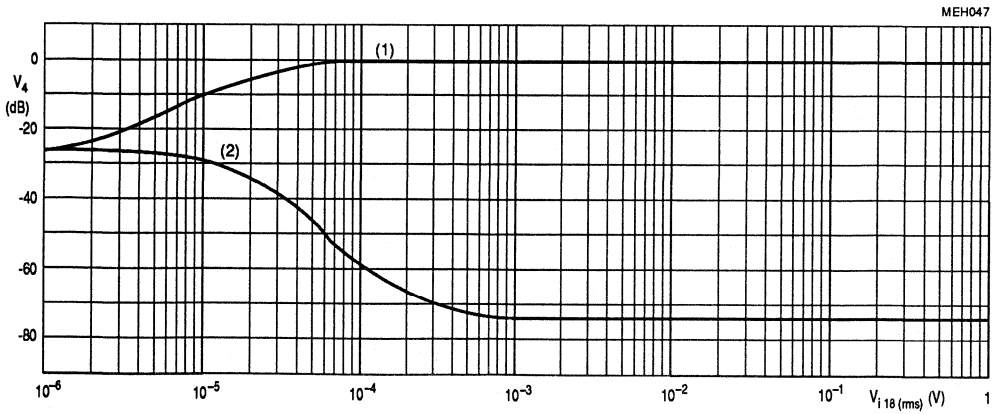


Fig.3 Test circuit.



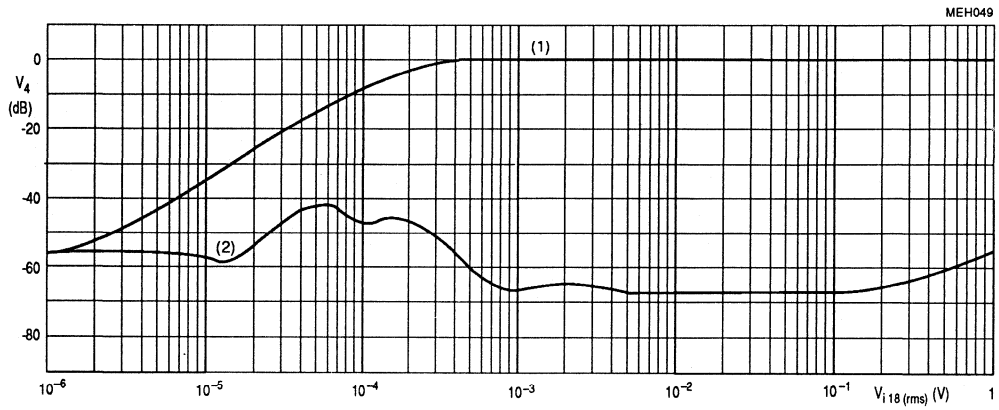
(1) audio signal
(2) noise

Fig.4 FM-MUTE-ON: Audio signal and noise as functions of input signal V_{IIF} (pin 18) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



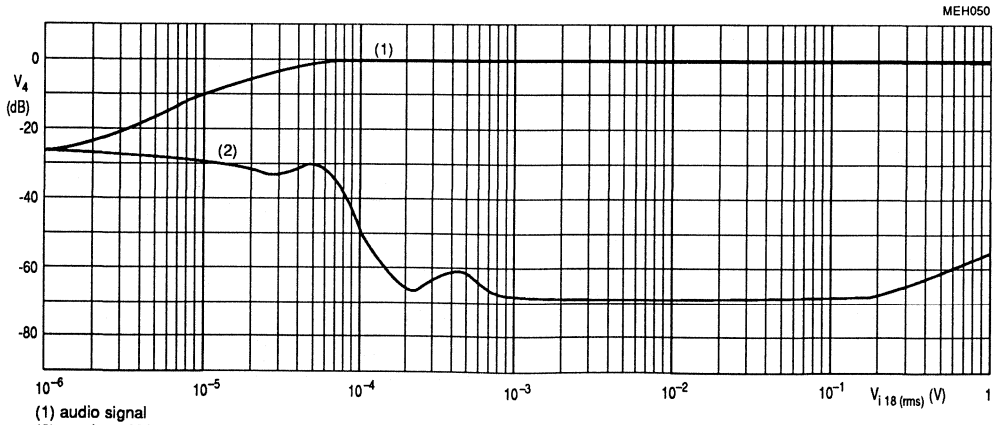
(1) audio signal
(2) noise

Fig.5 FM-MUTE-OFF: Audio signal and noise as functions of input signal V_{IIF} (pin 18) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



(1) audio signal
(2) spurious AM signal

Fig.6 FM-MUTE-ON: Typical AM suppression as a function of input signal V_{iIF} (pin 18) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz, m = 0.3 and a bandwidth from 250 to 15000 Hz.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-OFF: Typical AM suppression as function of input signal V_{iIF} (pin 18) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz, m = 0.3 and a bandwidth from 250 to 15000 Hz.

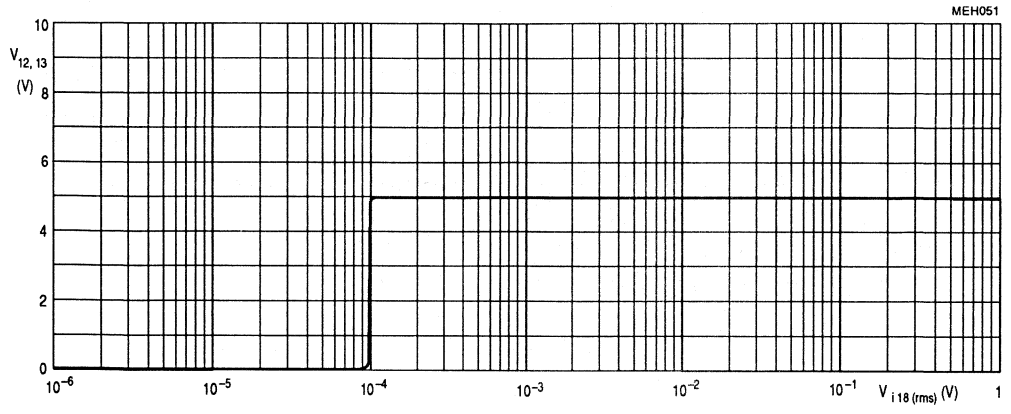


Fig.8 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 18).

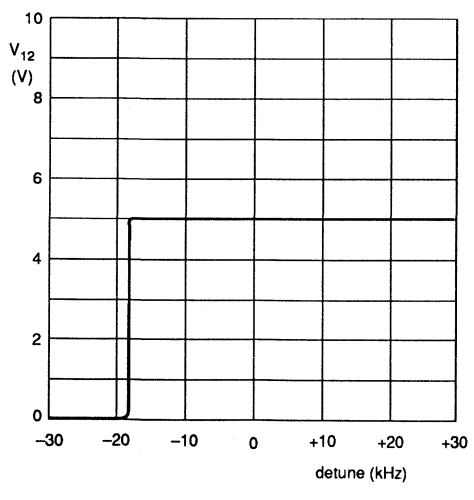


Fig.9 STOP-1 output voltage dependent on $V_{iIF\,(rms)}$ = 10 mV (pin 18).

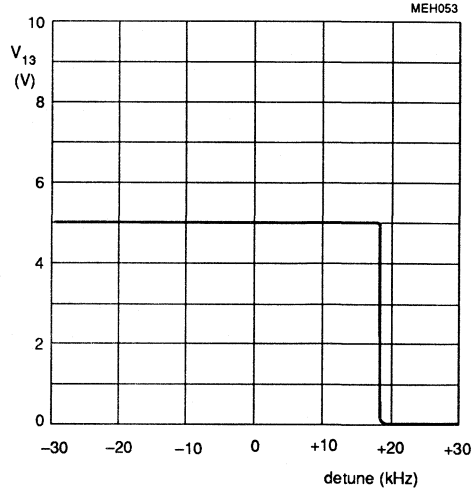


Fig.10 STOP-0 output voltage dependent on $V_{iIF\,(rms)}$ = 10 mV (pin 18).

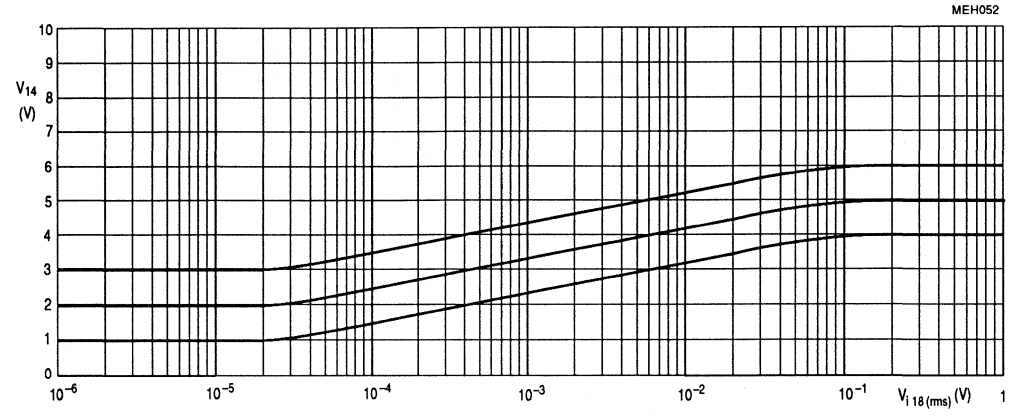


Fig.11 External mute voltage V_{14} dependent on input signal V_{iIF} (pin 18); typical adjusting range (curve at V_2 = 1 V).

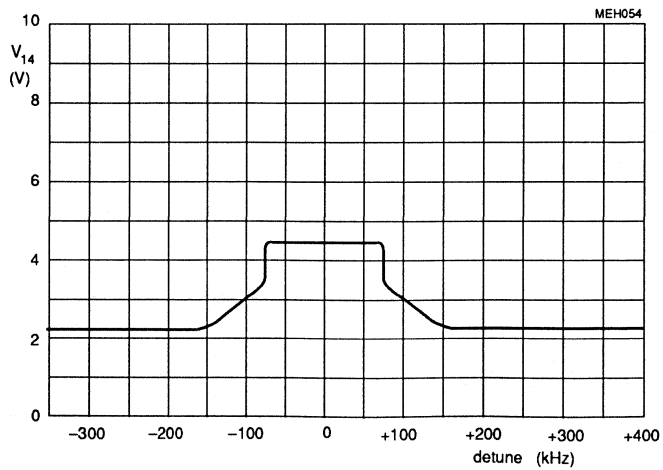


Fig.12 Mute voltage V_{14} dependent on detuning; $V_{iIF\ (rms)}$ = 10 mV.

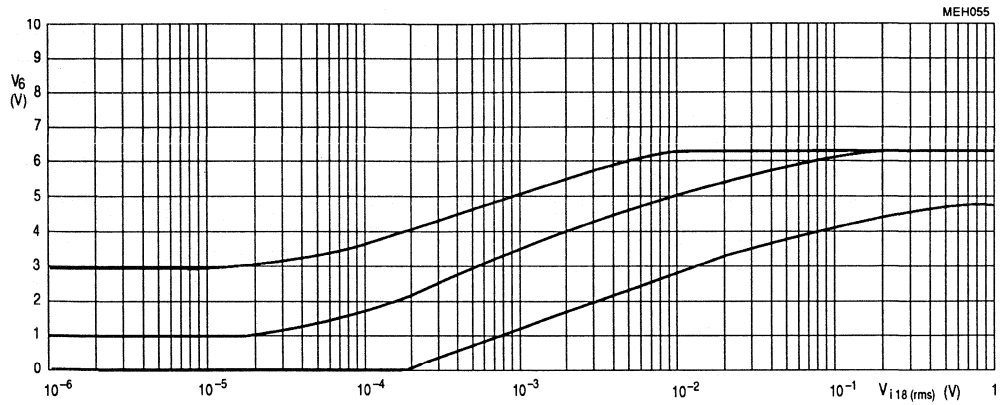


Fig.13 Control voltage V_6 dependent on input signal V_{IIF} (pin 18); typical adjusting range (curve at V_2 = 1 V).

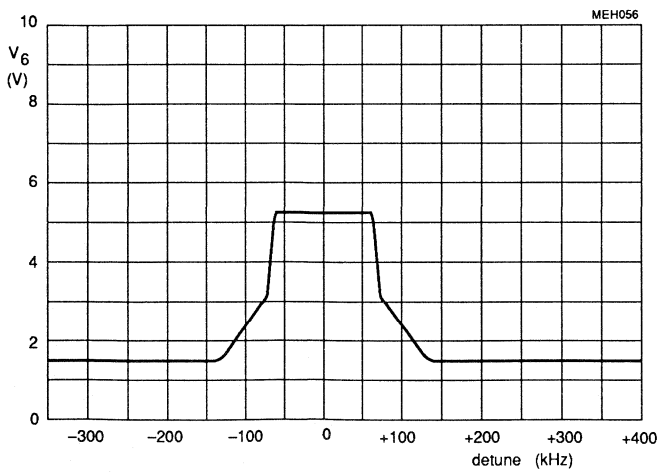


Fig.14 Control voltage V_6 dependent on detuning; $V_{IIF\ (rms)}$ = 10 mV.

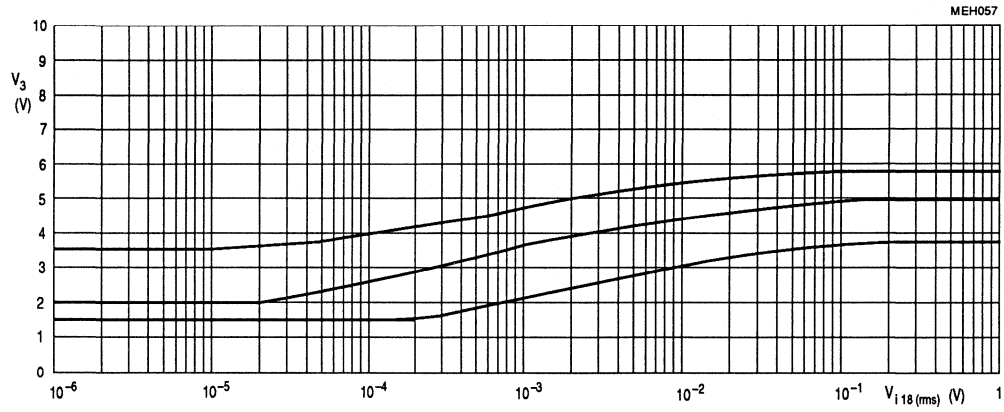


Fig.15 Level output voltage V_3 dependent on input signal V_{iIF} (pin 18); typical adjusting range (curve at V_2 = 1 V).

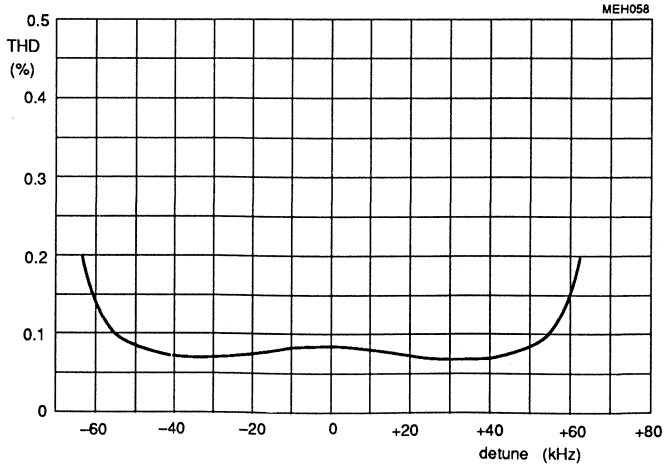


Fig.16 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz, f_m = 1 kHz; V_{iIF} = 10 mV.

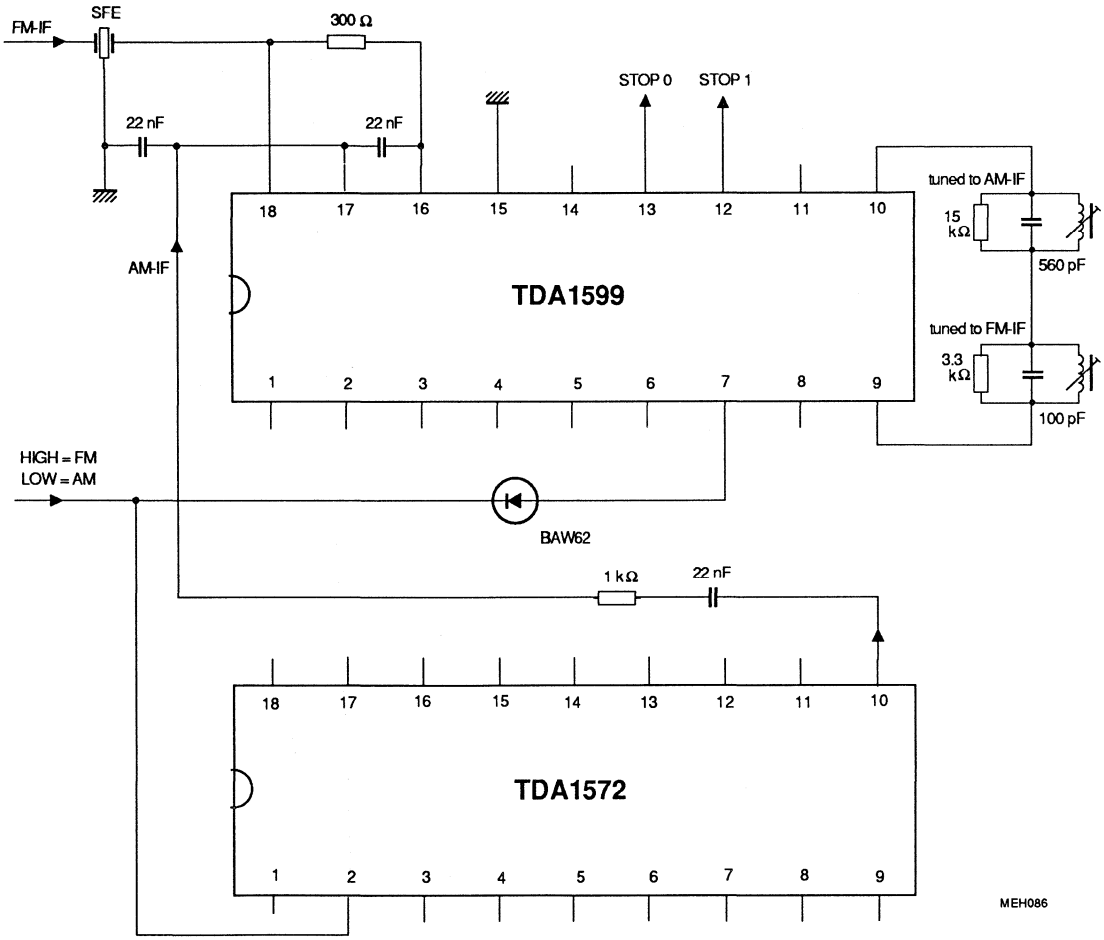


Fig.17 Interface for AM stop pulse application.

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA1599T
IF amplifier/demodulator for FM radio receivers

FEATURES
- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning-dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	-	20	26	mA
V_i	IF input sensivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; Δf = ±75 kHz)	-	82	-	dB
THD	total harmonic distortion (f_m = 1 kHz; Δf = ±75 kHz)	-	0.1	0.3	%
	with K2-adjustment and FM-MUTE-OFF	-	0.07	0.25	%
T_{amb}	operating ambient temperature range	–40	-	+85	°C

GENERAL DESCRIPTION
The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front-ends, stereo decoders and AM receivers circuits.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599T	20	mini-pack	plastic	SOT163

IF amplifier/demodulator for FM radio receivers

TDA1599T

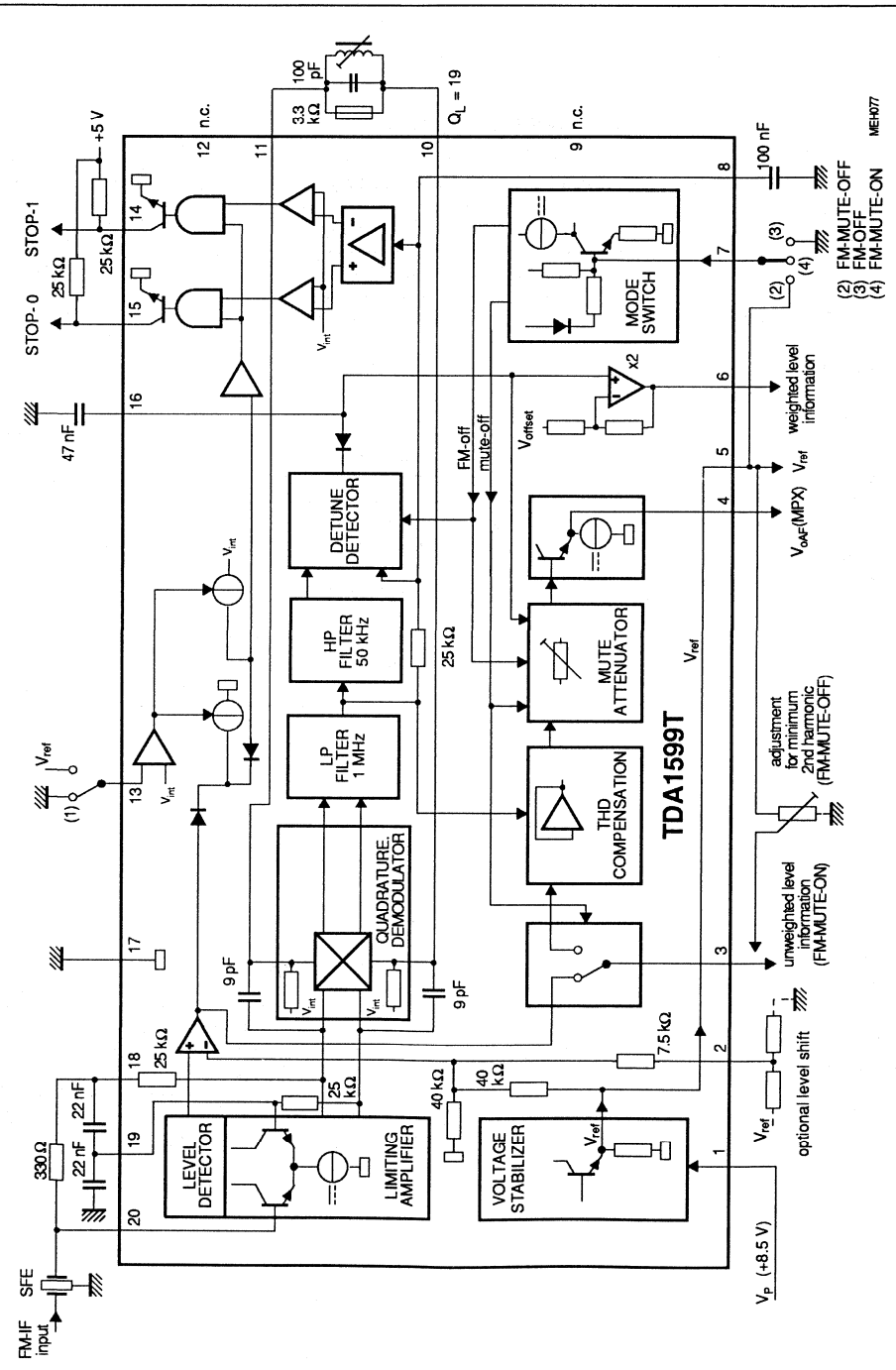


Fig.1 Block diagram and application circuit.

IF amplifier/demodulator for FM radio receivers

TDA1599T

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage (+8.5 V)
LVA	2	level adjustment for stop condition
ULV	3	unweighted level output / K2 adjustment
V_{oAF}	4	audio frequency output (MPX signal)
V_{ref}	5	reference voltage output
WLV	6	weighted level output
MODE	7	mode switch input
DDV	8	detune detector voltage
n. c.	9	not connected
DEMI1	10	demodulator input 1
DEMI2	11	demodulator input 2
n. c.	12	not connected
TSW	13	tau switch input
ST1	14	STOP-1, stop pulse output 1
ST0	15	STOP-0, stop pulse output 0
MUTE	16	muting voltage
GND	17	ground (0 V)
LFB1	18	IF limiter feedback 1
LFB2	19	IF limiter feedback 2
V_{iIF}	20	IF signal input

PIN CONFIGURATION

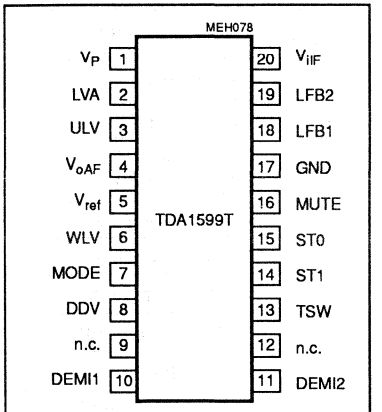


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling. Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feed-back loop give a very stable IF performance. The amplifier gain is virtually independent from temperature changes.

The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. Quadrature detection of the FM signal is performed by feeding one differential amplifier directly from the limiter amplifier output, and the other via an external 90 degrees shase shifting network. The demodulater has good stability and its zero cross-over shift is small. The bandwidth of the demodulator output is restricted to approximately 1 MHz by an internal low-pass filter.

The THD compensation circuit compensates non-linearities introduced by demodulation. For this to operate correctly the demodulator resonant circuit between pins 10 and 11 must have a loaded Q-factor of 19. Consequently there is no need for the demodulator tuned circuit to be adjusted for minimum distortion, instead the adjustment criterium is for a symmetrical stop pulse.

The control voltage for the mute attenuator (pin 16) is generated from the values of the level detector and the detuning detector outputs. The mute attenuator has a fast attack and a slow decay which is determined by the capacitor on pin16. The AF signal is passed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier which introduces an additional voltage shift and gain.

The level detector generates a voltage output which is proportional to the amplitude of the input signal. The unweighted level detector output is available when the mode switch is operating in the FM-MUTE-ON condition.

The open collector tuning stop outputs STOP-0 and STOP-1 (from pins 15 and 14 respectively) are voltages derived from detuning and level of the input signal. If only one tuning-stop output is required, pins 14 and 15 may be tied together.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.3	13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11, 16	–0.3	10	V
V_{n2}	voltage at pins 7, 3, 8, 13, 14, 15, 18, 19, and 20	–0.3	V_P	V
V_{13}	voltage on pin13	-	6	V
$I_{14, 15}$	current at pins 14 and 15	-	2	mA
P_{tot}	power dissipation	-	360	mW
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
V_{ESD}	electrostatic handling*			
	all pins except 5 and 6	-	±2000	V
	pin 5	-	+900	V
			–2000	V
	pin 6	-	+1500	V
			–2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	90	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

IF amplifier/demodulator for FM radio receivers

TDA1599T

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; $V_{i\ (rms)}$= 10 mV at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	-	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		-	0	-	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{ref}$	-	-	V
	input voltage for FM-OFF	AF attenuation >60 dB	-	-	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		-	6	-	pF
AF output (pin 4)						
R_o	output resistance		-	400	-	Ω
V_4	DC output level	$V_{iIF\ (rms)} \leq 5$ µV at pin 20	2.75	3.1	3.45	V
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 15, see Fig.10				
	for $V_{15} \geq 3.5$ V		-	-	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	-	-	kHz
Δf	detuning frequency for STOP 1	on pin 14, see Fig.9				
	for $V_{14} \geq 3.5$ V		-	-	−14.0	kHz
	for $V_{14} \leq 0.3$ V		−22.0	-	-	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.8				
		$V_{14,\ 15} \geq 3.5$ V	250	-	-	µV
		$V_{14,\ 15} \leq 0.3$ V	-	-	50	µV
$V_{14,\ 15}$	output voltage	$I_{14,\ 15}$ = 1 mA	-	-	0.3	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	I_5 = −1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = −1 mA	-	40	80	Ω
TC	temperature coefficient		-	3.3	-	mV/VK

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External muting						
V_{16}	muting voltage at $I_2 = 0$, see Fig.11	$V_{20\ (rms)} \leq 5\ \mu V$	1.45	1.75	2.05	V
		$V_{20\ (rms)} = 1\ mV$	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 $\mu V \leq V_{20} \leq 100$ mV)					
	20 $\Delta \log V_{20} = 20$ dB($\Delta V_{16} / \Delta \log V_{20}$)		-	0.85	-	V/dec
Internal mute, $\alpha = 20 \log (\Delta V_{4\ (FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\ (FM\text{-}MUTE\text{-}ON)})$						
α	mute voltage	$V_{16} \geq V_{ref}$	-	0	-	dB
		$V_{16} = 0.77\ V_{ref}$	1.5	-	4.5	dB
		$V_{16} = 0.55\ V_{ref}$	-	20	-	dB
I_{16}	current for capacitor on pin16					
	charge current	$V_{13} = 0$ V	-	–8	-	µA
	discharge current	$V_{13} = 0$ V	-	+120	-	µA
	charge current	$V_{13} = V_{ref}$	-	–100	-	µA
	discharge current	$V_{13} = V_{ref}$	-	+120	-	µA
Level detector						
R_6	output resistance		-	-	500	Ω
V_6	output voltage at $I_2 = 0$, see Fig,13	$V_{20\ (rms)} \leq 5\ \mu V$	0.1	-	1.1	V
		$V_{20\ (rms)} = 1\ mV$	3.5	-	4.7	V
		±200 kHz detuning	1.2	1.5	1.8	V
ΔV_6	output voltage at detuning	±45 kHz detuning	-	-	0.2	V
TC	temperature coefficient		-	3.3	-	mV/VK
Δf	detuning frequency, see Fig.12	$V_6 = 1.8$ V	90	-	160	kHz
S	steepness of control voltage (slope: 50 $\mu V \leq V_{20} \leq 50$ mV)					
	20 $\Delta \log V_{20} = 20$ dB ($\Delta V_6 / \Delta \log V_{20}$)		1.4	1.7	2.0	V/dec
$\Delta V_6 / \Delta f$	slope of output voltage at detuning	$\Delta f = 125 \pm 20$ kHz	-	35	-	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm \Delta V_6 / V_{ref}$	0.42	0.5	-	V/V
	gain	$-\Delta V_6 / \Delta V_2$	-	1.7	-	V/V
	range by pin 2	$\pm \Delta V_{16} / V_{ref}$	0.21	0.25	-	V/V
	gain	$-\Delta V_{16} / \Delta V_2$	-	0.85	-	V/V
Power supply ripple rejection		f = 1 kHz				
RR_{1000}	20 log $\Delta V_1 / \Delta V_4$	$V_{R\ (rms)} = 50$ mV	33	36	-	dB

OPERATING CHARACTERISTICS

V_P = 7.5 to 12 V; T_{amb} = 25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; $V_{i\,(rms)}$= 10 mV at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator		V_2 = 1 V				
V_i	input signal for start of limiting (–3 dB) (RMS value, pin 20)	$V_7 = V_{ref}$; FM-MUTE-OFF	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{ref}$	-	15	-	µV
	S/N = 46 dB	$V_7 = V_{ref}$	-	60	-	µV
S/N	signal-to-noise ratio	deviation ±75 kHz	-	82	-	dB
V_o	AF output signal (RMS value, pin 4)		180	200	220	mV
THD	total harmonic distortion without de-emphasis	deviation ±75 kHz; f_m = 1 kHz, I_7 = 0				
	without detuning		-	0.1	0.3	%
	±25 kHz detuning		-	-	0.6	%
	compensated via pin 3	$V_7 = V_{ref}$	-	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4\,(V_3 = 0) - V_4\,(V_3 = V_{ref})$)		10	-	-	mV
α_{AM}	AM suppression on pin4	$V_7 = V_{ref}$, m = 30 %				
	$V_{i\,(rms)}$ = 0.3 to 1000 mV (RMS value)	on pin20	46	55	-	dB
	$V_{i\,(rms)}$ = 1 to 300 mV (RMS value)	on pin20	60	65	-	dB
Dynamic mute attenuation,	$\alpha = 20 \log (\Delta V_{4\,(FM\text{-}MUTE\text{-}OFF)} / \Delta V_{4\,(FM\text{-}MUTE\text{-}ON)})$					
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz V_2 = 1 V	-	14	-	dB
Tuning stop detector						
Δf	detuning frequency for STOP 0	on pin 15, see Fig.10				
	for $V_{15} \geq 3.5$ V		-	-	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	-	-	kHz
Δf	detuning frequency for STOP 1	on pin14, see Fig.9				
	for $V_{14} \geq 3.5$ V		-	-	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	-	-	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.8				
		$V_{14,\,15} \geq 3.5$ V	250	-	-	µV
		$V_{14,\,15} \leq 0.3$ V	-	-	50	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Level detector		$I_7 = 0$				
V_6	output voltage	$V_{20\ (rms)} \leq 5\ \mu V$	0.1	-	1.1	V
		$V_{20\ (rms)} = 1\ mV$	3.5	-	4.7	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	$I_5 = -1\ mA$	3.3	3.7	4.1	V
Operation with AM-IF						
Level and stop information (on pins 6, 13, 14, 15 and 16) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonant circuit is provided for demodulator (Fig.17).						

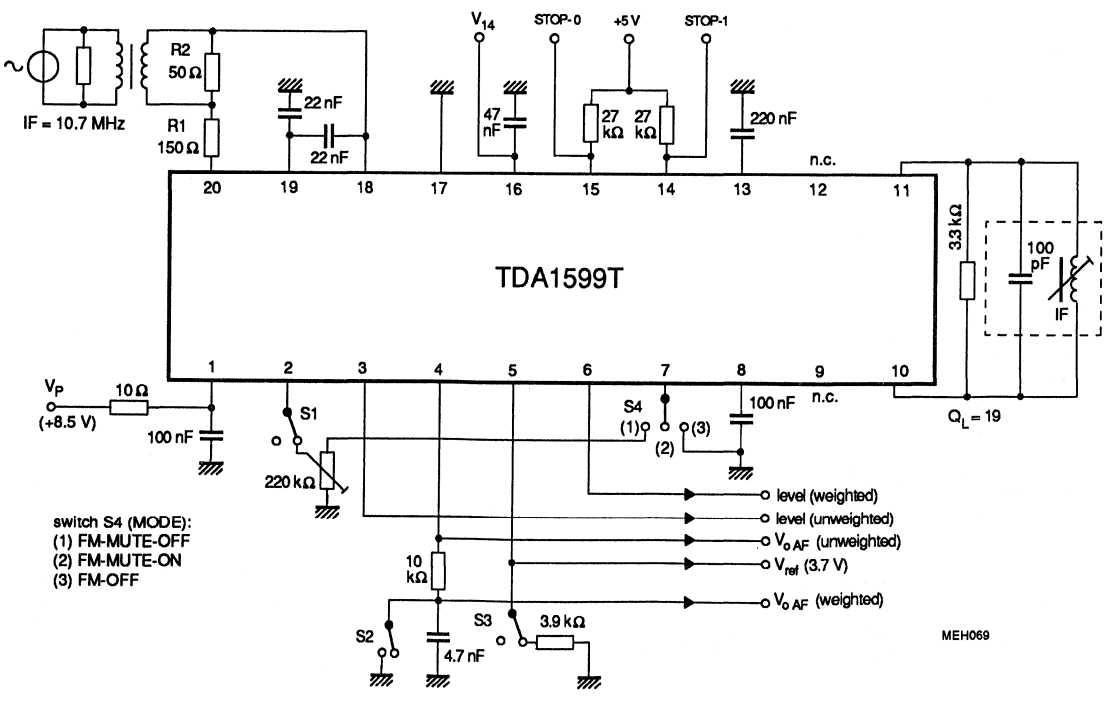
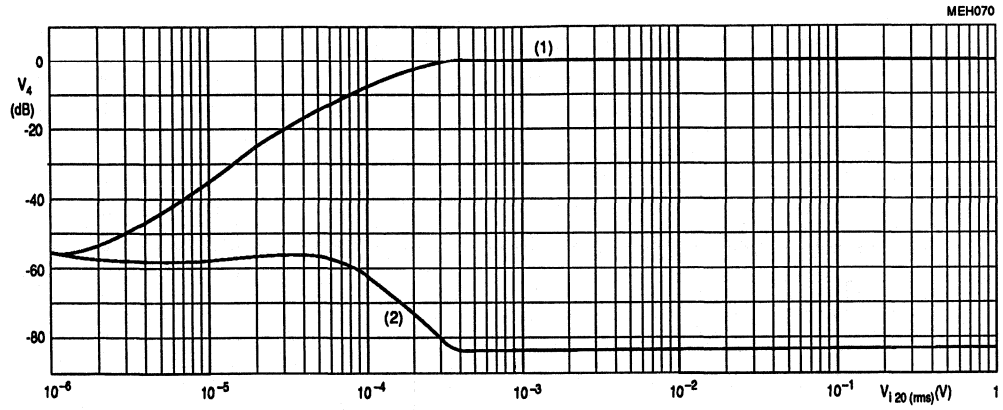
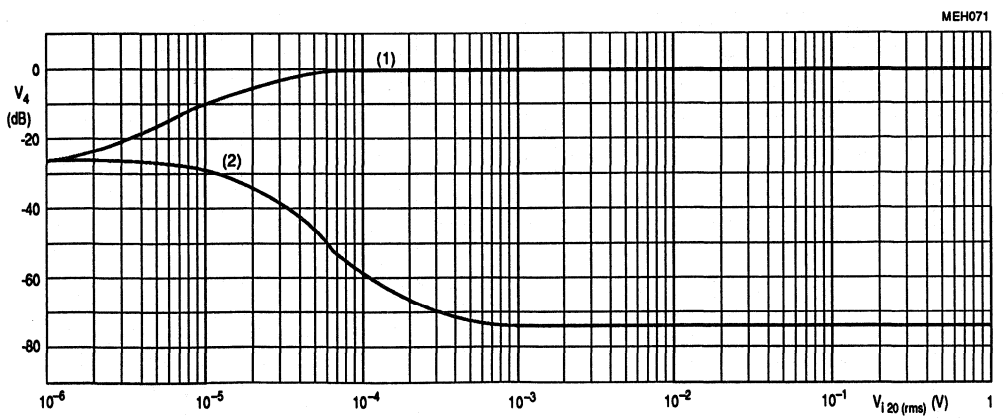


Fig.3 Test circuit.



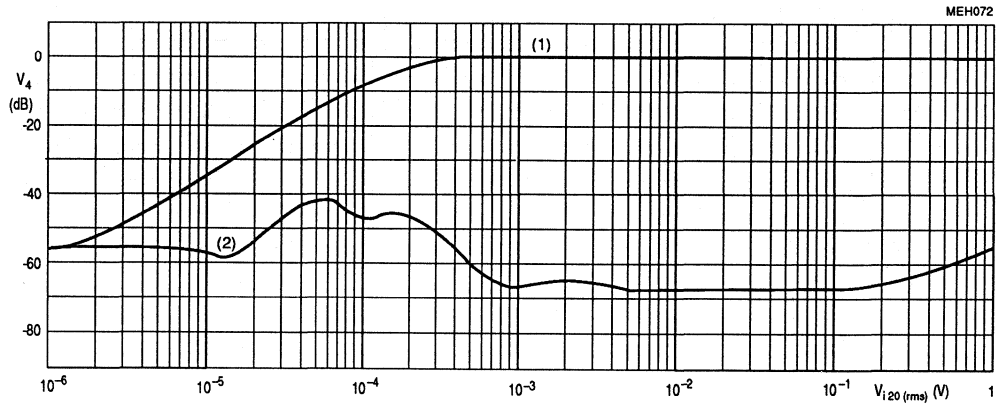
(1) audio signal
(2) noise

Fig.4 FM-MUTE-ON: Audio signal and noise as functions of input signal V_{IIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



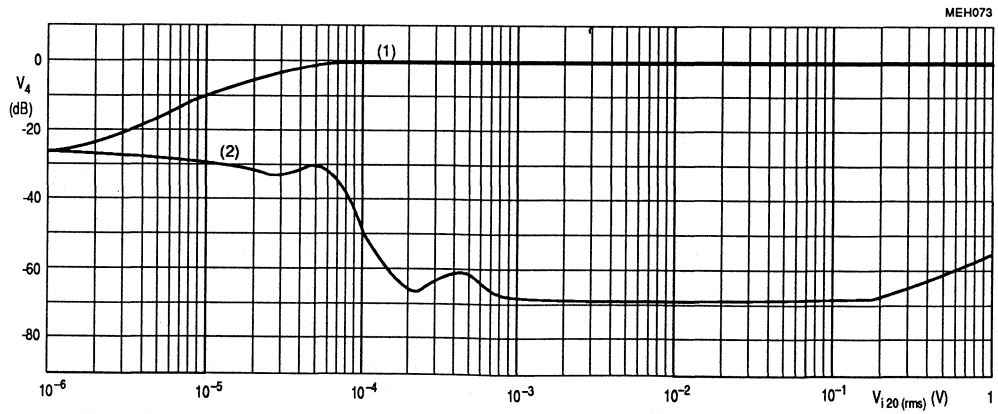
(1) audio signal
(2) noise

Fig.5 FM-MUTE-OFF: Audio signal and noise as functions of input signal V_{IIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



(1) audio signal
(2) spurious AM signal

Fig.6 FM-MUTE-ON: Typical AM suppression as a function of input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz, m = 0.3 and a bandwidth from 250 to 15000 Hz.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-OFF: Typical AM suppression as a function of input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz, m = 0.3 and a bandwidth from 250 to 15000 Hz.

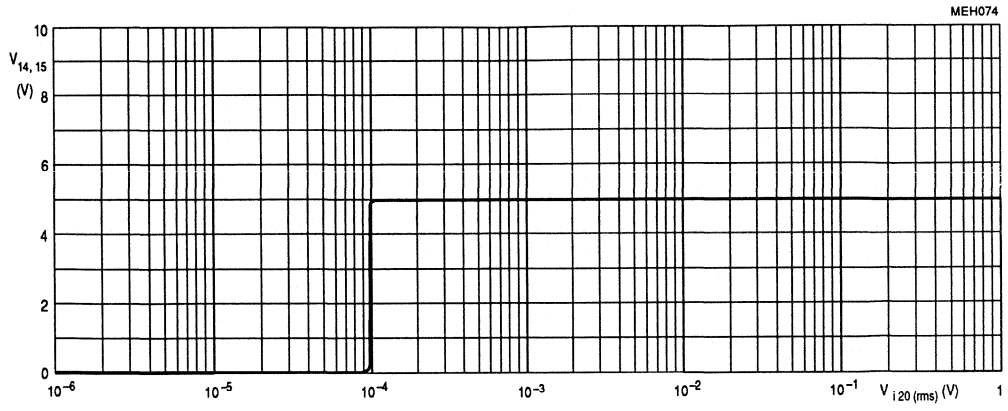


Fig.8 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

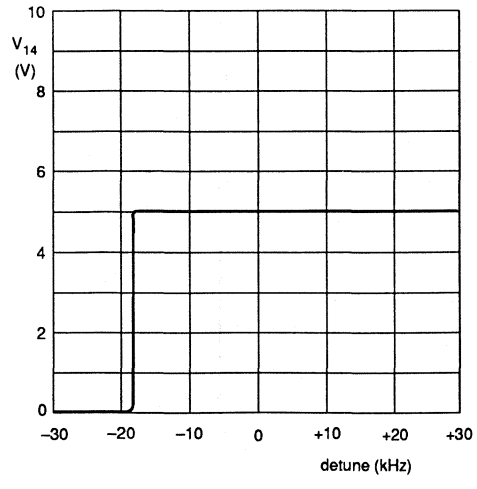


Fig.9 STOP-1 output voltage dependent on $V_{iIF\,(rms)}$ = 10 mV (pin 20).

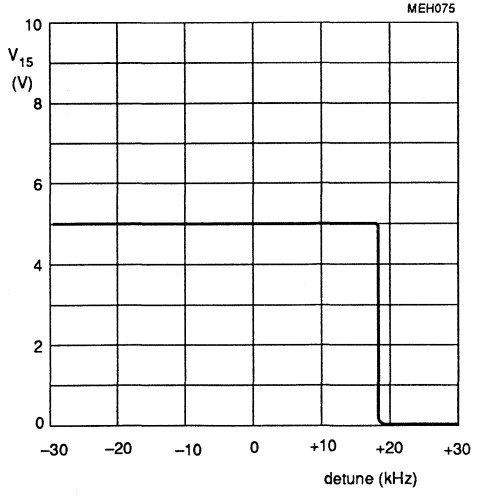


Fig.10 STOP-0 output voltage dependent on $V_{iIF\,(rms)}$ = 10 mV (pin 20).

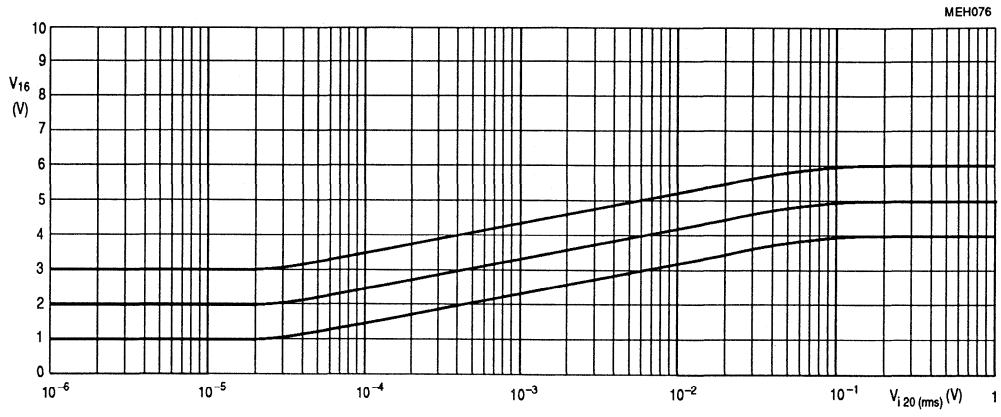


Fig.11 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range (curve at V_2 = 1 V).

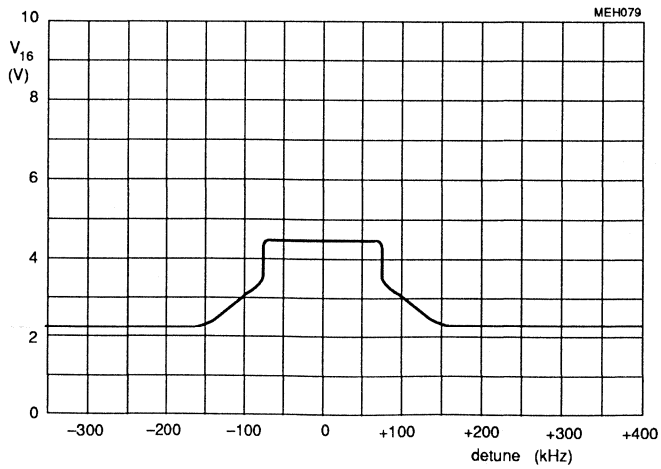


Fig.12 Mute voltage V_{16} dependent on detuning; $V_{iIF\ (rms)}$ = 10 mV.

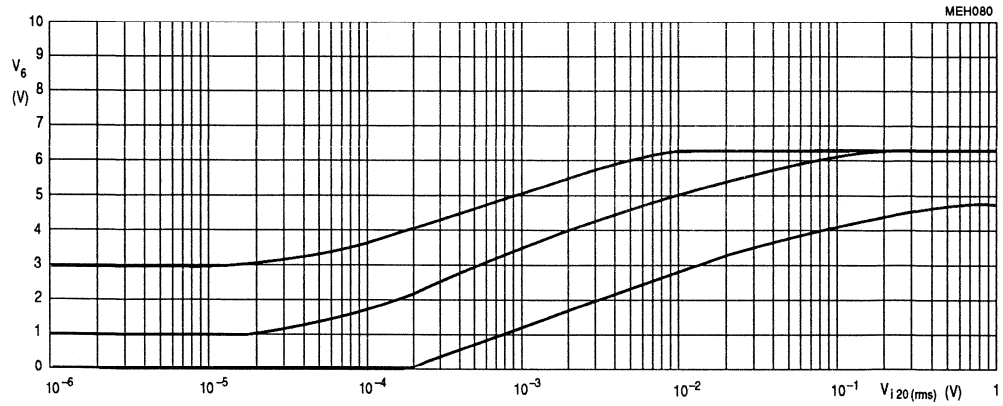


Fig.13 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range (curve at V_2 = 1 V).

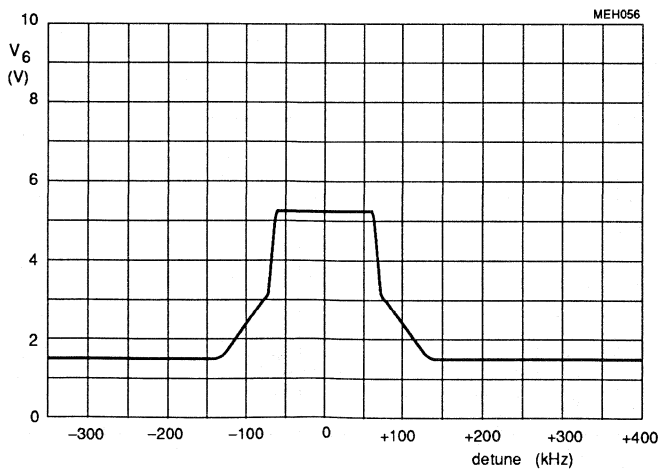


Fig.14 Control voltage V_6 dependent on detuning; $V_{iIF\ (rms)}$ = 10 mV.

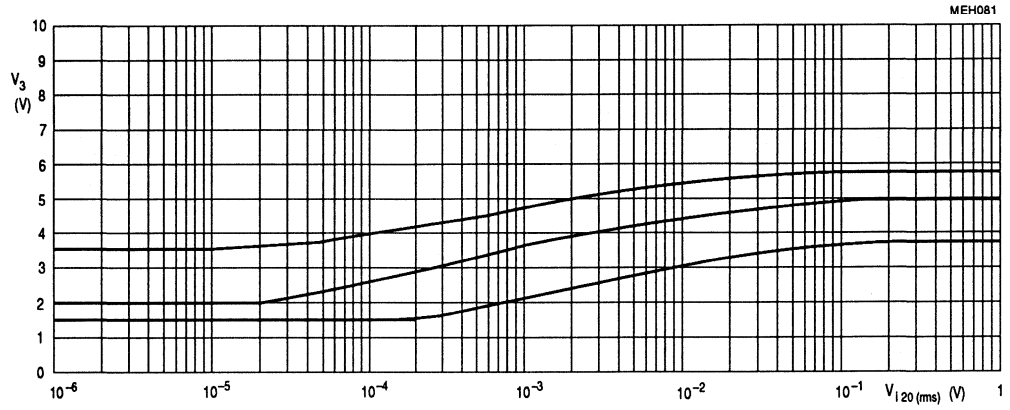


Fig.15 Level output voltage V_3 dependent on input signal V_{IIF} (pin 20); typical adjusting range (curve at V_2 = 1 V).

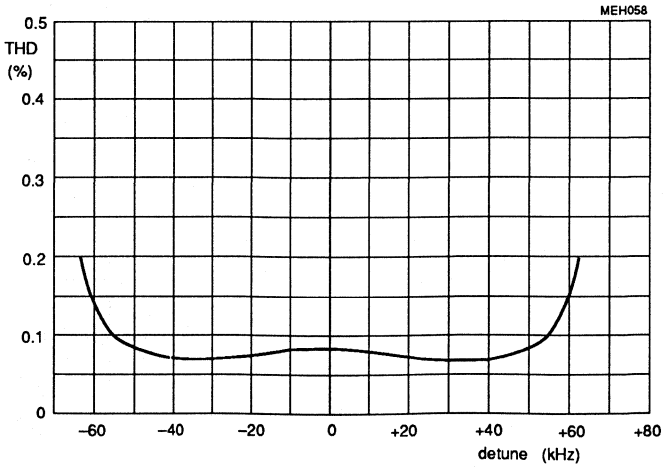


Fig.16 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz, f_m = 1 kHz; V_{IIF} = 10 mV.

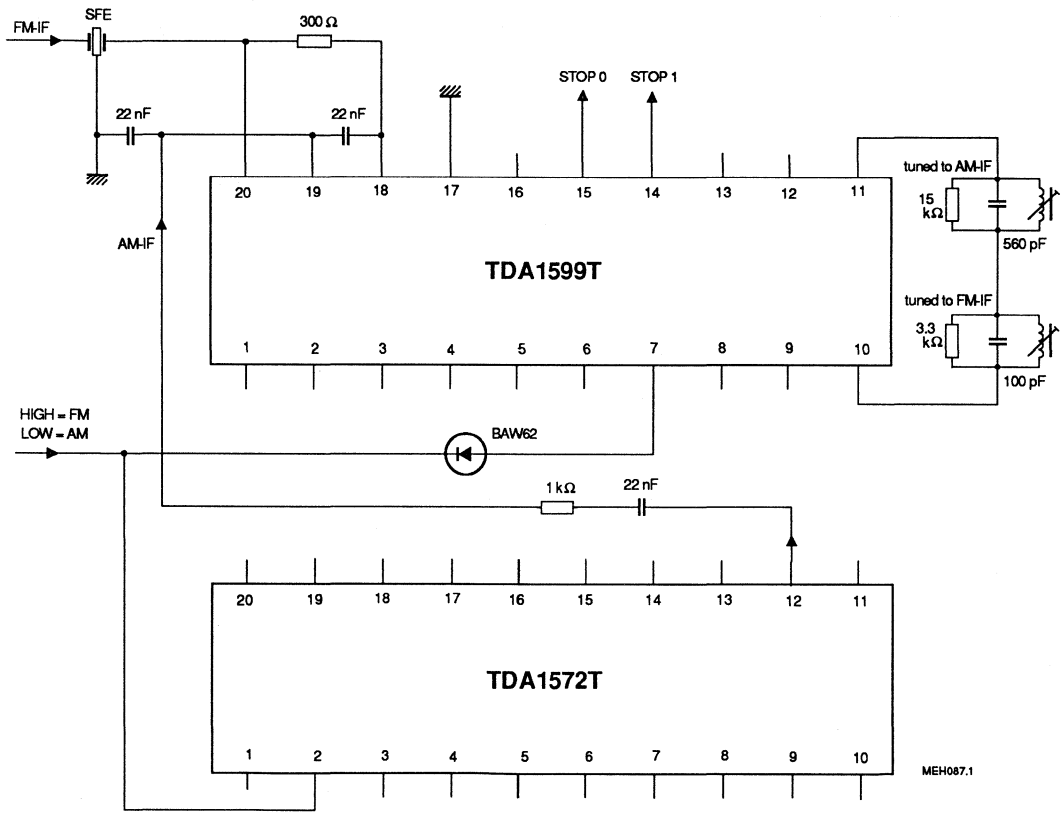


Fig.17 Interface for AM stop pulse application.

MULTI-FUNCTION OSCILLATOR SWITCH FOR AN AUDIO CASSETTE RECORDER

GENERAL DESCRIPTION

The TDA1600 is a bipolar circuit designed for high fidelity cassette recorders. This device contains several functions (see 'features') which can be selected by external d.c. voltage levels or via a microprocessor. The TDA1600 operates from a mains-fed asymmetrical power supply. For application purposes the voltage output can be either ½ V_P asymmetrical or ½ V_P symmetrical. The output of all the functions are current protected.

Features

- Stereo playback amplifier
- Electronic switch for playback equalization
- Electronic head-switch (two times)
- Erase and bias oscillator
- LED driver
- Tape selector
- Reference voltage source (½ V_P)
- Logic part

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	–	20	V
Playback amplifier						
Open loop gain		Go	–	106	–	dB
Minimum closed loop gain		Gc	–	30	–	dB
S/N ratio	V_O = 50 mV	S/N	–	65	–	dB
Total harmonic distortion	V_O = 50 mV	THD	–	–60	–	dB
Head-switch						
Maximum voltage (peak-to-peak value)		V_{OM}	–	–	120	V
Oscillator						
Frequency range		f_o	60	–	120	kHz
Maximum output current (peak value)		I_{OM}	–	–	80	mA
Maximum output voltage (peak value)		V_{OM}	–	–	40	V
LED driver						
Maximum d.c. output current		I_{OM}	–	–	± 15	mA
Reference voltage						
Output voltage		V_{REF}	–	½ V_P	–	V
Maximum load current		$I_{L\,max}$	–	–	± 18	mA
Logic part						
Input current		I_I	–	–1	–	μA

PACKAGE OUTLINE

24-lead DIL; plastic, with internal heatspreader (SOT101B).

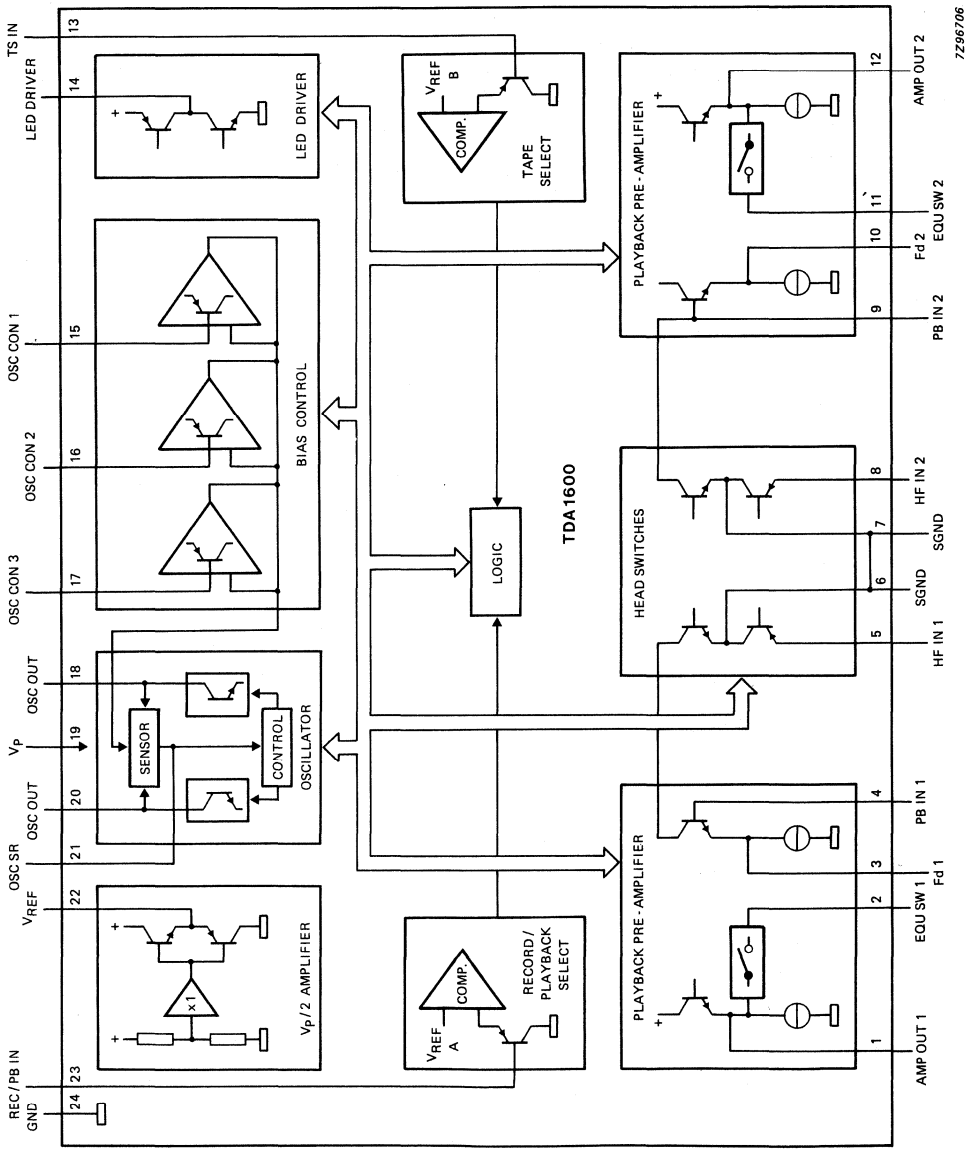


Fig. 1 Block diagram.

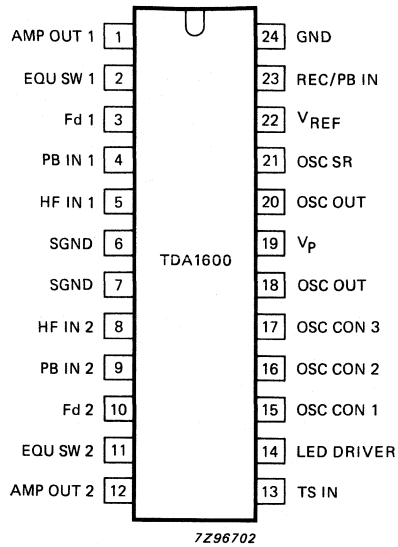


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PINNING

1	AMP OUT 1	pre-amplifier 1 output
2	EQU SW 1	equalization switching for pre-amplifier 1
3	Fd 1	feedback to pre-amplifier 1
4	PB IN 1	input to pre-amplifier 1 from playback side of head
5	HF IN 1	H.F. input from recording side of head
6	SGND	signal ground
7	SGND	signal ground
8	HF IN 2	H.F. input from recording side of head
9	PB IN 2	input to pre-amplifier 2 from playback side of head
10	Fd 2	feedback to pre-amplifier 2
11	EQU SW 2	equalization switching for pre-amplifier 2
12	AMP OUT 2	pre-amplifier 2 output
13	TS IN	tape select input
14	LED DRIVER	LED driver output
15	OSC CON 1	control input for oscillator
16	OSC CON 2	control input for oscillator
17	OSC CON 3	control input for oscillator
18	OSC OUT	oscillator output
19	V_P	supply voltage
20	OSC OUT	oscillator output
21	OSC SR	smoothing oscillator regulator
22	V_{REF}	reference voltage
23	REC/PB IN	record/playback select input
24	GND	ground

FUNCTIONAL DESCRIPTION

Playback amplifier

The playback amplifier is a low noise pre-amplifier which is internally connected to the head-switch. The gain of the amplifier can be externally fixed, to provide an optimal output voltage for a noise reduction system (e.g. Dolby). The playback constants (70 μs and 120 μs) are determined by external components, while the switch over is controlled by the logic part of the circuit. In the record mode, the playback amplifier is switched OFF.

Head-switch

The electronic head-switch has two positions:

- record mode: the playback side of the head is switched to signal ground, while the recording side is opened to allow the bias and audio current to be fed to the head.
- playback mode: the recording side of the head is switched to signal ground, while the playback side is connected to the input of the playback amplifier.

Both of these positions are controlled by the logic part of the circuit.

Erase and bias oscillator

Every audio hi-fidelity cassette recorder contains a high frequency bias current for linearization of the magnetic recording process on the tape. The high frequency bias current is added to the audio current (from a recording amplifier) and fed into the recording head. The oscillator generates a voltage which is converted into a bias current by an external resistor. The oscillator output voltage is dependent upon the type of tape selected; Ferro (FeO_2), Chrome (CrO_2) or Metal. The selection of the voltage level is controlled by the logic part, while the ratio level is determined by four external resistors. The oscillator also provides the current necessary for erasing the tape. The bias oscillator is only activated during the record mode.

LED driver

This circuit provides the voltage which drives the LED tape indicator. The circuit has three output positions; 0, ½ V_P or V_P, all of which are controlled by the logic part of the device.

Reference voltage

The circuit delivers an output voltage which is half the supply voltage. By using this output as signal ground, a symmetrical power supply is available (+ ½ V_P and −½ V_P), which can be used for the overall recording system. This application allows some flexibility in the choice of other IC's and components for the overall system.

Logic part

The logic part converts the incoming information, from the tape selector switches and from the record/playback switch, into the necessary switching signals. The switching signals are required for the analogue parts of the circuit. This conversion is determined by the input signal level and is independent of the rise or fall-time of this signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_P	–	20	V
Logic input voltage	pins 13 and 23	V_I	0	V_P	V
Control input voltage	pins 15, 16 and 17	V_I	0	V_P	V
Head-switch voltage	pins 5 and 8	V_I	−60	+60	V
Total power dissipation	T_{amb} = +60 °C	P_{tot}	–	2,5	W
Storage temperature range		T_{stg}	−65	+150	°C
Junction temperature		T_j	–	+150	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 15 V; f = 315 Hz; T_{amb} = 25 °C, unless otherwise specified (see Fig. 6)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	10	15	20	V
Supply current	note 1,					
	playback mode	I_P	–	25	45	mA
	record mode	I_P	–	50	70	mA
Playback amplifier	position FeO_2					
Open loop gain		Go	86	106	–	dB
Closed loop gain	note 2, FeO_2	Gc	49	50	51	dB
Closed loop gain	CrO_2 and Metal	Gc	30	31	32	dB
Output voltage	V_I = 150 μV	V_O	–	50	–	mV
Total harmonic distortion	V_O = 50 mV	THD	–	–60	–55	dB
	V_O = 500 mV	THD	–	–50	–45	dB
S/N ratio	note 3; weighted curve 20 Hz to 20 kHz at position CrO_2 and Metal	S/N	59	65	–	dB
	see Fig. 5, weighted curve A (IEC 179) at position CrO_2 and Metal	S/N	–	61	–	dB
	weighted curve 20 Hz to 20 kHz at position CrO_2 and Metal	S/N	–	54	–	dB
Frequency response				see Fig. 3		

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Channel separation	V_O = 50 mV		45	60	–	dB
Ripple rejection	V_{rip} = 100 mV, f = 100 Hz and R_S = 1 kΩ	RR	35	41	–	dB
Input impedance		Z_I	100	–	–	kΩ
Input bias current		I_{bias}	–	0,8	1,5	μA
D.C. output voltage w.r.t. $V_{6/7}$	pins 6 and 7	V_O	−1,1	−0,9	–	V
D.C. output voltage w.r.t. $V_{6/7}$	record mode pins 6 and 7	V_O	−1,1	−0,9	–	V
Input signal suppression	record mode, V_I = 20 mV, f = 85 kHz		–	65	–	dB
Head-switch						
Impedance ON	playback mode, (V_{23} = 2 V) between pins 5/8 and 6/7 at I = 100 μA (rms)	Zon	–	40	80	Ω
Impedance ON	record mode, (V_{23} = 13 V) between pins 4/9 and 6/7 at I = 1,5 mA (rms) f = 85 kHz	Zon	–	10	30	Ω
Leakage current	between pins 5/8 and 6/7 at V_{DC} = ± 60 V	$\|I_I\|$	–	1,0	2,5	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Erase and bias oscillator						
Oscillator frequency	note 4	f_o	–	85	–	kHz
Output current (peak value)		I_O	–	–	80	mA
Maximum output voltage (peak)	V_P = 20 V	V_{OM}	–	–	40	V
Control voltage range	pins 15, 16 and 17	V_O	–13	–	–2	V
Output voltage (peak) w.r.t. V_P	note 5, control voltage = –2 V	V_O	1,8	2,0	2,2	V
Output voltage (peak) w.r.t. V_P	note 5, control voltage = –13 V	V_O	12,8	13,0	13,2	V
Input current at control inputs		I_I	–4	–	–	μA
Distortion of output voltage	between pins 18 and 20, I_O = 80 mA	THD	–	–65	–	dB
LED driver						
Output voltage	V_{13} = 15 V, (FeO_2) and R_{load} = 10 kΩ	$\lvert V_{14\text{-}22}\rvert$	–	–	10	V
Output voltage loss	V_{13} = 7,5 V, (CrO_2) and I_O = –15 mA	$V_{14\text{-}24}$	1,5	2,0	2,5	V
Output voltage loss	V_{13} = 0 V, (Metal) and I_O = 15 mA	$V_{14\text{-}19}$	1,5	2,0	2,5	V
Output current limit		I_O	± 15	± 20	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage						
Output voltage	note 6, no external load	V_{22-24}	7,25	7,50	7,75	V
Output voltage deviation	ΔI_I = 15 mA	ΔV_O	–	30	90	mV
Load current		I_L	–	–	18	mA
Output current limit		I_{OI}	20	30	–	mA
Logic inputs						
Input for tape selection	pin 13					
Input current		I_I	–	–1	–20	μA
Input voltage	FeO_2	V_I	11	–	15	V
Input voltage	CrO_2	V_I	6	–	9	V
Input voltage	Metal	V_I	0	–	4	V
Input for record/playback mode selection	pin 23					
Input current		I_I	–	–1	–20	μA
Input voltage	see Fig. 4					
	playback mode	V_I	0	–	4	V
	record mode	V_I	11	–	15	V

DEVELOPMENT DATA

Notes to the characteristics

1. The supply current is measured in the test circuit without loading the LED driver or the additional load of the ½ V_P amplifier. In the record mode the tape selector is at Metal position.
2. The closed loop gain will be fixed by R_{FeO_2} in the FeO_2 position, by $R_{FeO_2}//R_{CrO_2}$ in the CrO_2 position and by $R_{FeO_2}//R_{CrO_2}$ in the Metal position. The gain of the amplifier must not be lower than 30 dB.
3. The S/N ratio is related to V_O = 50 mV (at f = 315 Hz) and R_S = 1 kΩ.
4. The oscillator frequency is determined by L and C_L and may be adjusted between 60 kHz and 120 kHz.
5. The voltage applied to the control inputs (pins 15, 16 and 17) is $-(V_P - 2\ V)$ min. and –2 V max. with respect to V_P.
6. The output voltage is independent of the operating mode (playback/record).

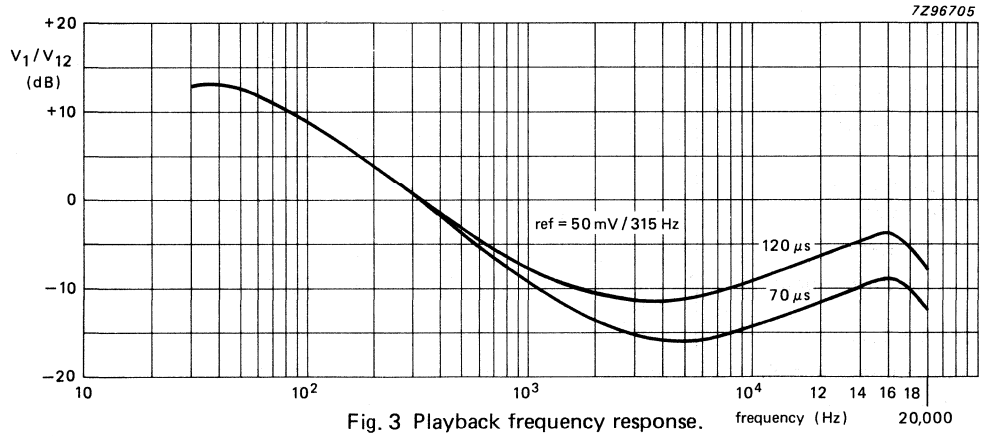


Fig. 3 Playback frequency response.

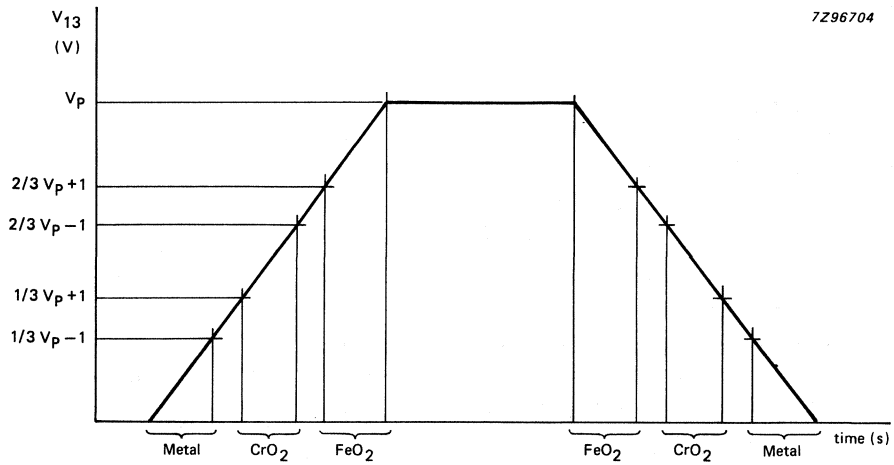


Fig. 4(a) Tape select input.

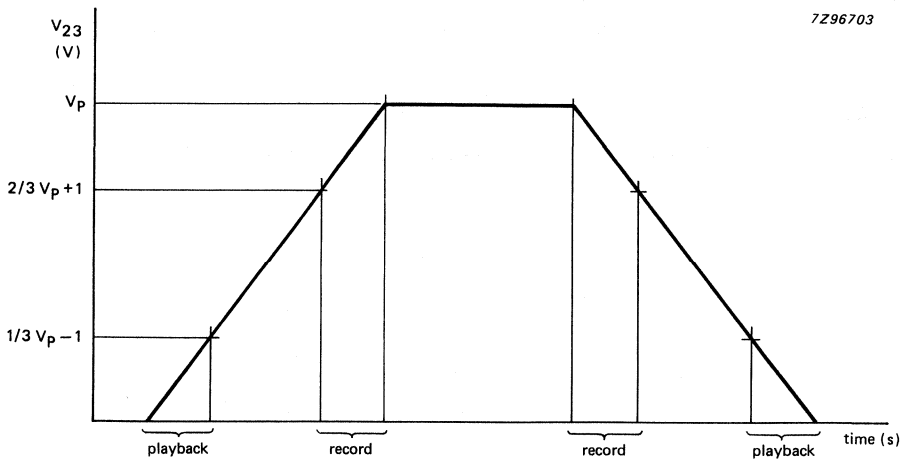


Fig. 4(b) Record/playback input.

APPLICATION INFORMATION

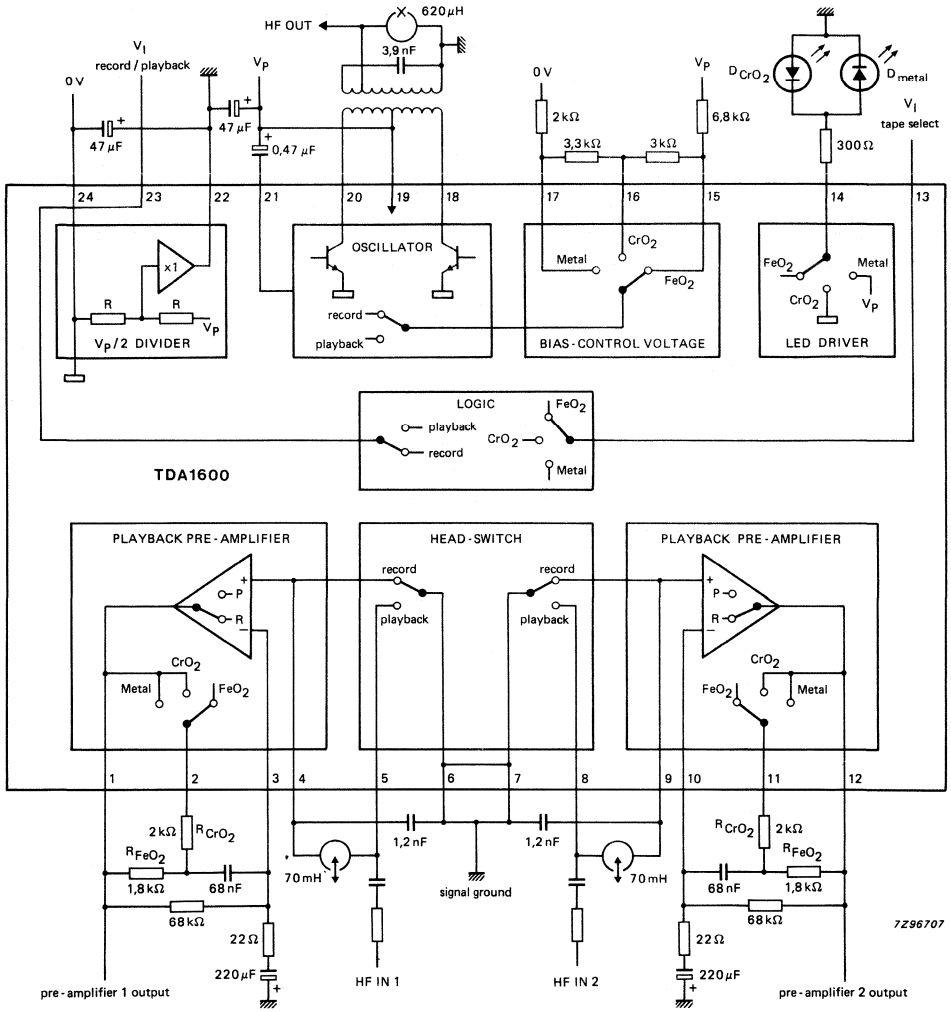


Fig. 5 Application diagram.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

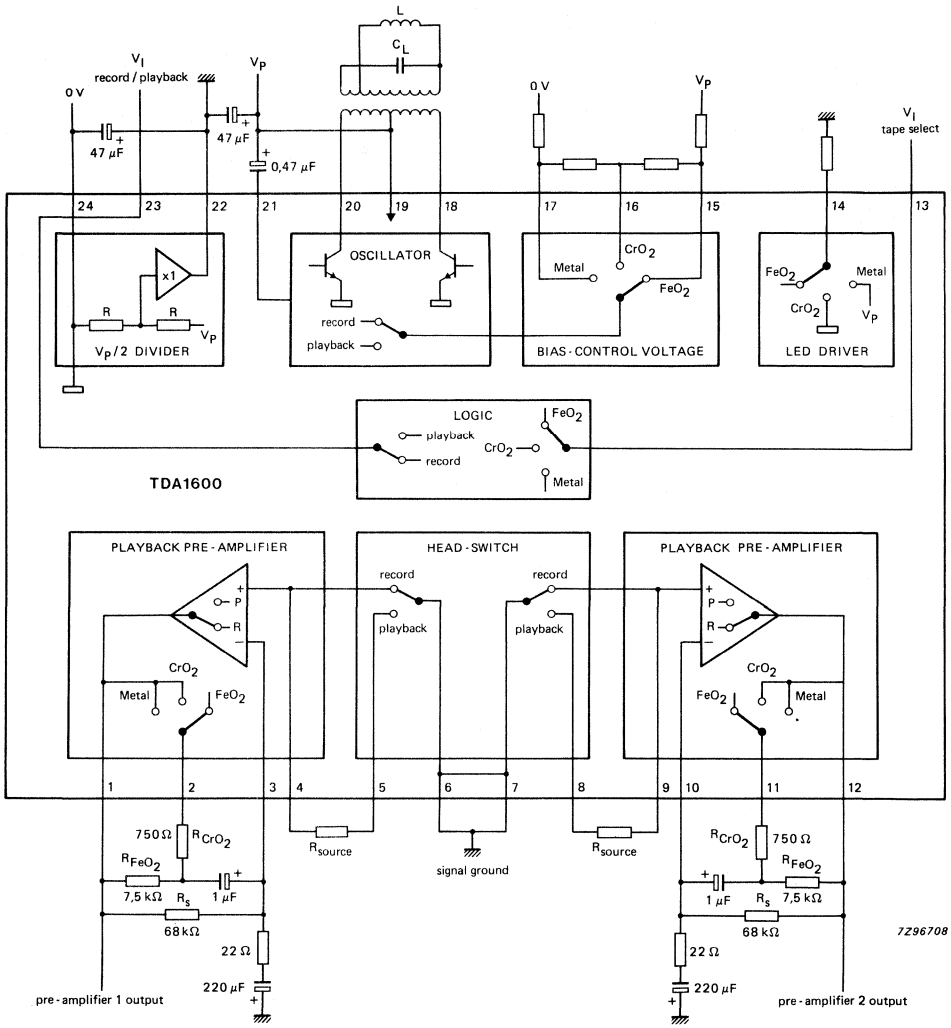


Fig. 6 Test circuit diagram.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

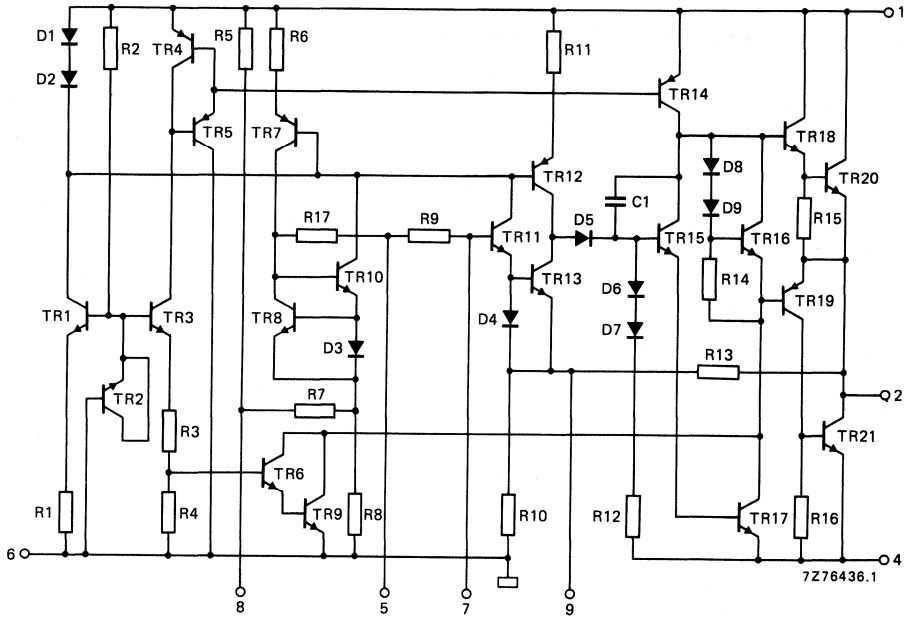


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C

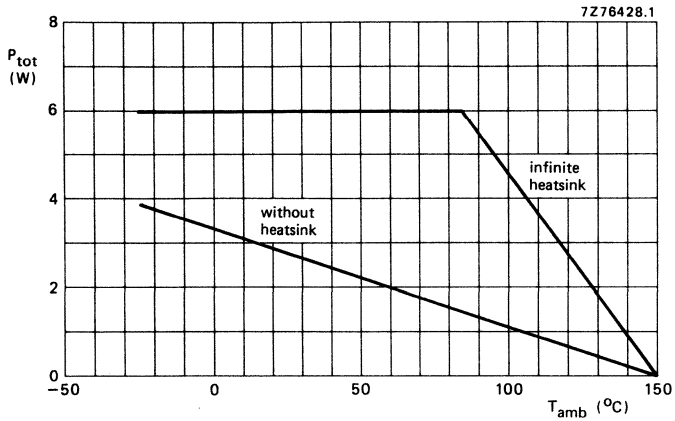


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

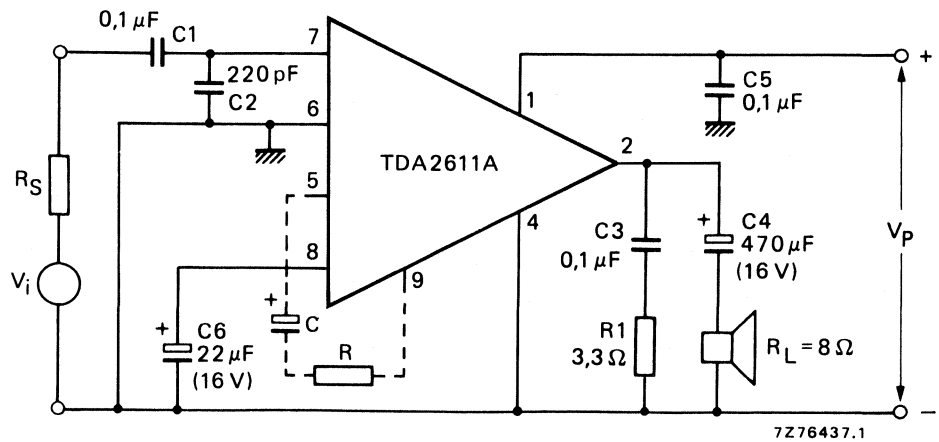


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

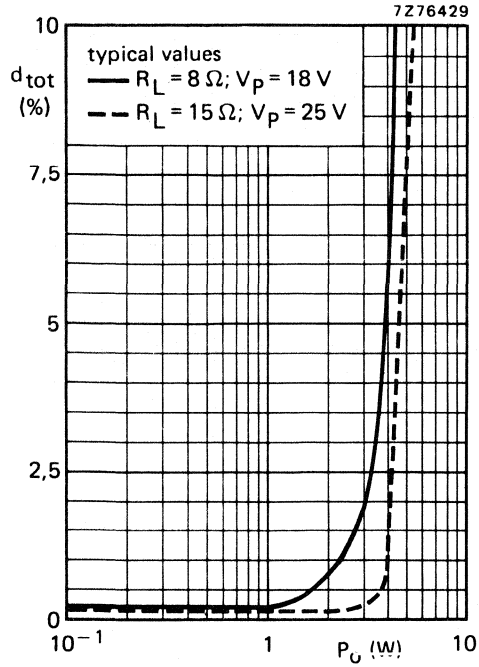


Fig. 4 Total harmonic distortion as a function of output power.

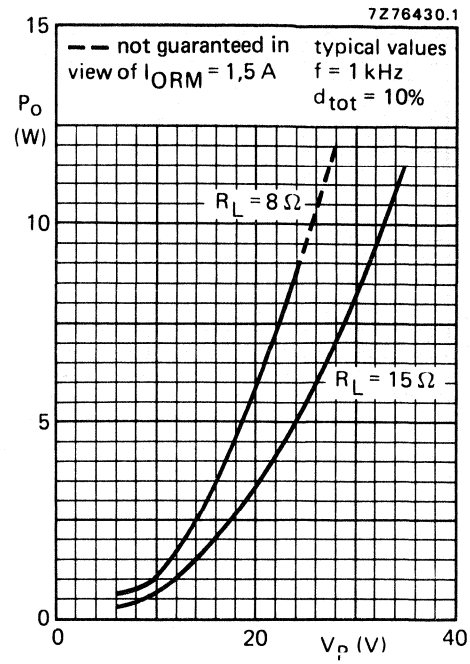


Fig. 5 Output power as a function of supply voltage.

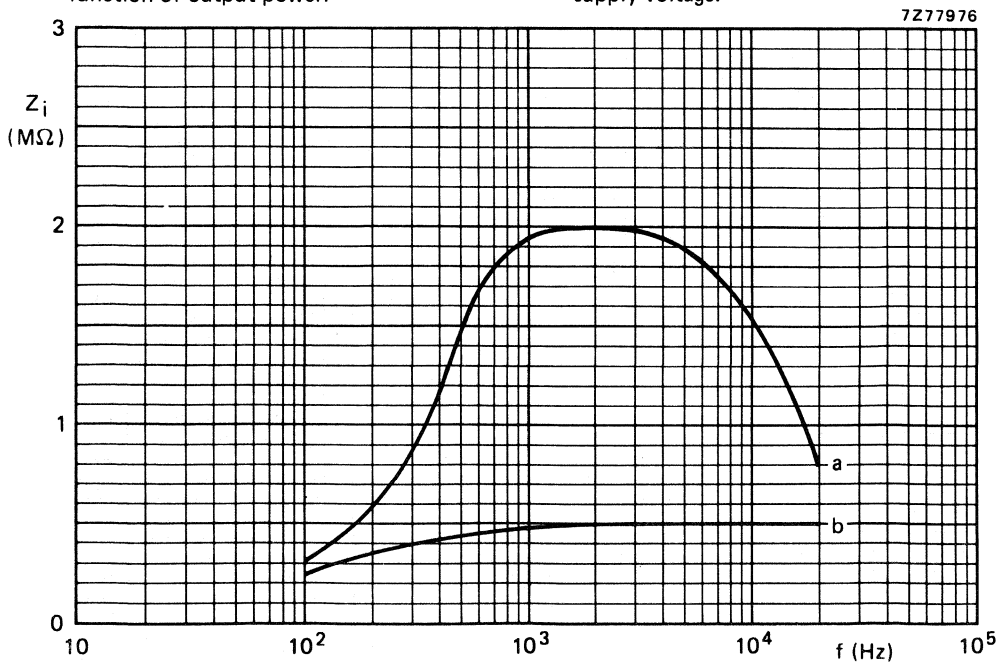


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

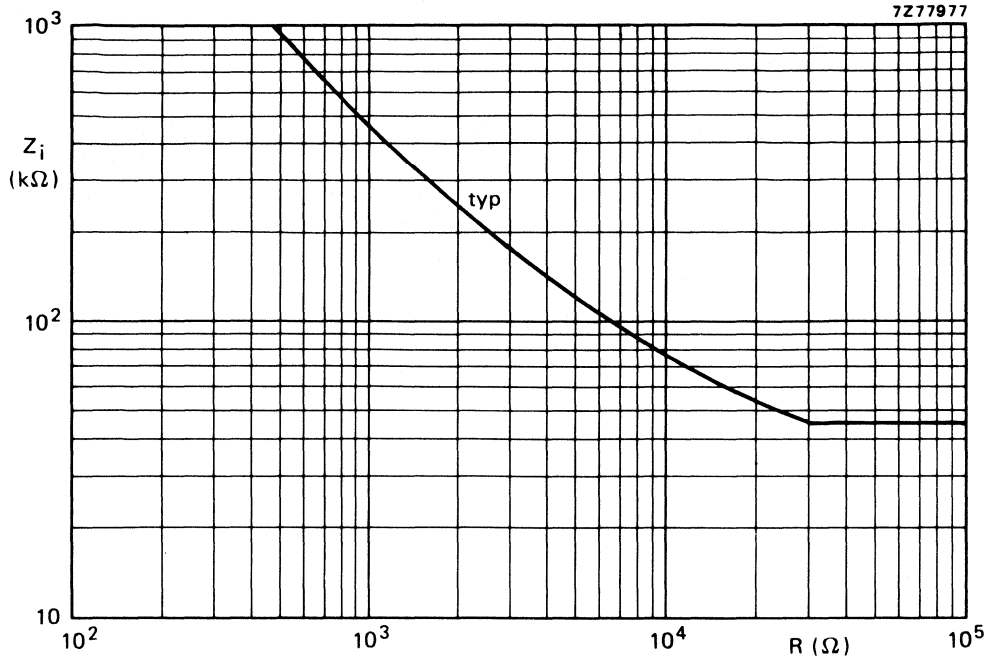


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

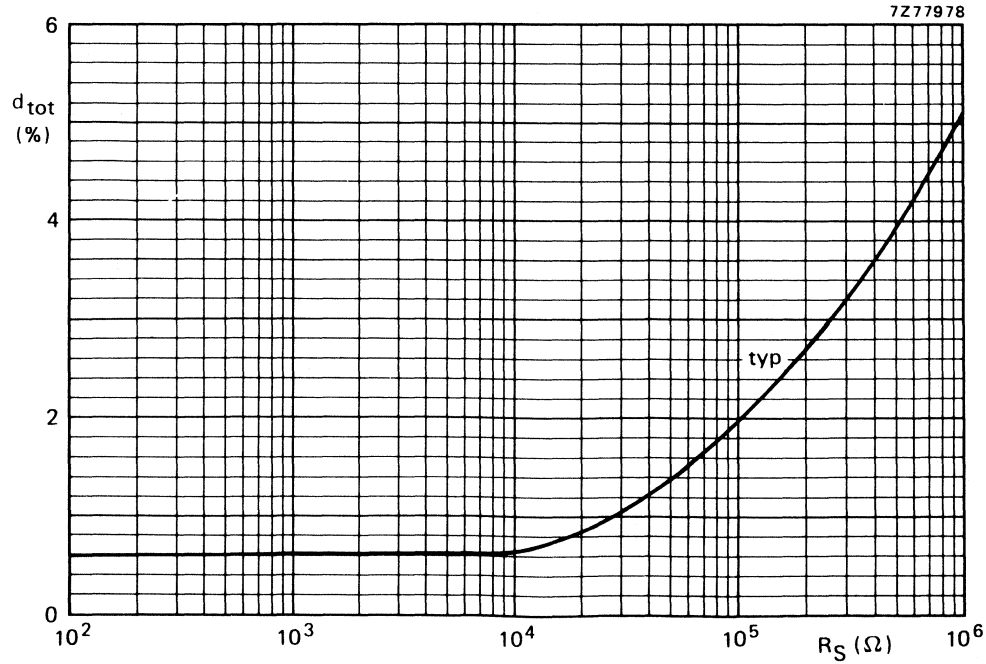


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

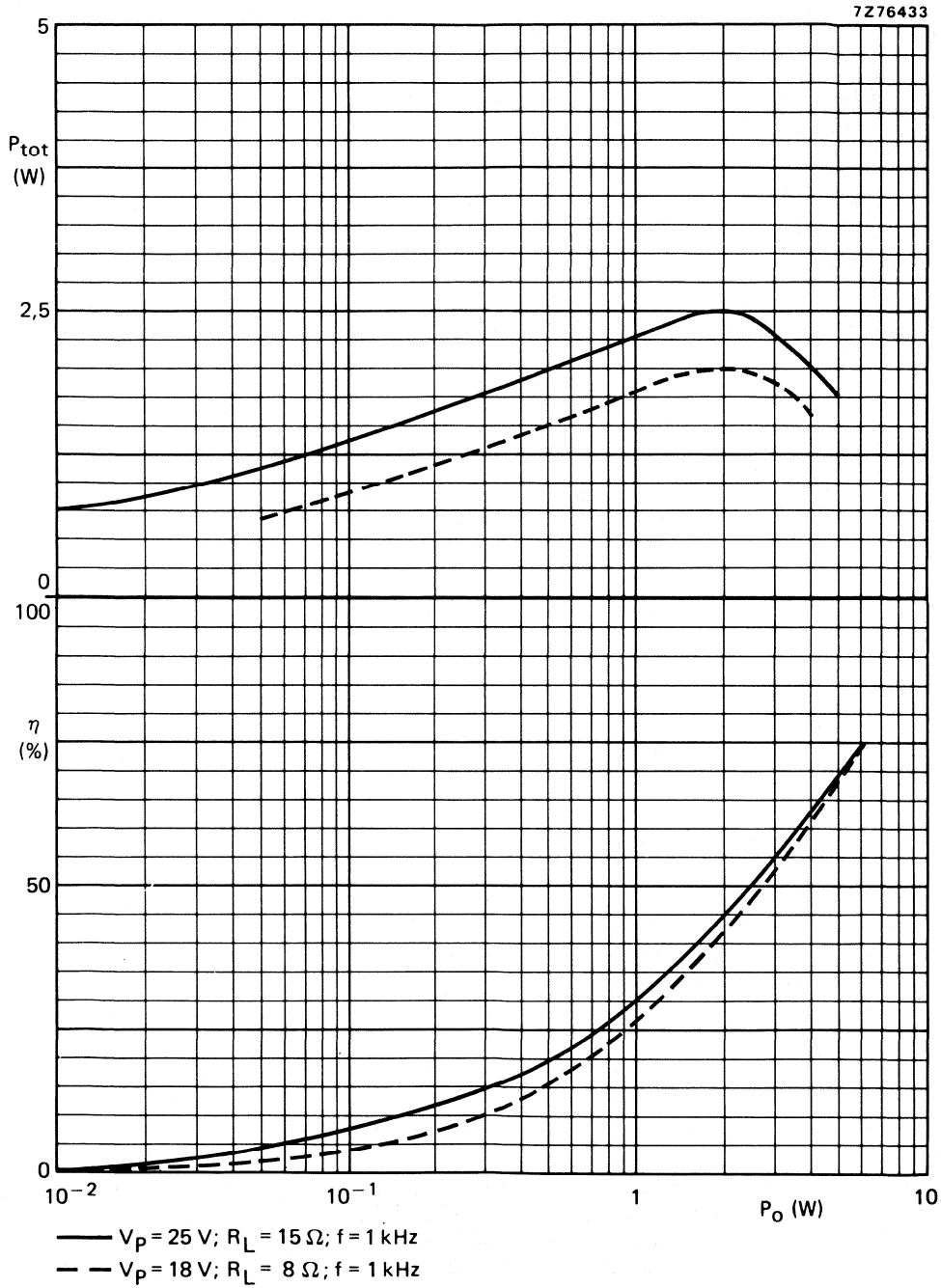


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

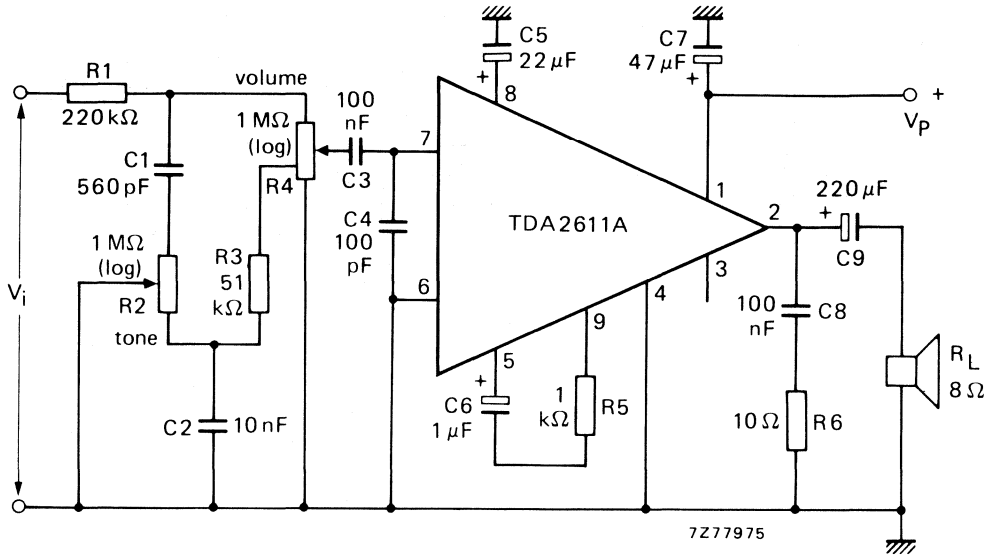


Fig. 10 Ceramic pickup amplifier circuit.

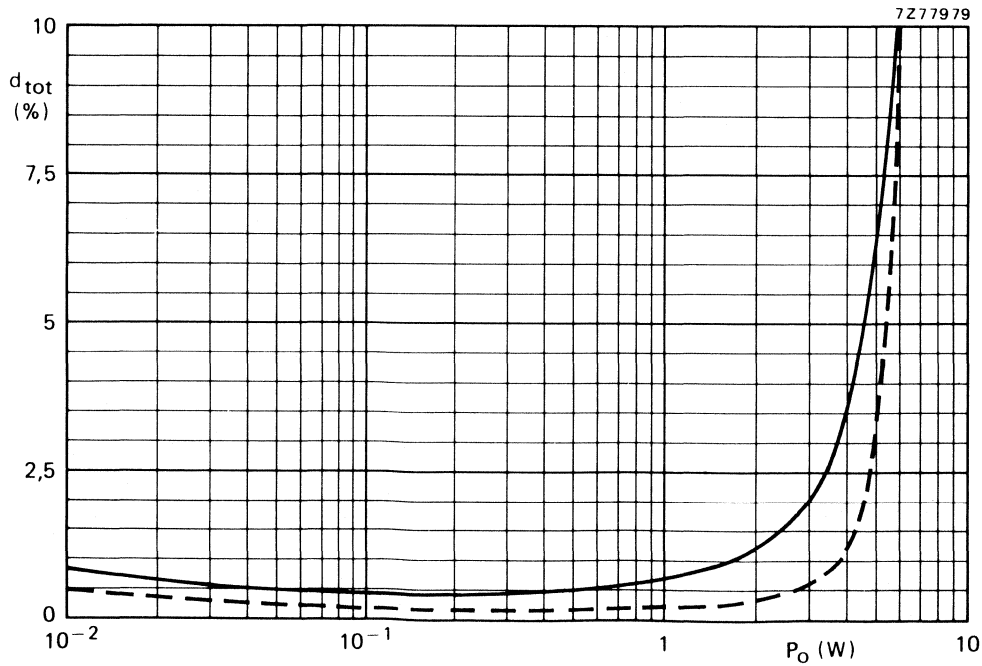


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

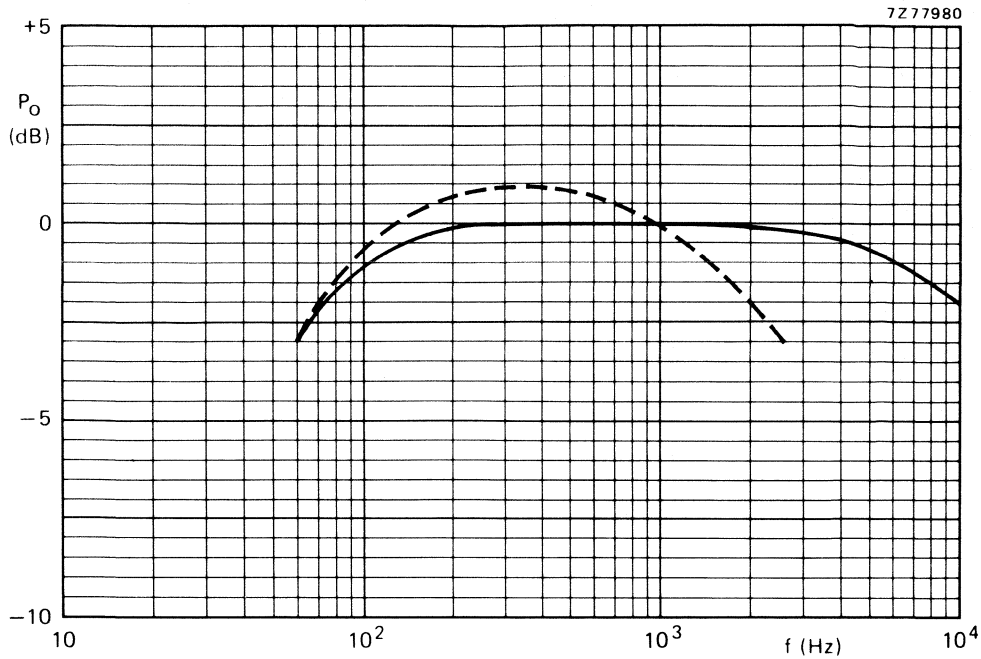


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

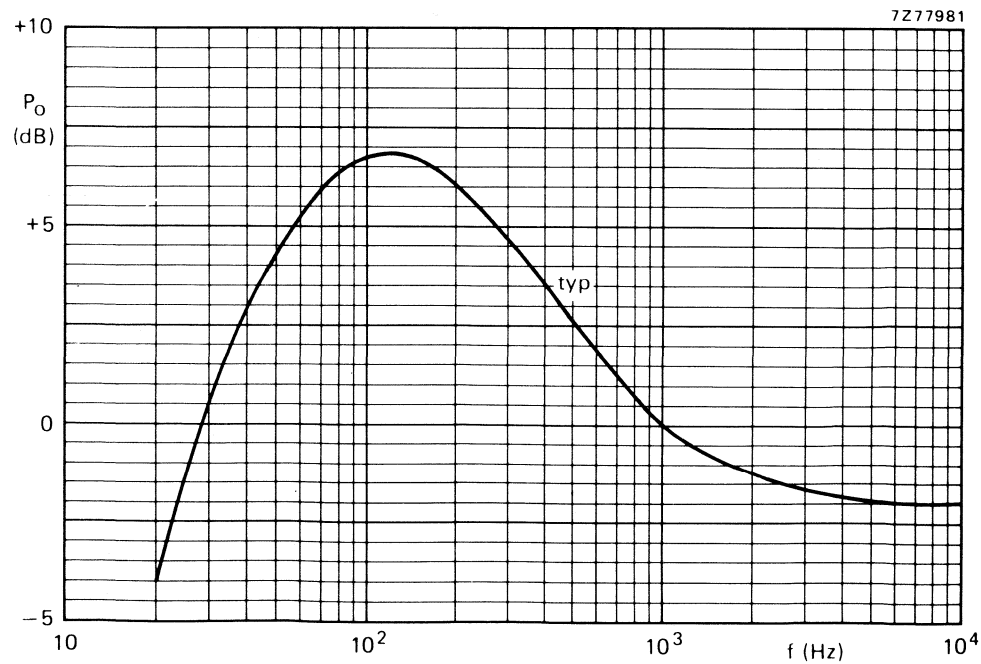


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_o	typ.	6 W
Voltage gain	G_v	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT-110B).

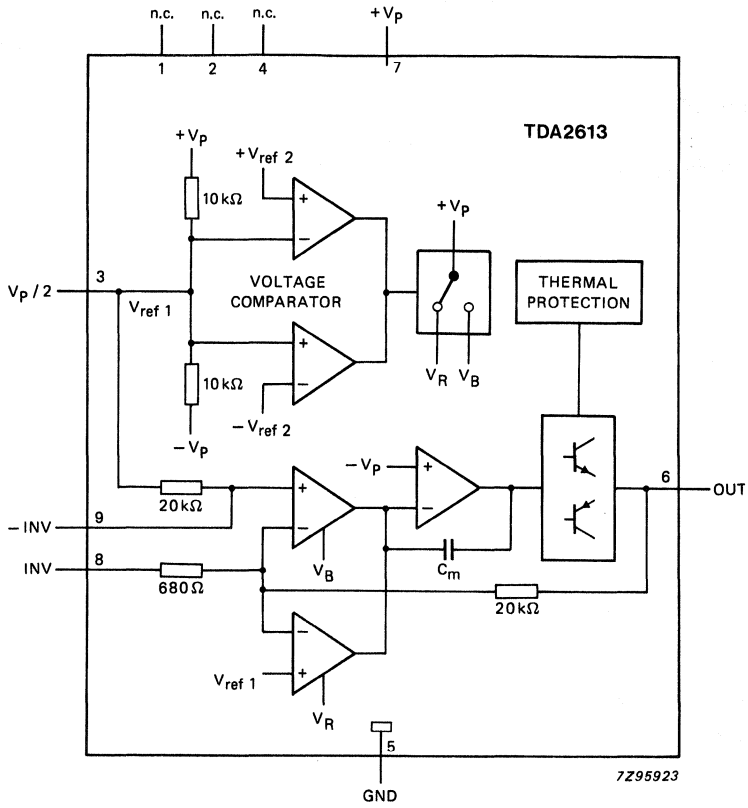


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected
2.	n.c.	not connected
3.	$V_P/2$	½ V_P (asymmetrical) ground (symmetrical)
4.	n.c.	not connected
5.	GND	ground (asymmetrical) negative supply (symmetrical)
6.	OUT	output
7.	+V_P	positive supply
8.	INV	inverting input
9.	−INV	non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	40	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) ⩾ 4 Ω, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to V_P = ± 20 V.

DEVELOPMENT DATA

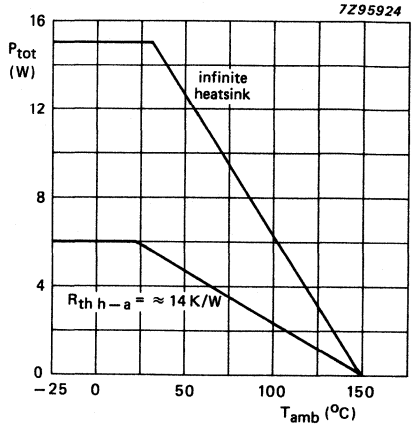


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case

$R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	40	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to $V_P/2$	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2$ kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

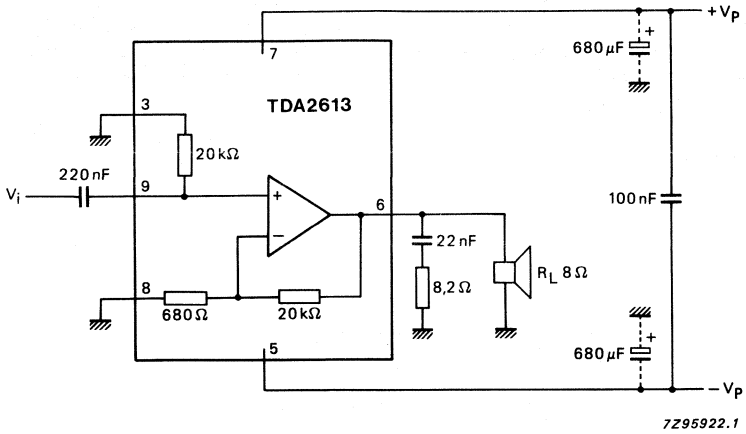


Fig. 3 Test and application circuit; symmetrical power supply.

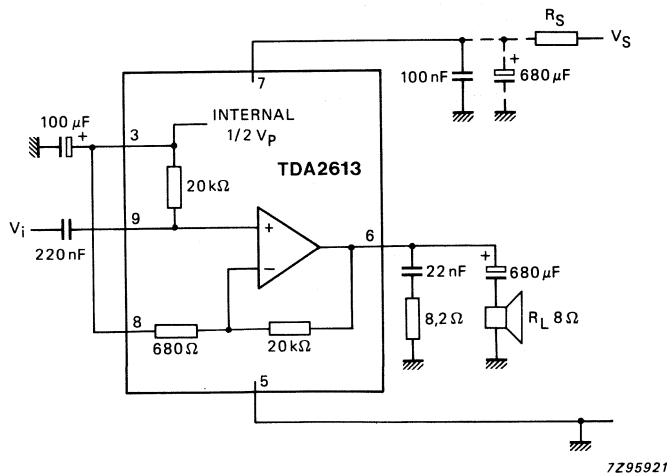


Fig. 4 Test and application circuit; asymmetrical power supply.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

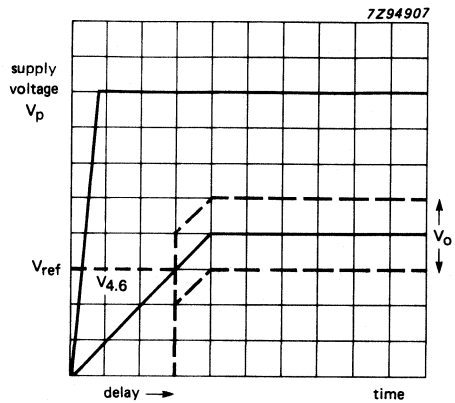


Fig. 5 Input mute circuit; time delay.

AUTOMATIC TUNING CIRCUIT

GENERAL DESCRIPTION

The TDA2614 is a monolithic integrated circuit for automatic tuning applications in TV and radio receivers.

Features

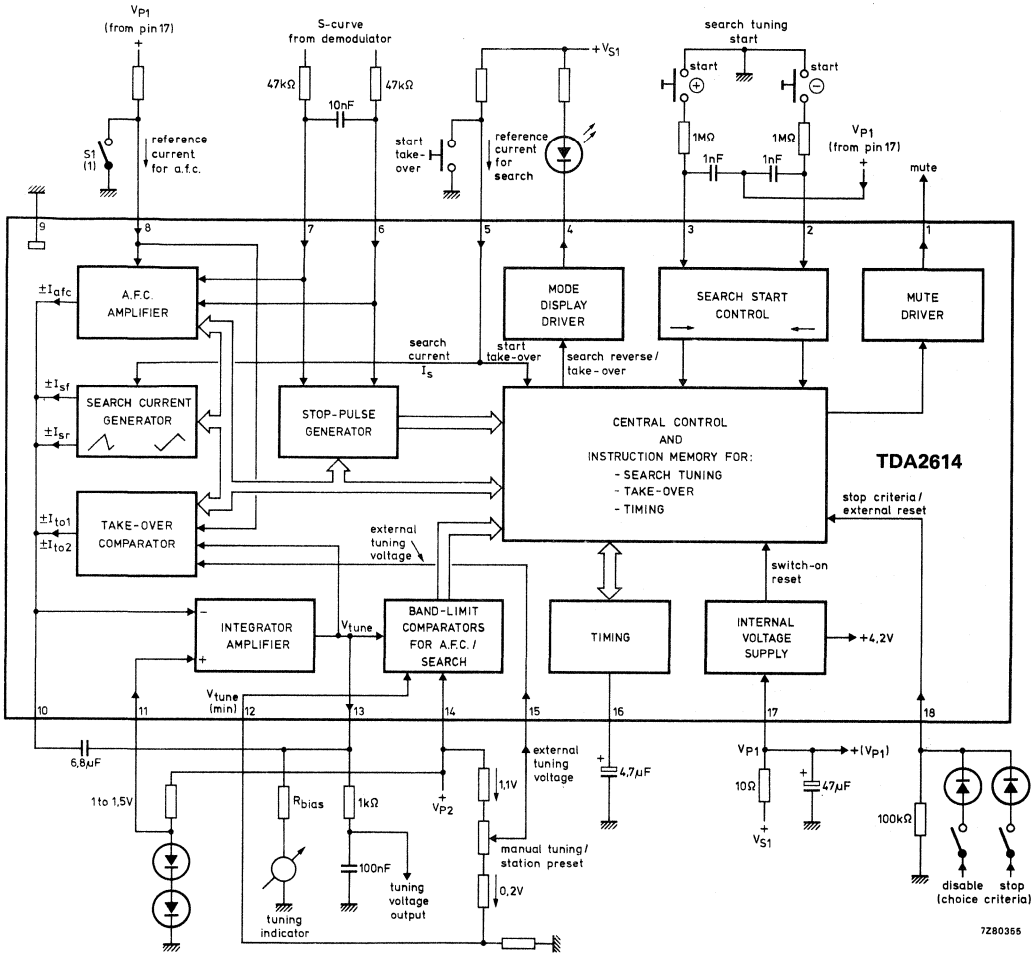
- Bi-directional search; sawtooth characteristic
- Stop-pulse generator (S-curve evaluation)
- Start/stop memory
- Internal control of timing and mute operation
- Take-over circuit for external station-presets
- Search tuning always starts from previous tuning position
- Integrating a.f.c.
- Integrator/amplifier for driving analogue displays
- Comparators for band limits
- Station select input (e.g. field-strength, stereo, traffic news, TV carrier)
- Adjustable a.f.c. and search-tuning characteristic
- Internal switch-on reset (preset station circuit take-over)

QUICK REFERENCE DATA

Supply voltages			
(pin 17)	V_{P1}	typ.	15 V
(pin 14)	V_{P2}	typ.	30 V
Supply currents (unloaded)			
(pin 17)	I_{P1}	typ.	10 mA
(pin 14)	I_{P2}	typ.	1,2 mA
Tuning voltage	$V_{13\text{-}9}$		0,5 to $V_{P2}-1$ V
Permissible load current (for display)	I_{13}	typ.	1,2 mA
Integrator current for search (adjustable)	$\pm I_{s10}$		20 to 200 μA
Integrator input current (a.f.c. off)	I_{o10}	typ.	10 nA
Input voltage range for the a.f.c. inputs	$V_{6;7\text{-}9}$		2,5 to $V_{P1}-1,4$ V
Supply voltage ranges			
(pin 17)	V_{P1}		6 to 24 V
(pin 14)	V_{P2}		6 to 33 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



(1) S1:

1 – A.F.C. OFF (search stand-by mode)
2 – Continuous take-over without muting (take-over stand-by mode)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)		V_{P1}	max.	24 V
Supply voltage (pin 14)		V_{P2}	max.	33 V
Voltages/currents				
Mute output (pin 1)		V_{1-9}	max.	33 V
		I_1	max.	10 mA
		$-V_{1-9}$	max.	0,5 V
	or:	$-I_1$	max.	10 mA
Start inputs (pins 2 and 3)		$V_{2;3-9}$	max.	V_{P1} + 0,5 V
	or:	$I_{2;3}$	max.	10 mA
		$-V_{2;3-9}$	max.	5 V
	or:	$-I_{2;3}$	max.	10 mA
Mode output (pin 4)		V_{4-9}	max.	33 V
		I_4	max.	50 mA
		$-V_{4-9}$	max.	0,5 V
	or:	$-I_4$	max.	10 mA
Search current/take-over control (pin 5)		V_{5-9}	max.	V_{P1} V
		$-V_{5-9}$	max.	0,5 V
	or:	$-I_5$	max.	10 mA
A.F.C. inputs (pins 6 and 7)		$V_{6;7-9}$	max.	V_{P1} V
		$\pm I_{6;7}$	max.	2 mA
		$-V_{6;7-9}$	max.	0,5 V
A.F.C. switch (pin 8)		V_{8-9}	max.	V_{P1} V
		I_8	max.	2 mA
		$-V_{8-9}$	max.	0,5 V
	or:	$-I_8$	max.	10 mA
Integrator input (pin 10)		V_{10-9}	max.	5 V
	or:	I_{10}	max.	10 mA
		$-V_{10-9}$	max.	0,5 V
	or:	$-I_{10}$	max.	10 mA
for $t < 1$ ms		$\pm V_{10-9}$	max.	30 V
		$\pm I_{10}$	max.	60 mA
Integrator bias (pin 11)		V_{11-9}	max.	10 V
		$-V_{11-9}$	max.	0,5 V
		$-I_{11}$	max.	5 mA
Band limiting (pin 12)		V_{12-9}	max.	14 V
		$-V_{12-9}$	max.	0,5 V
		$-I_{12}$	max.	10 mA
Integrator output (pin 13)		V_{13-9}	max.	V_{P2} V
		$-V_{13-9}$	max.	0 V

RATINGS (continued)

External tuning (pin 15)		V_{15-9}	max.	V_{P2}	V
		$-V_{15-9}$	max.	0,5	V
	or:	$-I_{15}$	max.	10	mA
Timing (pin 16)		V_{16-9}	max.	V_{P1}	V
		$-V_{16-9}$	max.	0,5	V
Station select input (pin 18)		V_{18-9}	max.	V_{P1}	V
		$-V_{18-9}$	max.	0,5	V
	or:	$-I_{18}$	max.	10	mA
Total power dissipation		P_{tot}	max.	800	mW
Storage temperature range		T_{stg}		−55 to + 150	°C
Operating ambient temperature range		T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr-a}$	=	80	K/W

CHARACTERISTICS

V_{P1} = 6 to 24 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply control section					
Supply voltage range (pin 17)	V_{P1}	6 (5)	–	24	V
Supply current (pin 17) at V_{P1} = 15 V	I_{P1}	–	10	20	mA
Supply tuning section					
Supply voltage range (pin 14)	V_{P2}	6	–	33	V
Supply current (pin 14) at V_{P2} = 30 V; without load at pin 13	I_{P2}	–	1,2	2	mA
Reset circuit (note 1)					
Input control voltage for reset	V_{18-9}	4,5	–	V_{P1}	V
A.F.C. amplifier					
Common-mode input voltage range	$V_{6;7-9}$	2,5	–	$V_{P1}-1,4$	V
Input bias current	$I_{6;7}$	–	0,2	0,5	μA
Input offset current	$I_{io6;7}$	–	–	0,2	μA
Input resistance	R_{6-7}	1	–	–	MΩ
Maximum a.f.c. output current	$\pm I_{afc10}$	–	$\frac{1}{120} \times I_8$	–	μA
at I_8 = 25 μA	$\pm I_{afc10}$	–	0,21	–	μA
A.F.C. input voltage for $I_{afc10} = 0,7 \times I_{afc10}$	V_{6-7}	–	100	–	mV
A.F.C. control input					
A.F.C. ON:					
permissible input current	I_8	15	–	500	μA
input voltage at I_8 = 25 μA	V_{8-9}	–	$V_{6;7-9}+0,6$	–	V
A.F.C. OFF (continuous take-over without muting); note 2:					
input voltage	V_{8-9}	0	–	$V_{6;7-9}$	V
reverse input current; V_{8-9} = 0 V	$-I_{i8}$	–	–	1	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Integrator amplifier (note 3)					
Required input bias voltage					
pin 11	$V_{11\text{-}9}$	1	–	1,5	V
pin 10	$V_{10\text{-}9}$	–	$V_{11\text{-}9}$	–	V
Input bias currents					
pin 11; at $V_{11\text{-}9}$ = 1,2 V	I_{11}	–	2	–	μA
pin 10; for search stand-by; A.F.C. OFF	$\pm I_{10}$	–	10	100	nA
Output voltage range with load; $\pm I_{13}$ = 1,2 mA	$V_{13\text{-}9}$	0,5	–	$V_{14\text{-}9}-1$	V
Available output current (t < 1 ms) peak value	$\pm I_{o13m}$	–	10	–	mA
Noise output voltage (peak value) (f = 20 Hz to 20 kHz) weighted to DIN45405; R_L = 1 kΩ in series with C_L = 0,1 μF	V_{no13m}	–	5	–	μV
Station search circuit (note 4)					
Start inputs (pins 2 and 3)					
Input bias voltage	V_i	–	$V_{P1}-0,2$	–	V
Input threshold voltage for "search start"	V_{is}	$V_{P1}-2,3$	$V_{P1}-1,8$	$V_{P1}-0,8$	V
Input control current for "search start"	$-I_{is}$	0,2	0,5	1	μA
Input short-circuit current					
at V_{P1} = 20 V	$-I_{i\,sc}$	–	0,7	–	μA
at V_{P1} = 6 V	$-I_{i\,sc}$	–	0,4	–	μA
Required voltage difference for defined direction of search mode	$\pm \Delta V_{2\text{-}3}$	300	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Search-current generator (note 5)					
Permissible input current range	I_5	20	–	200	μA
Input voltage at "search stand-by"	V_{5-9}	–	0,7	–	V
	or:	–	$V_{BE}+R_{i5}xI_5$	–	V
Input voltage at "search active"	V_{5-9}	–	1,5	–	V
	or:	–	$2V_{BE}+R_{i5}xI_5$	–	V
Input resistance	R_{i5}	–	2,5	–	kΩ
Output current at pin 10					
at search forward	$\pm I_{sf10}$	$0,65I_5$	I_5	$1,35I_5$	μA
at search reverse	$\pm I_{sr10}$	–	$I_{sr\,int}+I_{sf10}$	–	μA
	$I_{sr\,int}$	170	330	540	μA
	or:	–	$4V_{BE}/8,3$ kΩ	–	mA
Stop-pulse generation (note 6)					
Input threshold levels					
for "stop preparation"	$\pm V_{6-7}$	100	160	200	mV
for "stop release"; $I_{sf10} = 0$; note 7	$\pm V_{6-7}$	–	0	30	mV
Stop-criteria (external reset) (note 8)					
Desired tuning position from "search start" to "search stop"					
required input voltage	V_{18-9}	0	–	450	mV
or input open circuit	I_{18}	–	–	0,1	μA
Non-desired tuning position search re-started					
required input voltage	V_{18-9}	1	–	2,5	V
or input control current	I_{18}	20	–	125	μA
Reset to "search stand-by"					
required input voltage	V_{18-9}	4,5	–	V_{P1}	V
or input control current	I_{18}	0,7	–	–	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Band-limit comparators (note 9)					
Lower-band limit					
Permissible input voltage range	V_{12-9}	–	0,5	$V_{P2}-4$	V
Input current	$-I_{12}$	–	0,5	2	μA
Lower switching threshold level	V_{13-9}	$V_{12-9}+0,18$	$V_{12-9}+0,2$	$V_{12-9}+0,22$	V
Upper-band limit					
Permissible input voltage range	V_{14-9}	6	–	33	V
Upper switching threshold level	V_{13-9}	$V_{P2}-1,25$	$V_{P2}-1,1$	$V_{P2}-1$	V
Take-over circuit (note 10)					
Take-over start inputs					
Input voltage (note 11)					
for "search stand-by"	V_{5-9}	–	0,7	–	V
for "search active"	V_{5-9}	–	1,5	–	V
Required control voltage for "start take-over"	V_{sto5-9}	–	–	0,35	V
or control current for "start take-over"	I_{sto5}	–	–	1	μA
Continuous take-over e.g. a.f.c. OFF; note 12					
Required control voltage for "continuous take-over"; a.f.c. OFF	V_{8-9}	–	–	$V_{6;7-9}$	V
Reverse input current; $V_{8-9} = 0$	$-I_8$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Take-over comparator					
Input voltage range	$V_{15\text{-}9}$	0,5	–	$V_{P2}-1$	V
Input bias current	$-I_{15}$	–	0,2	1	μA
Input offset voltage $I_{to1} = I_{to2} = 0$ (note 13)	$V_{io15\text{-}13}$	–	3	10	mV
Output current at $\pm V_{13\text{-}15} > 200$ mV					
at "take-over active"	$\pm I_{to1(10)}$	–	500	–	μA
at "continuous take-over"	$\pm I_{to2(10)}$	–	40	–	μA
De-tuning slope at pin 10 for $\pm V_{13\text{-}15} < 50$ mV					
at "take-over active"	S_{to1}	–	4	–	mS
at "continuous take-over"	S_{to2}	–	0,5	–	mS
Threshold voltage for start-timing at "take-over active"	$\pm\Delta V_{13\text{-}15}$	–	50	–	mV
Timing circuit					
Bias voltage	$V_{16\text{-}9}$	–	4,2	–	V
Internal discharge resistance (internally switched)	$R_{i'16\text{-}9}$	0,7	1	1,3	kΩ
Charge current (switched)					
slow	$-I_{16(1)}$	6	9	12	μA
fast	$-I_{16(2)}$	95	150	195	μA
Internal switching thresholds					
lower threshold voltage	$V_{16\text{-}9(1)}$	–	1	–	V
upper threshold voltage	$V_{16\text{-}9(2)}$	–	3,8	–	V
Mute-driver (open collector)					
Output voltage					
LOW level (conducting)		mute active			
HIGH level (non-conducting)		mute in-active			
Output saturation voltage at $I_1 = 2$ mA	$V_{1\text{-}9sat}$	–	–	0,5	V
Output leakage current at $V_{1\text{-}9} = 20$ V	I_1	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Mode-driver					
Output voltage					
LOW level (conducting)		search forward or search stand-by mode			
HIGH level (non-conducting)		search reverse mode or take-over active mode or take-over stand-by mode			
Output saturation voltage at I_4 = 25 mA	$V_{4\text{-}9sat}$	–	–	0,8	V
Reverse output current at $V_{4\text{-}9}$ = 20 V	I_4	–	–	1	μA
Switch-on reset (note 14)					
Reset threshold voltage	$V_{17\text{-}9}$	2	–	4	V

Notes to the characteristics

1. The a.f.c. circuit is operational during the "take-over stand-by" mode as well as during the "search stand-by" mode. The latter is set automatically after "search start" and a station is been found (see also note 4).
   In addition, this mode can be selected by activating the reset via pin 18. The "take-over stand-by" mode is set automatically after "start take-over" and an external tuning voltage applied at pin 15 is taken over (see also note 10).
   The a.f.c. output current is controlled to zero by the band limit comparators, when the tuning voltage range limit is reached (see also note 9).
2. The "continuous take-over without muting" mode is only set during a.f.c. OFF, in the "take-over stand-by" mode.
3. The inputs of the integrator amplifier are protected against over-load by internal clamping diodes, enabling a charged storage capacitor to be directly connected.
   Also, the response of the protection circuit will increase the slew-rate of the amplifier, so that the loss of charge when connecting the capacitor is decreased (see Fig. 4).
4. Station search-tuning circuit
   start instruction + (pin 3): the tuning voltage will go positive ($+I_{10}$)
   start instruction – (pin 2): the tuning voltage will go negative ($-I_{10}$).

   The start instruction is internally stored and therefore continuous operation is not necessary. So, the automatically activated variation of the tuning voltage (search) is terminated when the station is found, and a control voltage appears at the a.f.c. inputs (stop-pulse generation).
   This results in analizing the level at pin 18 (station select input for field-strength, stereo, traffic news, TV-carrier etc.) which is controlled by the timing circuit. If $V_{18\text{-}9} < 0{,}45$ V (desired station) the start memory is reset (search stand-by mode) and the tuning voltage will be controlled by the a.f.c. If $V_{18\text{-}9}$ = 1 to 2,5 V (non-desired station) the search-current generator is re-activated, until the next stop pulse appears.

When the tuning voltage range limit is reached (band-limit comparators), a fast "search reverse" follows automatically, during which a "search stop" is impossible. After reaching the other tuning voltage limit, the search is reset in the originally selected direction.

The "take-over active" mode has priority and stops the search tuning. For all the various operation modes, signals are available at the outputs pin 4 (mode display) and pin 1 (muting).
If a start instruction is operated continuously, the circuit operates in a scan-mode, i.e. after having stopped at a desired station a restart appears automatically after about 1,5 seconds.

5. The search tuning speed depends on the value of $C_{10\text{-}13}$ and the reference current I_5.
6. The circuit is only active for search forward in the "search a tive" mode.
7. The signal sequence "search/stop-release" is only possible if before the search-direction choice was made (positive or negative), the threshold voltage for "stop preparation" was passed (see Fig. 8). For more data of pins 6 and 7, see item a.f.c. amplifier.
8. The circuit responds to pin 18 only in the "search active" mode at the end of the analizing time; the timing circuit determines the required analizing time once the "stop-release" threshold is established (see Fig. 8). The circuit responds immediately and independently of the mode to a reset instruction.
9. The circuit limits the tuning voltage at pin 13 to the preset values at pin 12 (lower limit) and pin 14 (upper limit).

   Switching from search forward to reverse and back to forward is obtained automatically during "search active".

   During "a.f.c. ON" the values are limited to those preset (given under item band-limiter comparators).
10. The take-over circuit controls the tuning voltage to a value of an external reference voltage derived from pin 15. There are two operation modes possible.

    a. Tuning by station-selection switches with muting.

       The reference voltage from an external station memory (tuning potentiometer, electronic analogue memory e.g. D/A converter) is applied to pin 15. With the additional start instruction at pin 5 "start take-over" (e.g. mute contact of a tuning potentiometer module) the take-over circuit will be activated. The "start take-over" instruction will be internally stored. The take-over follows as an automatic control process of both the take-over comparator and the timing circuit. After terminating the tuning ($V_{13} = V_{15}$) the circuit returns to the "take-over stand-by" mode ($I_{to1} = I_{to2} = 0$) and the tuning voltage is applied by the a.f.c. circuit. If operation is re-activated from e.g. "search start", the circuit commences its search from the previous set tuning voltage. During changing the tuning voltage the mute output (pin 1) is active.

    b. Manual tuning without muting

       This operation mode is only possible during the "take-over stand-by" mode.
       For manual tuning with the tuning potentiometer it is necessary that the tuning voltage continuously follows the reference voltage at pin 15.
       To achieve this, pin 8 has to be grounded (a.f.c. OFF). The mute output (pin 1) is non-active.
11. See also items under "station search-tuning circuit".
12. For example during manual tuning.
13. I_{to1} is the fast and I_{to2} is the slow take-over current.
14. When the supply voltage V_{P1} (at pin 17) is switched on the circuit is set in the "take-over active" mode. This operation mode corresponds to the instruction "take-over" at pin 5.

Table 1 Operating modes

ref. no.	search tuning			take-over		timing			outputs		input	tuning currents (pin 10)					remarks
	stand-by	active		stand-by	active	stand-by	active		mode	mute	a.f.c.						
		forward	reverse				0,1 s	1,5 s	pin 4	pin 1	pin 8	I_{afc}	I_{sf}	I_{sr}	I_{tol}	I_{to2}	
1	+					+			0	1	0	0	0	0	0	0	
2	+					+			0	1	1	1	0	0	0	0	• listen
3		+				+			0	0	0	0	1	0	0	0	
4		+				+			0	0	1	1	1	0	0	0	• search tuning
5		+					+		0	0	0	0	0	0	0	0	
6		+					+		0	0	1	1	1	0	0	0	• evaluation
7		+						+	0	1	0	0	0	0	0	0	
8		+						+	0	1	1	1	0	0	0	0	• listen (scan)
9			+			+			1	0	X	0	0	1	0	0	• reverse
10				+		+			1	1	0	0	0	0	1	0	• continuous take-over (no muting)*
11				+		+			1	1	1	1	0	0	0	0	• listen
12					+	+			1	0	X	0	0	0	1	1	take-over (mute)
13					+		+		1	0	0	0	0	0	1	0	
14					+		+		1	0	1	1	0	0	1	0	take-over (mute)

+ corresponds to instantaneous mode of operation

1 = high-ohmic
0 = conducting

0 = current not released
1 = current released
X = don't care

* For example during manual tuning.

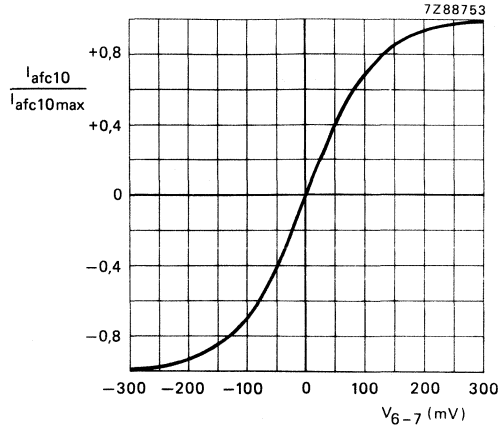


Fig. 2 A.F.C. control curve.

$$I_{afc10} = \left\{ \frac{2}{e^{-\frac{V_{6-7}}{2V_T}} + 1} \right\} \times \frac{I_8}{120} \qquad I_8 = \frac{V_{P1} - V_{8-9}}{R_{8-17} + 10\ k\Omega}$$

$$V_T = \frac{kxT}{q} = 28\ mV\ (at\ T_j = 330\ K)$$

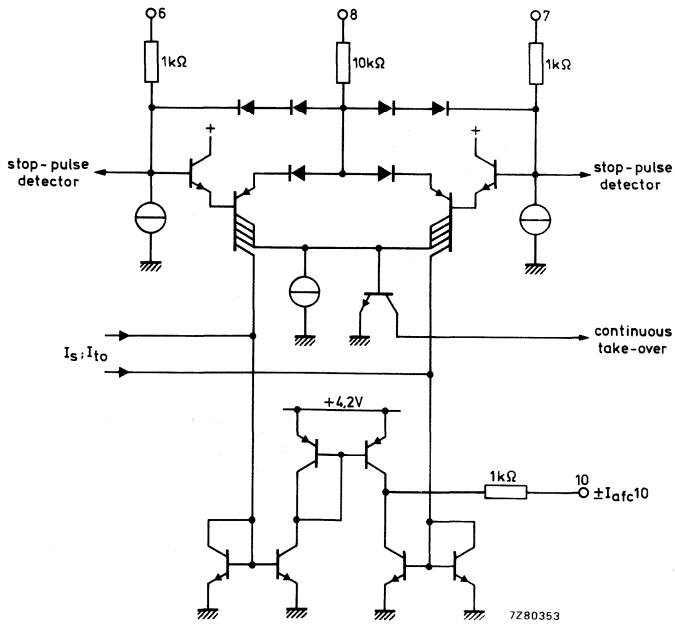


Fig. 3 A.F.C. amplifier (schematic).

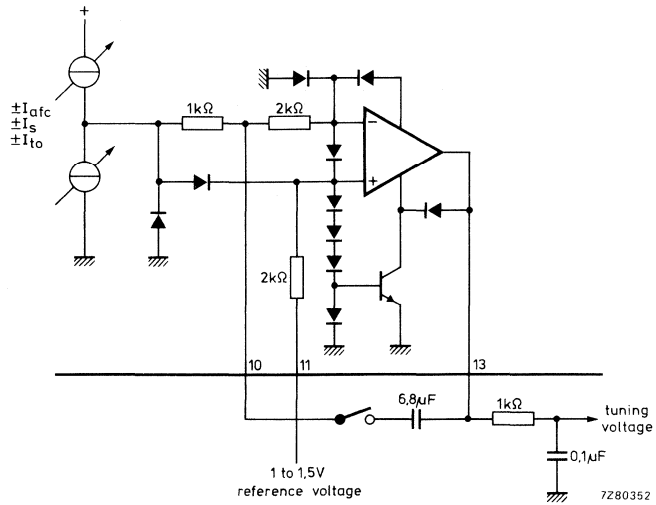
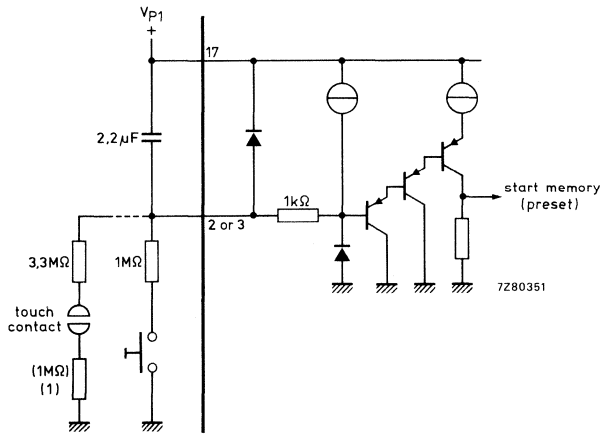


Fig. 4 Integrator with switch-on clamping circuit (schematic).



(1) In case the mains supply cannot be disconnected.

Fig. 5 Search-tuning start inputs (schematic).

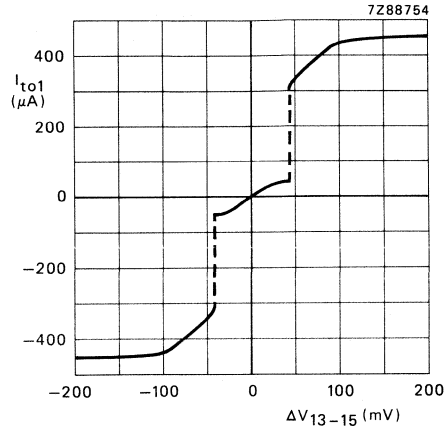


Fig. 6 Take-over current (I_{to10}) as a function of the voltage variation at pin 13 (ΔV_{13-15}) at tuning to external station memory (external presets).

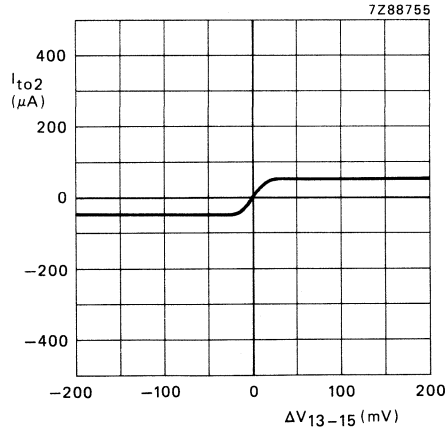
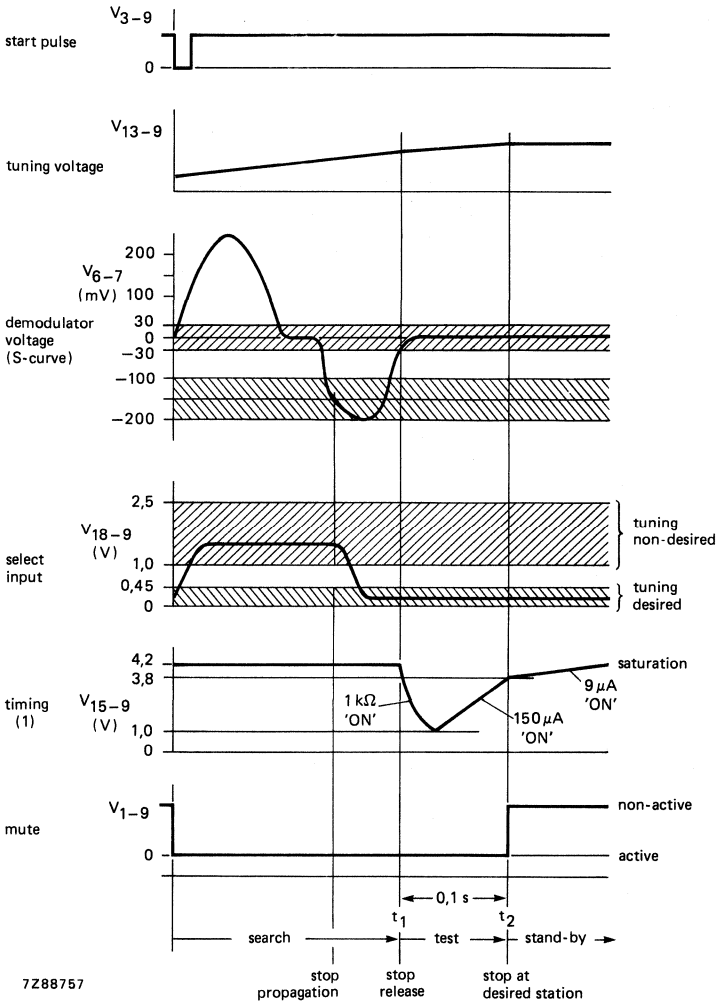


Fig. 7 Take-over current (I_{to10}) as a function of the voltage variation at pin 13 (ΔV_{13-15}) at continuous take-over (e.g. manual tuning).



(1) The timing is obtained by using the circuit below.

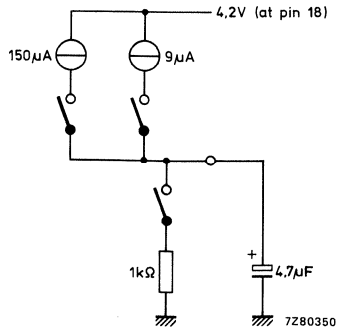


Fig. 8 Timing diagram for search tuning after "search start" instruction (+).

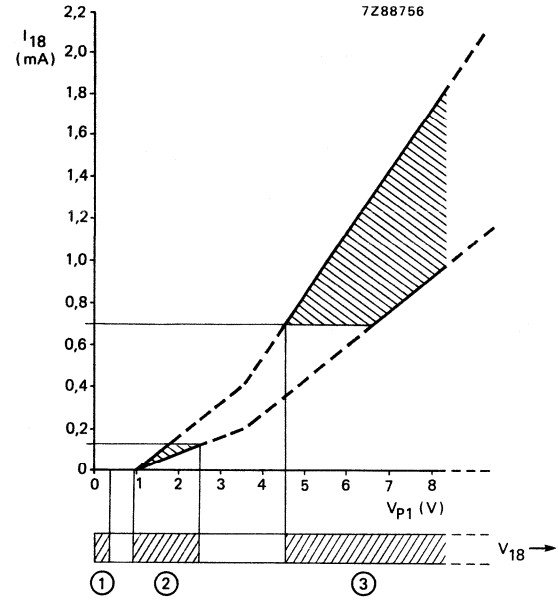


Fig. 9 Stop criteria:

operating range (1) = desired tuning position
operating range (2) = non-desired tuning position
operating range (3) = reset to "search stand-by mode".

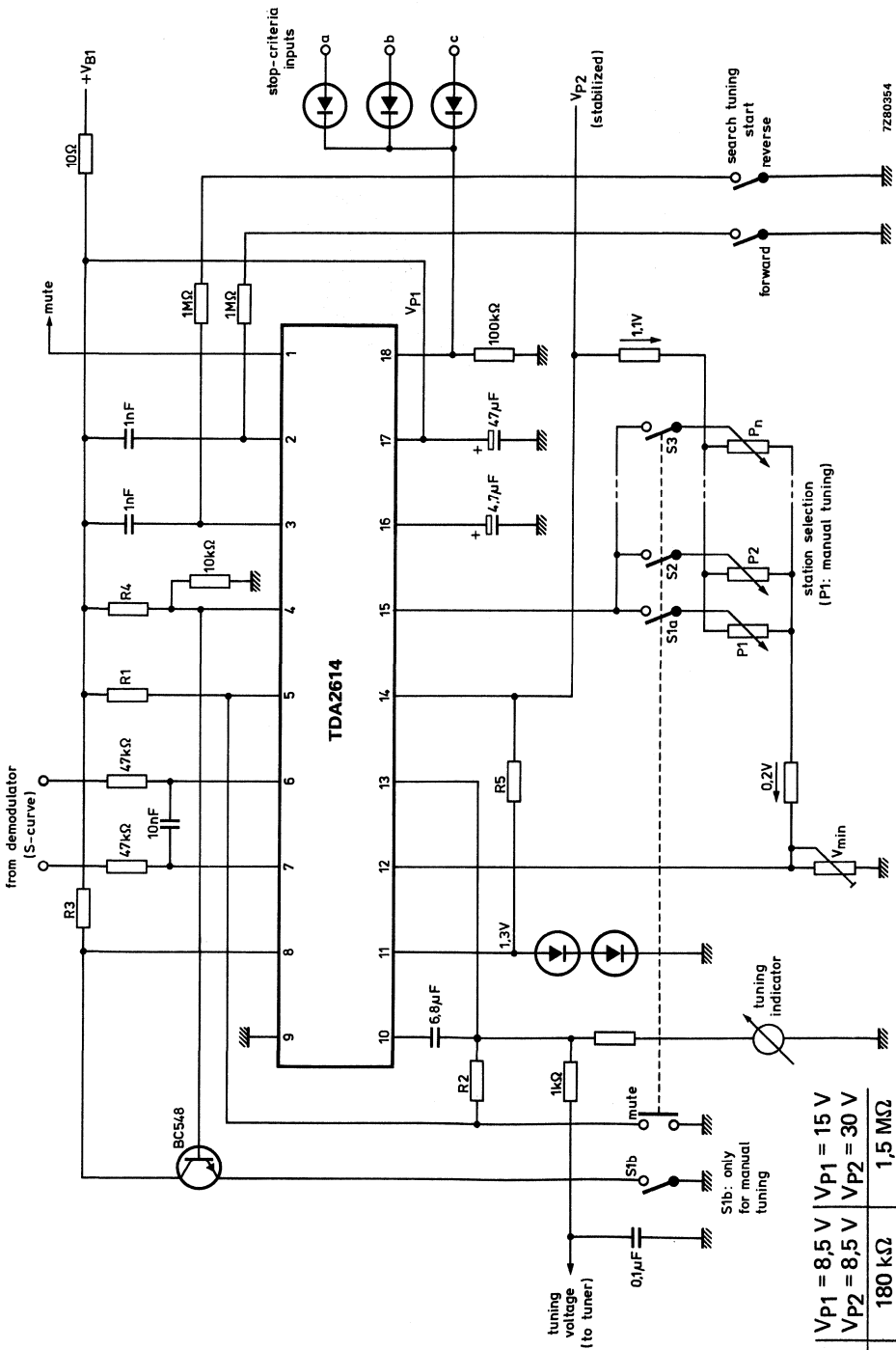


Fig. 10 Application circuit diagram.

	VP1 = 8,5 V VP2 = 8,5 V	VP1 = 15 V VP2 = 30 V
R1	180 kΩ	1,5 MΩ
R2	82 kΩ	150 kΩ
R3	220 kΩ	390 kΩ
R4	47 kΩ	100 kΩ
R5	68 kΩ	150 kΩ

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.
The difference between the TDA3047 and TDA3048 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

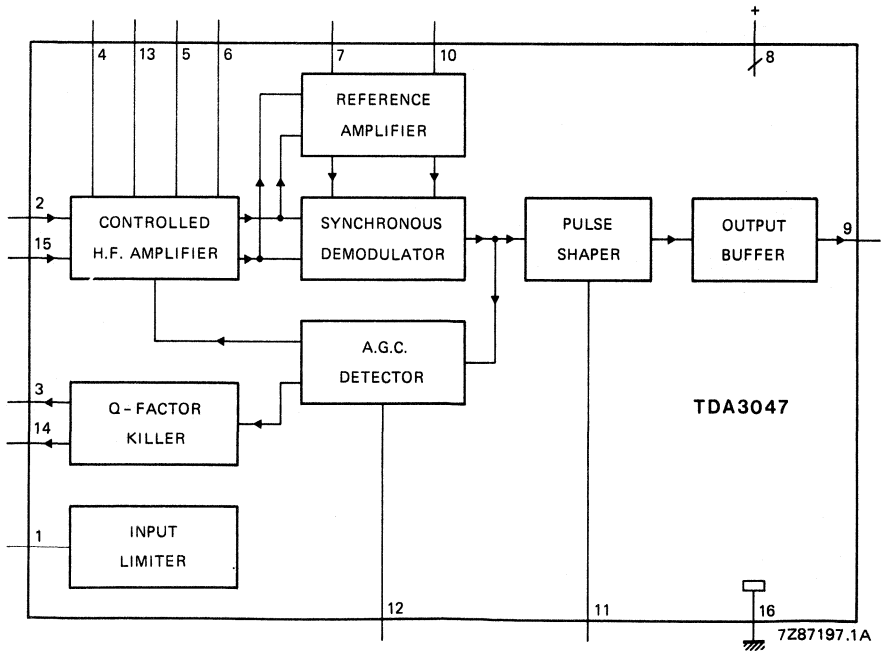


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINES

TDA3047P: 16-lead DIL; plastic (SOT38).
TDA3047T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *high*					
at $V_{9-16} = 4{,}5$ V	$-I_9$	75	120	–	μA
at $V_{9-16} = 3{,}0$ V	$-I_9$	75	130	–	μA
at $V_{9-16} = 1{,}0$ V	$-I_9$	75	140	–	μA
Output current; output voltage *low*					
at $V_{9-16} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2,5	7,5	20	μA

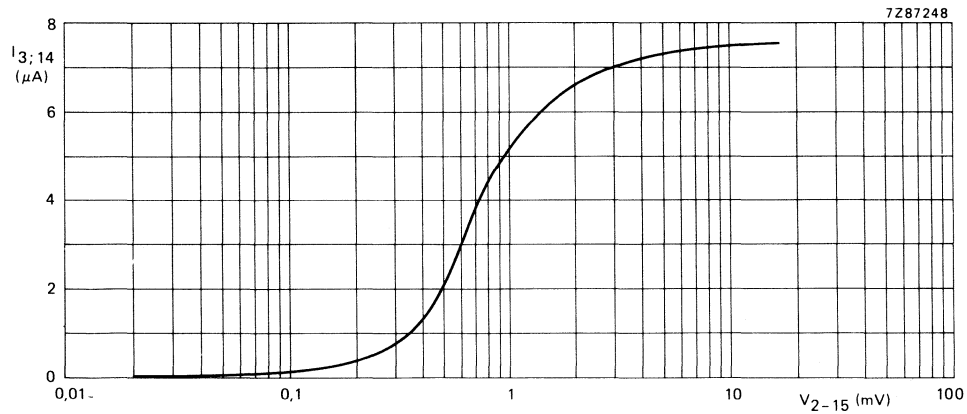
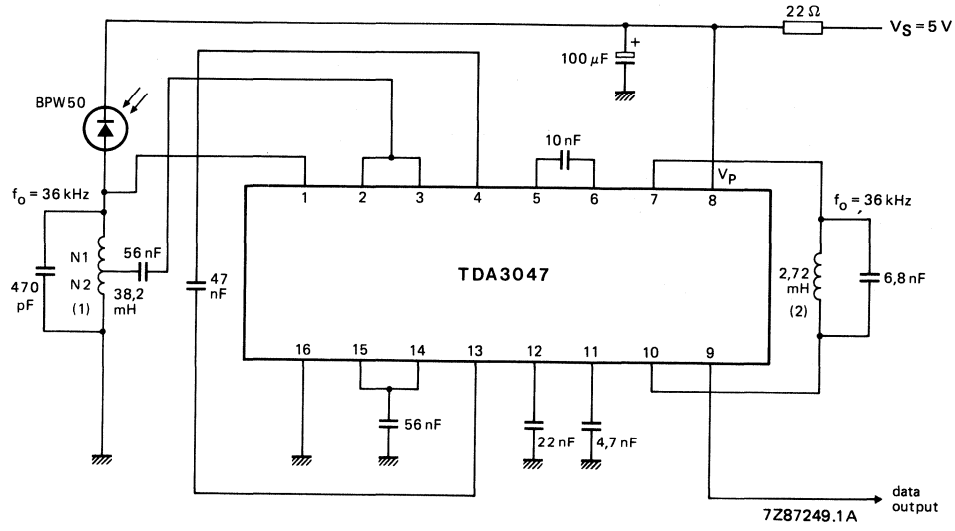


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

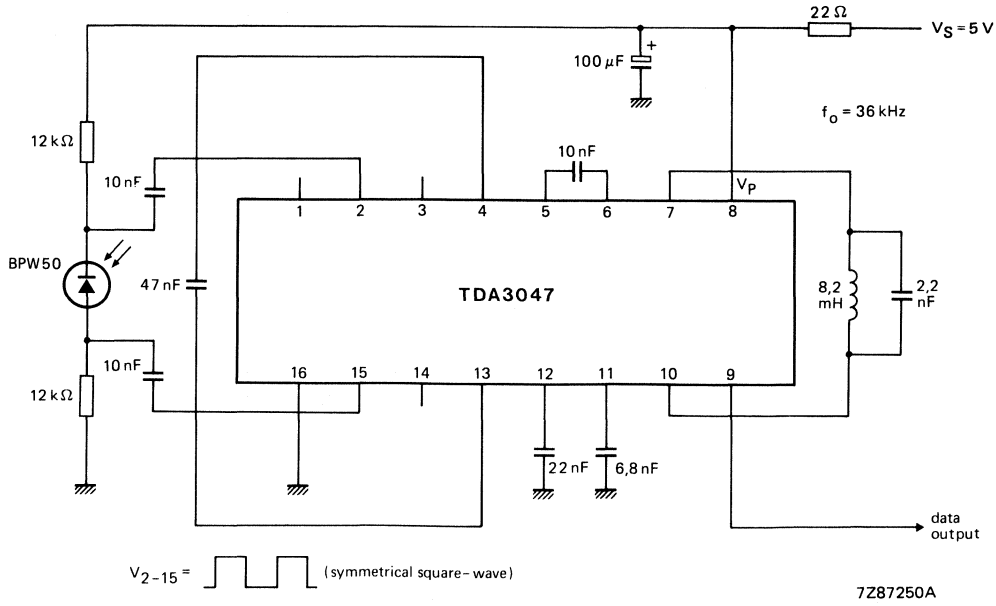


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.
The difference between the TDA3048 and TDA3047 is the polarity of the output signal.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,03 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5 V

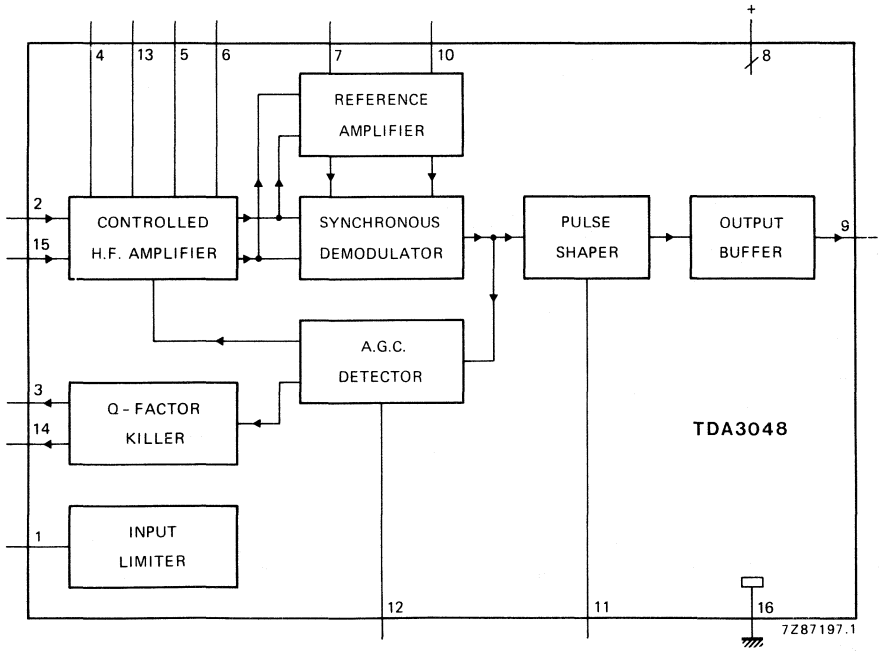


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINES

TDA3048P: 16-lead DIL; plastic (SOT38).
TDA3048T: 16-lead mini-pack; plastic (SO16L; SOT162A).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low*.

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4,5 V
pins 4 and 13	V_{4-13}	max.	4,5 V
pins 5 and 6	V_{5-6}	max.	4,5 V
pins 7 and 10	V_{7-10}	max.	4,5 V
pins 9 and 11	V_{9-11}	max.	4,5 V
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0,03	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2,25	2,45	2,65	V
Input voltage (pin 15)	V_{15-16}	2,25	2,45	2,65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9-8} = 4{,}5$ V	I_9	75	120	–	μA
$-V_{9-8} = 3{,}0$ V	I_9	75	130	–	μA
$-V_{9-8} = 1{,}0$ V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8} = 0{,}5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3,4	3,55	3,7	V
Hysteresis of trigger levels	ΔV_{11-16}	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,4	5,0	6,6	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at V_{12-16} = 2 V	$-I_3$	2,5	7,5	20	μA
Output current (pin 14) at V_{12-16} = 2 V	$-I_{14}$	2,5	7,5	20	μA

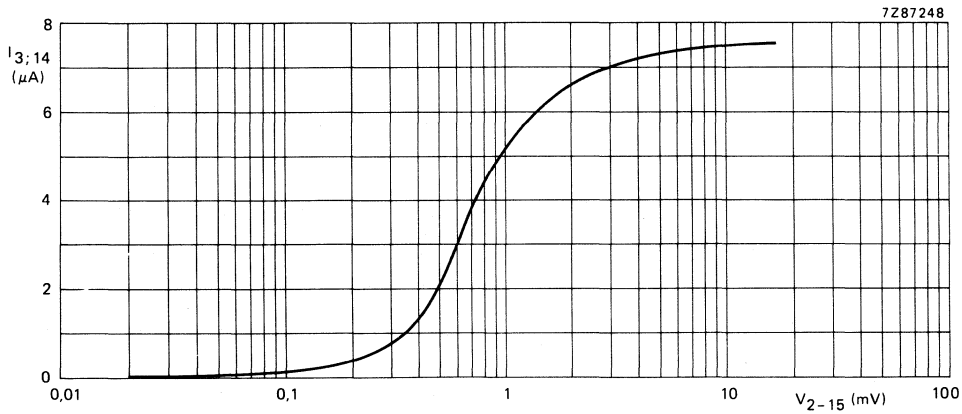
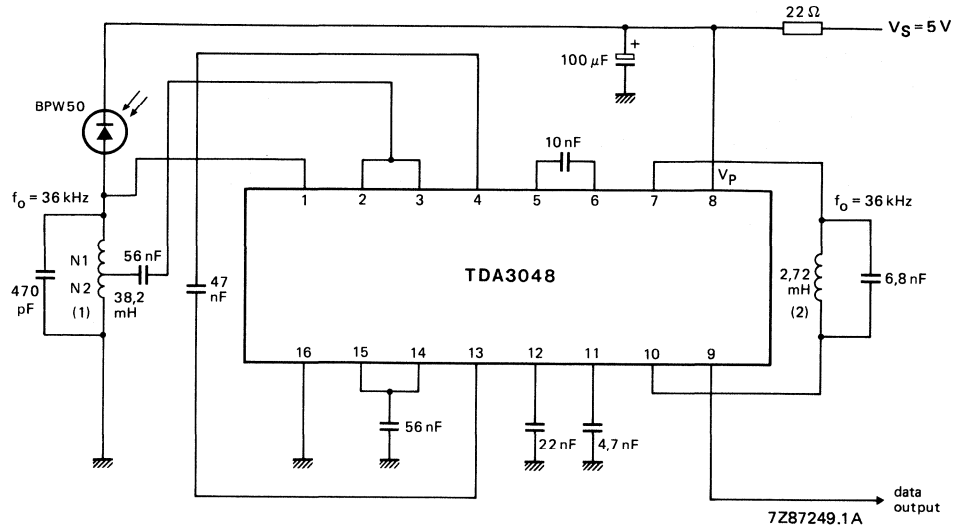


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; V_P = 5 V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

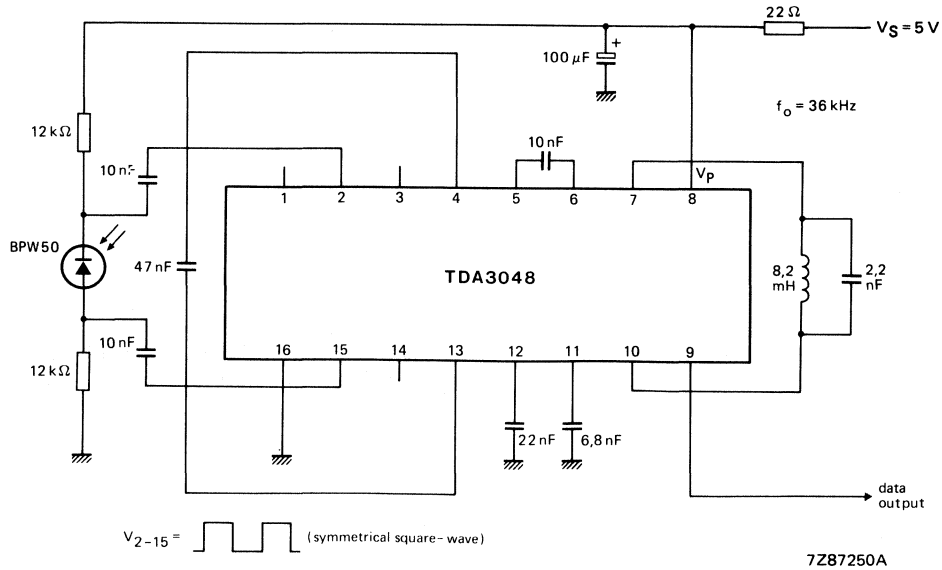


Fig. 4 Wide-band receiver with TDA3048.
For better sensitivity both 12 kΩ resistors may have a higher value.

FM RADIO CIRCUIT

GENERAL DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7010T includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 4)	V_P	2,7 to 10	V
Supply current at V_P = 4,5 V	I_P	typ. 8	mA
R.F. input frequency range	f_{rf}	1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ. 1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ. 200	mV
A.F. output voltage at R_L = 22 kΩ	V_o	typ. 75	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

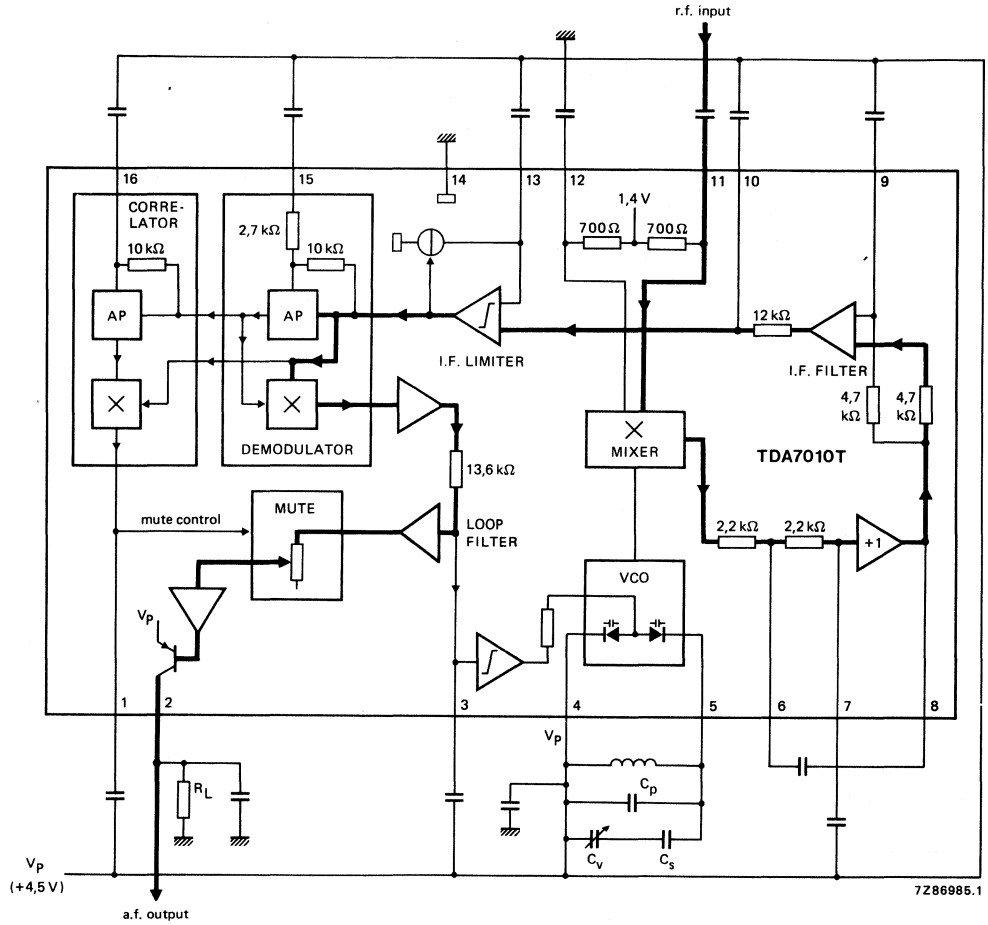


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	V_P	max.	12 V
Oscillator voltage (pin 5)	V_{6-5}	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}		–55 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 60 °C

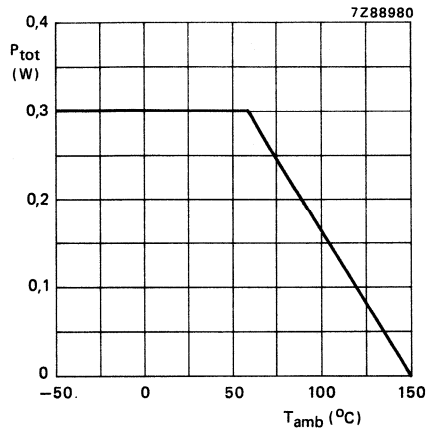


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 5)	I_5	–	280	–	μA
Voltage at pin 12	V_{12-14}	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	V_{2-14}	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 5	$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	43	–	dB
	S_{-300}	–	28	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

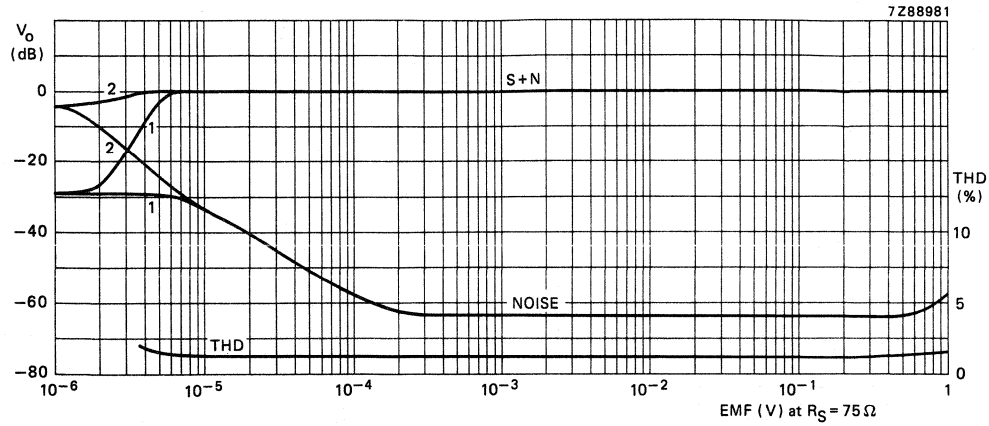


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: $\Delta f = \pm 22{,}5$ kHz; f_m = 1 kHz.
for THD curve: $\Delta f = \pm 75$ kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.

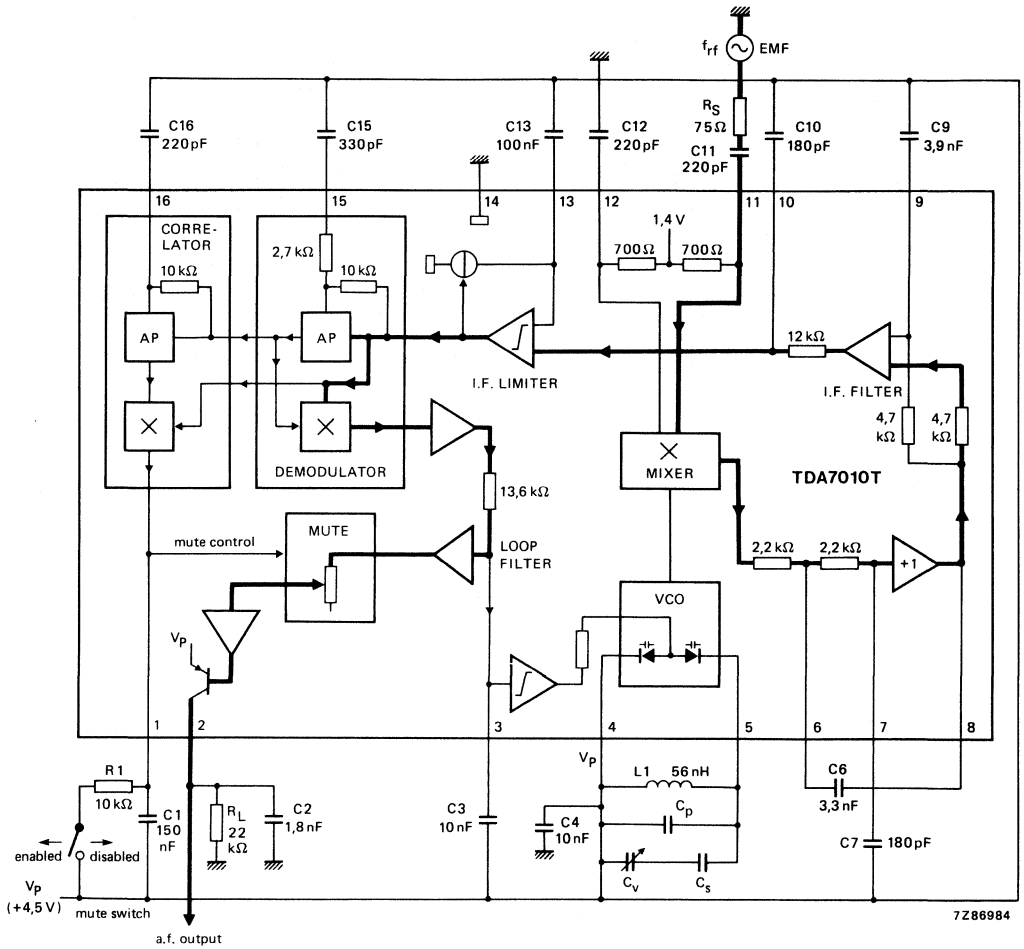


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.

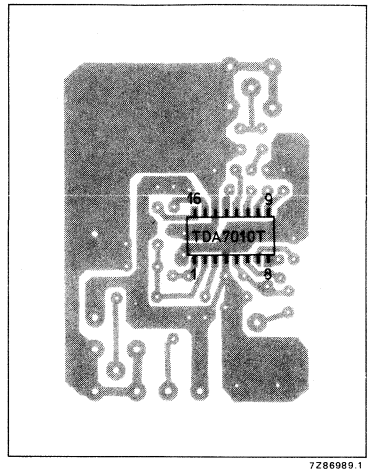


Fig. 5 Track side of printed-circuit board used for the circuit of Fig. 4.

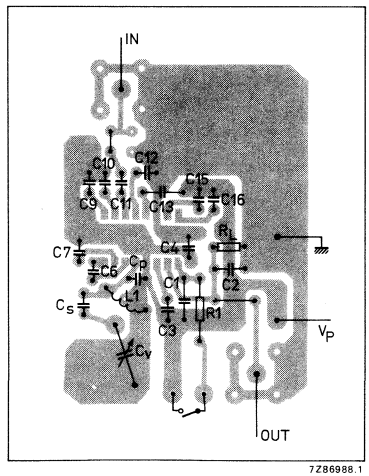


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

FM RADIO CIRCUIT FOR MTS

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  - mono earphone amplifier or
  - MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	–	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
RF input frequency		f_{rf}	1,5	–	110	MHz
Sensitivity (e.m.f.) for –3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	–	4	–	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	–	200	–	mV
AF output voltage		V_o	–	90	–	mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

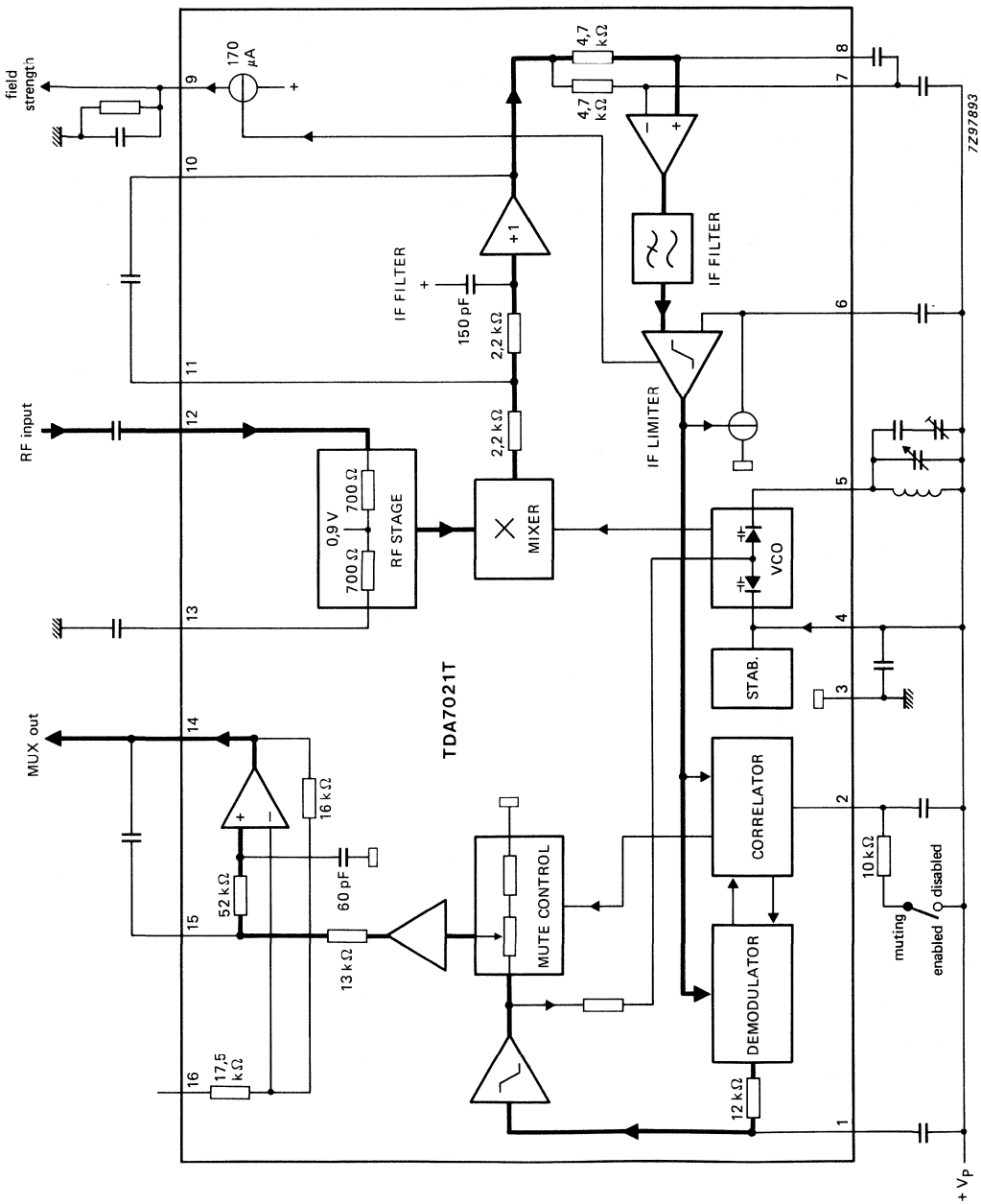


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	–	7,0	V
Oscillator voltage		V_{5-4}	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–10	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 °C, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	μA
Voltage at pin 13		V_{13-3}	–	0,9	–	V
Output voltage (pin 14)		V_{14-3}	–	1,3	–	V

DEVELOPMENT DATA

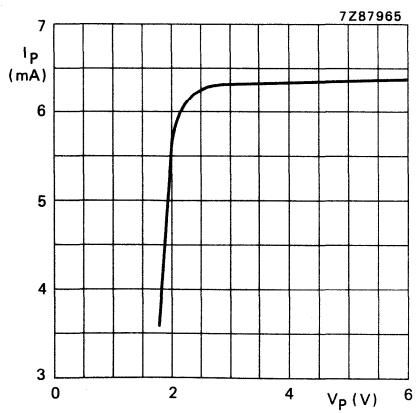


Fig. 2 Supply current as a function of the supply voltage.

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for −3 dB limiting	muting disabled	EMF	–	4,0	–	μV
for −3 dB muting		EMF	–	5,0	–	μV
for (S+N)/N = 26 dB		EMF	–	7,0	–	μV
Signal handling (e.m.f.)	THD < 10%;					
	Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	Δf = ± 22,5 kHz	THD	–	0,7	–	%
	Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5-4(rms)}$	–	250	–	mV
Variation of oscillator frequency with temperature	V_P = 1 V	$\frac{\Delta f_{osc}}{\Delta T_{amb}}$	–	5	–	kHz/°C
Selectivity	see Fig. 9; no modulation	S_{+300}	–	46	–	dB
		S_{-300}	=	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 μs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	−100	–	+100	μA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

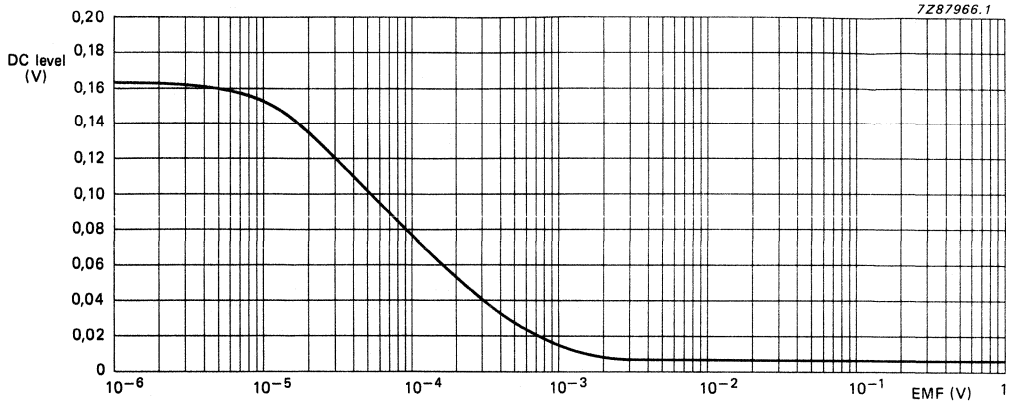


Fig. 3 Field strength voltage (V_{9-3}) at R_{source} = 1 kΩ; f = 96,75 MHz; V_P = 3 V.

DEVELOPMENT DATA

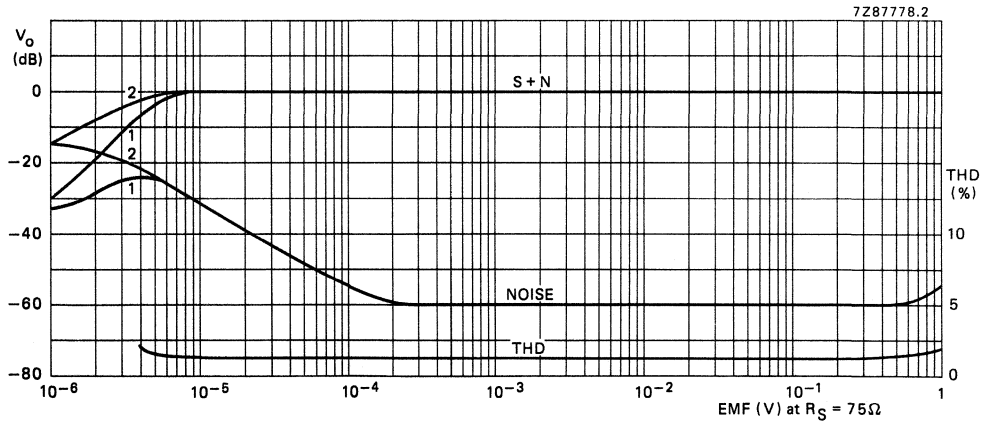
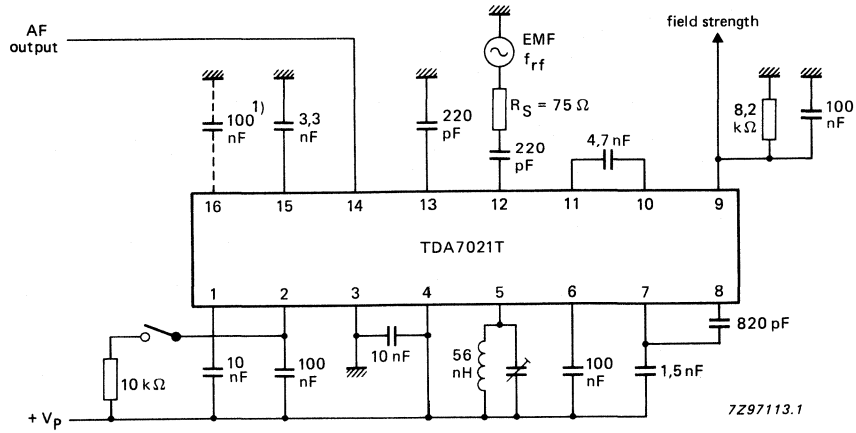


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S_{+300}	–	40	–	dB
		S_{-300}	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on:					
	at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

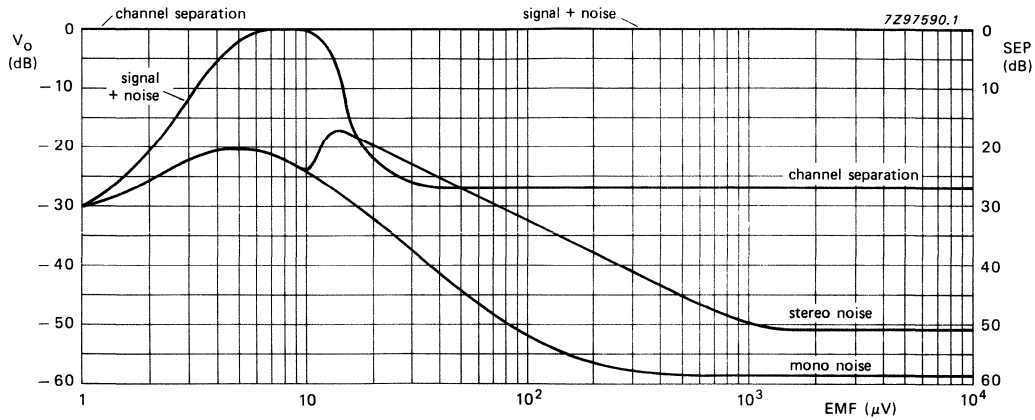


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

DEVELOPMENT DATA

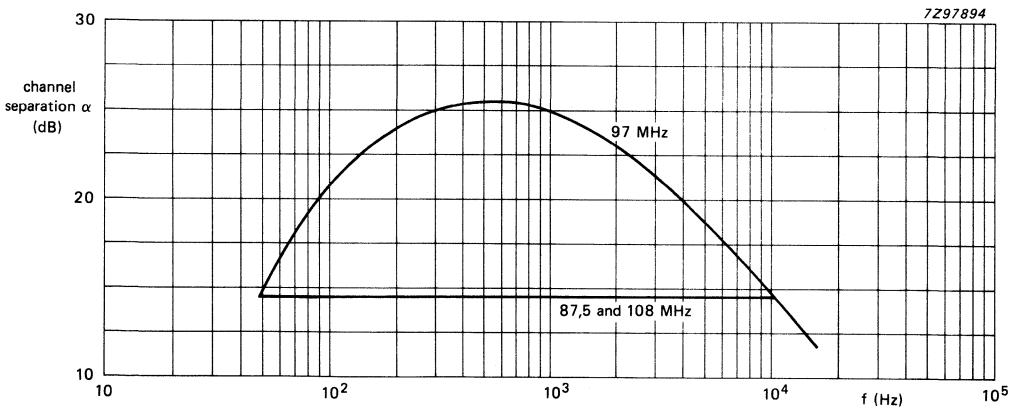


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

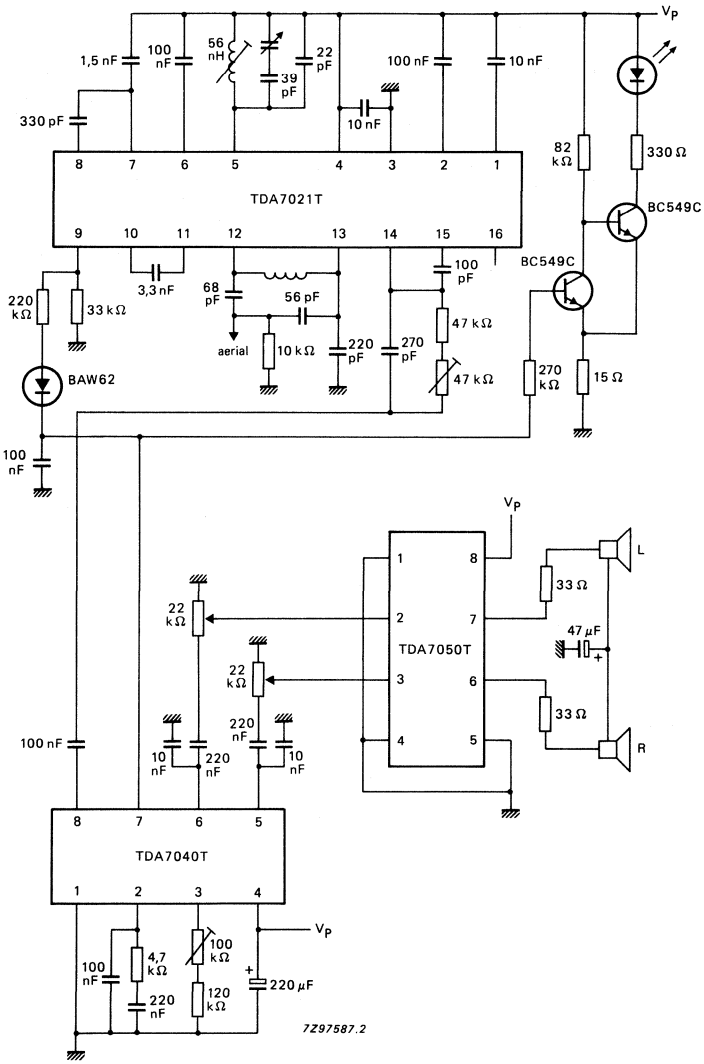


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

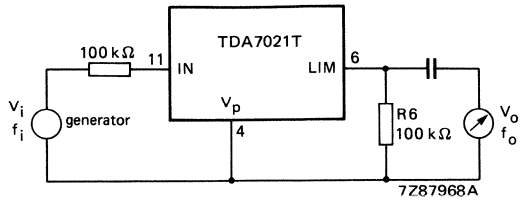


Fig. 9 Test set-up; V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\ \text{kHz} - f_i)}{V_o \mid f_i}$$

$$S_{-300} = 20 \log \frac{V_o \mid (300\ \text{kHz} + f_i)}{V_o \mid f_i}$$

DEVELOPMENT DATA

LOW VOLTAGE MICRO TUNING SYSTEM (MTS)

GENERAL DESCRIPTION

The TDA7030T low voltage tuning system incorporates all analogue and digital functions necessary for complete control of a TDA7021T FM radio receiver. The tuning system coverage is precisely defined by an integrated 100 kHz crystal oscillator.

The complete low voltage radio receiver system comprises:

TDA7021T	Single-chip FM radio receiver;
TDA7030T	Low voltage micro tuning system;
TDA7040T	Low voltage stereo decoder;
TDA7050T	Low voltage stereo power amplifier.

Features

- Memory function with four presets and last-input recall
- Search tuning
- Integrating AFC
- 16-step stereo volume control
- On/off power switch driver
- On-chip interface for 16-point frequency scale LCD

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

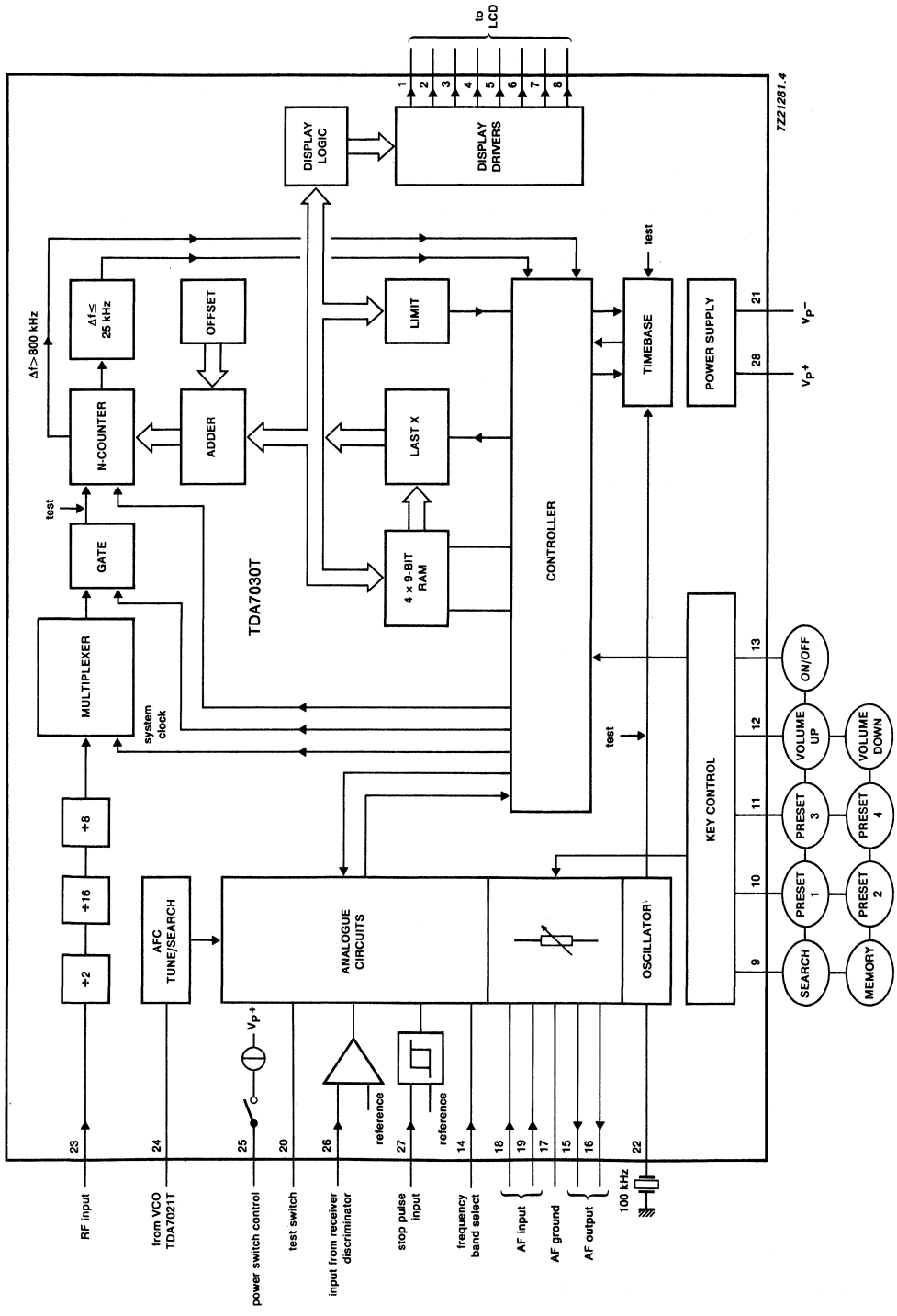


Fig. 1 Block diagram.

Notes to Fig.1

Prescaler first stage (divide-by-2):

input frequency 75.925 to 89.925 MHz (Japan)
87.425 to 107.925 (Europe and USA)
sensitivity 80 mV
input impedance 2.5 kΩ/6 pF
prescaler turns on when radio is switched on

Prescaler second stage (divide-by-16):

current is only switched on for dividing

Prescaler third stage (divide-by-8):

current is only switched on for dividing

Multiplexer:	switches the clock for the N-counter (proportional tuning)
Gate:	gate time 10.24 ms (one digit = 25 kHz)
N-counter:	13-bit down-counter for tuned frequency (one digit = 25 kHz)
Frequency decoder:	supplies N-counter information to the controller
Tuning current control:	1) integrating AFC ± 800 nA 2) search tuning (50 nA) 3) tuning current (800 nA) 4) down-set current (350 μA)
Adder and offset:	allows the system to store information in 9 bits
RAM:	4 x 9-bit
Last X:	last memory and search tuning counter
Limit:	band limit controller
Display drivers:	outputs to drive a 4 x 4 LCD matrix
Controller:	controls the system

DEVELOPMENT DATA

PINNING

pin	description	pin	description
1	LCD matrix: segments 3, 4, 11, 12	15	volume control: AF output right
2	LCD matrix: segments 2, 5, 10, 13	16	volume control: AF output left
3	LCD matrix: segments 1, 6, 9, 14	17	volume control: AF ground
4	LCD matrix: segments 0, 7, 8, 15	18	volume control: AF input right
5	LCD matrix: backplane 4	19	volume control: AF input left
6	LCD matrix: backplane 3	20	test switch
7	LCD matrix: backplane 2	21	negative supply voltage (V_P)
8	LCD matrix: backplane 1	22	oscillator crystal connection
9	key matrix: search/memory	23	RF input from receiver oscillator
10	key matrix: preset 1/preset 2	24	VCO tuning circuit
11	key matrix: preset 3/preset 4	25	current source for power switch transistor
12	key matrix: volume up/volume down	26	input from receiver discriminator
13	key matrix: on/off control	27	stop pulse/field strength
14	frequency band select	28	positive supply voltage (V_P)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 28)	$V_P = V_{28-21}$	−0.5	+ 7.0	V
Supply current (pin 21)	I_{21}	−10	+ 10	mA
AF ground current (pin 17)	I_{17}	−10	+ 10	mA
Input voltage (pins 9 to 16, 18 to 20 and 22 to 27)	V_I	−0.5	7.0	V
Input current (pins 9 to 16, 18 to 20 and 22 to 27)	I_I	–	1.0	mA
Output current (pins 9 to 16, 18 to 20 and 22 to 27)	I_O	–	−1.0	mA
Input voltage LCD matrix (pins 1 to 8)	V_I	−0.5	+ 5.0	V
Input current LCD matrix (pins 1 to 8)	I_I	–	1.0	mA
Output current LCD matrix (pins 1 to 8)	I_O	–	−1.0	mA
Total power dissipation	P_{tot}	–	35	mW
Operating ambient temperature range	T_{amb}	−10	+ 50	°C
Storage temperature range	T_{stg}	−25	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

$V_P = V_{28-21} = 3$ V; $T_{amb} = 25$ °C; all voltages are referred to pin 21; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range for specified operation (pin 28)		V_P	1.8	3.0	4.0	V
Supply current	$V_P = 3$ V					
standby		I_P	–	25	–	μA
radio on (pin 25)	$I_{PCS} = 0$	I_P	–	3.0	–	mA
tuning		I_P	–	6.8	–	mA
LCD matrix (pins 1 to 8)						
Output voltage		V_{LCD}	see Fig.3			
Output sink current	$V_{LCD} = 2$ V	I_{sink}	20	–	–	μA
Output source current	$V_{LCD} = 0.2$ V	I_{source}	–4	–	–	μA
Key matrix (pins 9 to 13)						
ON/OFF	active = HIGH	V_{ON}	V_P–0.1	–	V_P	V
	testmode = LOW	V_{ON}	0	–	0.5	V
Output current	$V_{ON} = 0$ to 0.5 V	I_O	–	–0.5	–	μA
Input current	$V_{ON} = V_P$–0.1 V to V_P	I_I	–	0.5	–	μA
Radio ON		I_I	–	8	–	μA
Search, preset 1, preset 3, volume up						
Active	KEY = HIGH	V_{9-12}	V_P–0.1	–	–	V
Input current	$V_{KEY} = V_P$–0.1 V to V_P	I_I	–	1	–	μA
Memory, preset 2, preset 4, volume down						
Active	KEY = LOW	V_{9-12}	0	–	0.2	V
Output current	$V_{KEY} = 0$ to 0.2 V	I_O	–	–1	–	μA
Frequency band select (pin 14)	frequency band with respect to TDA7021 IF					
76 to 90 MHz		V_{14}	V_P–0.2	–	V_P	V
input current		I_{14}	–	1.0	–	μA
87.5 to 108 MHz		V_{14}	0	–	0.5	V
output current		I_{14}	–	–0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Volume control AF outputs (pins 15 and 16)						
Attenuation in 16 steps, maximum attenuation step 15	R_L = 20 kΩ	$A_{(max.)}$	–	45	–	dB
Minimum attenuation (step 0)	R_L = 20 kΩ	$A_{(min.)}$	–	0	–	dB
AF output impedance		Z_O	–	20	–	kΩ
Attenuation per step;						
steps 1 to 3		$A_{1\text{-}3}$	–	2	–	dB
steps 4 to 12		$A_{4\text{-}12}$	–	3	–	dB
steps 13 to 15		$A_{13\text{-}15}$	–	4	–	dB
Total harmonic distortion	$V_{in} < 65$ mVeff; 1 kHz	THD	–	1.5	–	%
	$V_{in} < 200$ mVeff; 1 kHz	THD	–	–	4	%
Signal-to-noise ratio	measured unweighted from 400 Hz to 15 kHz					
0 dB attenuation		(S+N)/N	–	60	–	dB
20 dB attenuation		(S+N)/N	–	52	–	dB
Volume control AF inputs (pins 18 and 19)						
AF input voltage (RMS value)	total harmonic distortion < 1%	$V_{i(rms)}$	–	–	80	mV
AF input impedance		Z_i	–	10	–	kΩ
Testmode switch (pin 20)						
Testmode		V_{20}	1.8	–	V_P	V
Operating		V_{20}	0	–	0.3	V
Crystal oscillator (pin 22)						
Crystal frequency		f_{osc}	–	100	–	kHz
Series resonance resistance		$R_{(res)}$	–	–	15	kΩ
Shunt capacitance		C_S	–	–	2.5	pF
DC output current		I_{22}	–	–0.5	–	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (pin 23)						
Input frequency		f	50	–	150	MHz
Minimum voltage for save operation between 76 to 110 MHz		$V_{(min.)}$	–	–	90	mV
Maximum input voltage		$V_{(max.)}$	500	–	–	mV
Input resistance		R_I	–	2.5	–	kΩ
Input capacitance		C_I	–	6	–	pF
VCO tuning current (pin 24)						
AFC off		I_{24}	–	0	–	μA
RF down set	V_{28}-V_{24} > 0.2 V					
V_P = 3 V		I_{24}	–350	–	–	μA
V_P = 1.8 V		I_{24}	–150	–	–	μA
V_P = 5 V		I_{24}	–650	–	–	μA
RF tuning		I_{24}	–	800	–	nA
RF search		I_{24}	–	50	–	nA
AFC transconductance	V_{26} = V_{28-26}	g_m	–	5	–	nA/mV
Maximum source current		I_{source}	–800	–	–	nA
Maximum sink current		I_{sink}	800	–	–	nA
Power switch current source (pin 25)						
Minimum source current	V_{25} < 1 V	I_{25}	–500	–	–	μA
Receiver discriminator (pin 26)						
Input voltage	I_{24} = 0 μA	V_{26}	V_P–315	V_P–300	V_P–285	mV
Voltage when pin 26 acts as a voltage source		V_{26}	–	V_P–300	–	mV
Source current		I_{source}	–100	–	–	μA
Sink current		I_{sink}	50	–	–	μA
Stop pulse/field strength input (pin 27)						
Field strength detected		V_{27}	V_P–450	V_P–400	V_P–350	mV
No field strength detected		V_{27}	V_P–850	V_P–800	V_P–750	mV

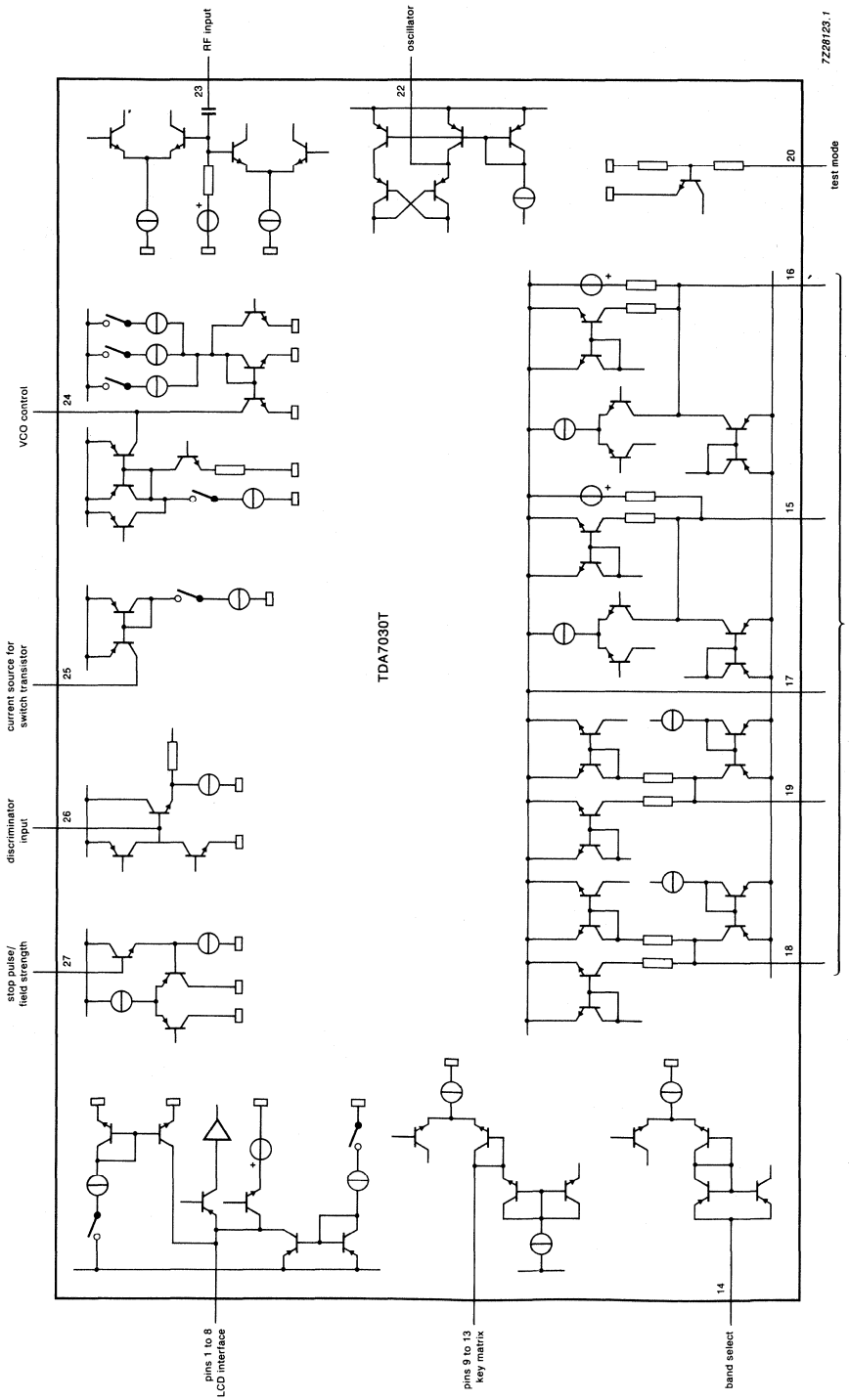
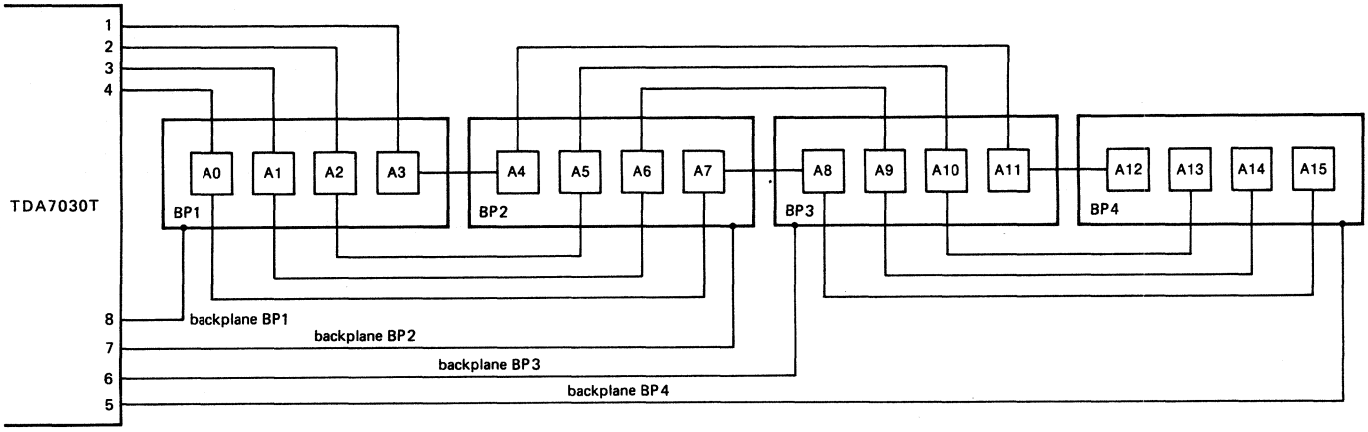
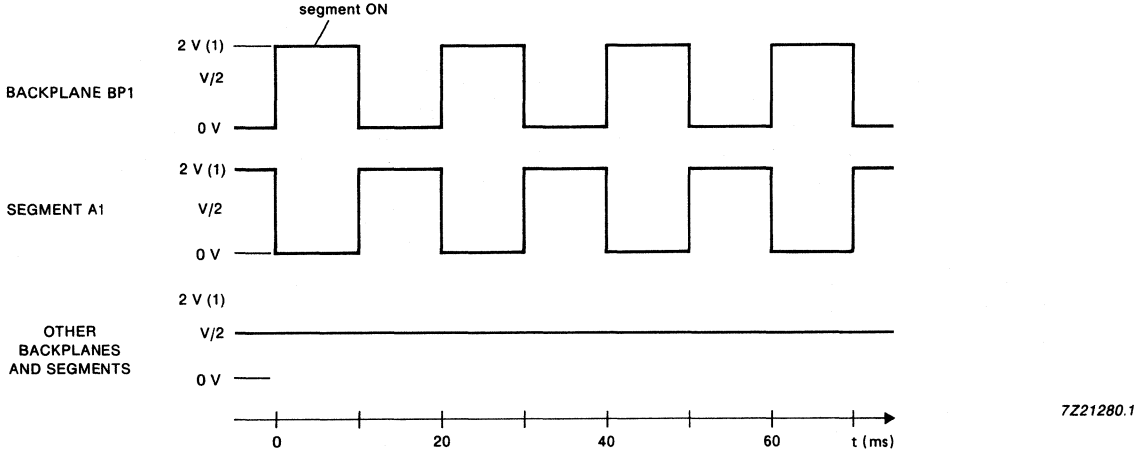


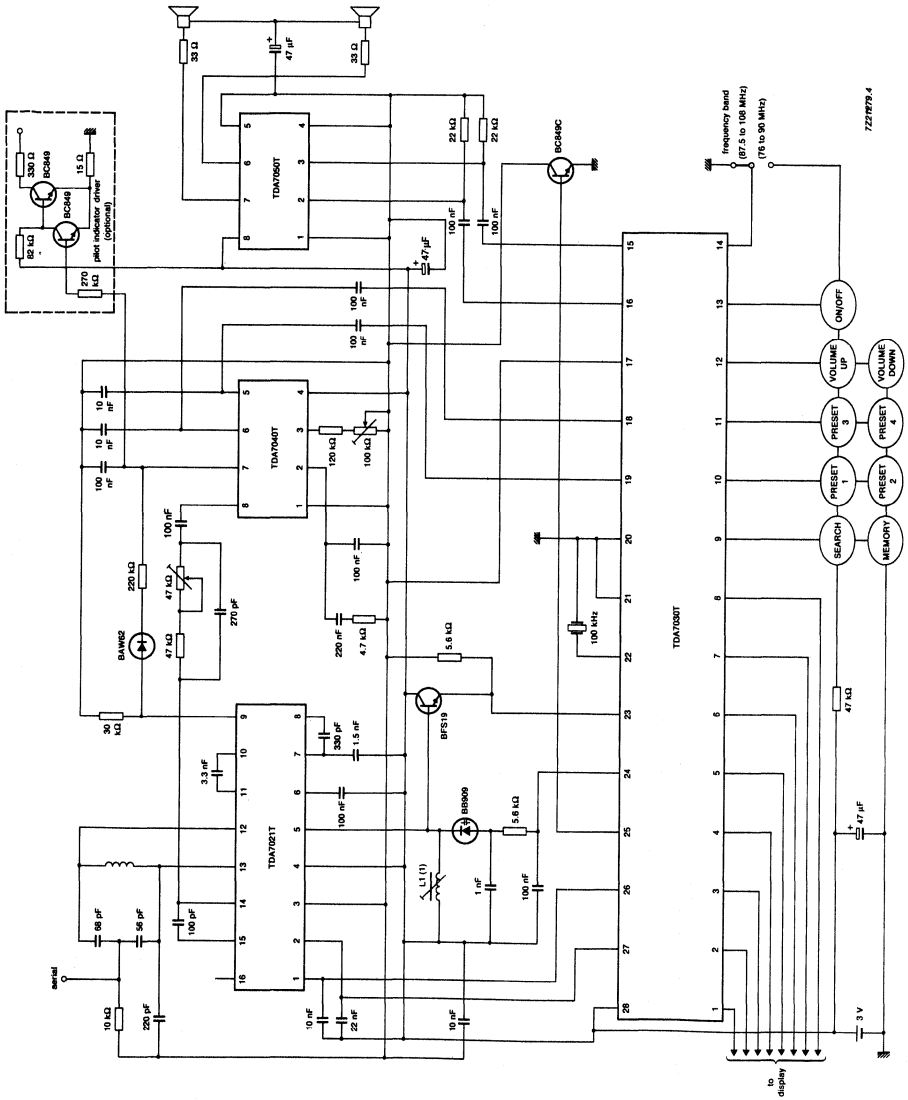
Fig.2 Pin interface diagram.





(1) $V_p \geq 2.2$ V

Fig.3 LCD matrix with waveforms showing drive for segment S1.



(1) From 87.5 to 108 MHz L1 = 52 nH
From 76 to 90 MHz L1 = 69 nH

Fig.4 System application using the TDA7030T in conjunction with the single-chip FM radio receiver (TDA7021T), low voltage stereo decoder (TDA7040T) and low voltage stereo power amplifier (TDA7050T).

LOW VOLTAGE PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA7040T is a monolithic integrated circuit for low cost FM stereo radios with an absolute minimum of peripheral components and a simple lay-out.

Features

- Built-in four pole low pass filter with a 70 kHz corner frequency suppressing unwanted out-of-band input signals
- Fully integrated 228 kHz oscillator
- Pilot presence detector and soft mono/stereo blend
- Built-in interference suppression
- External stereo lamp driver applicable
- Adjustable gain

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	–	6	V
Supply current V_P = 3 V	I_P	–	3	–	mA
Total harmonic distortion	THD	–	0,3	–	%
Signal to noise ratio	S/(S + N)	–	70	–	dB
Channel separation	α	–	40	–	dB

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

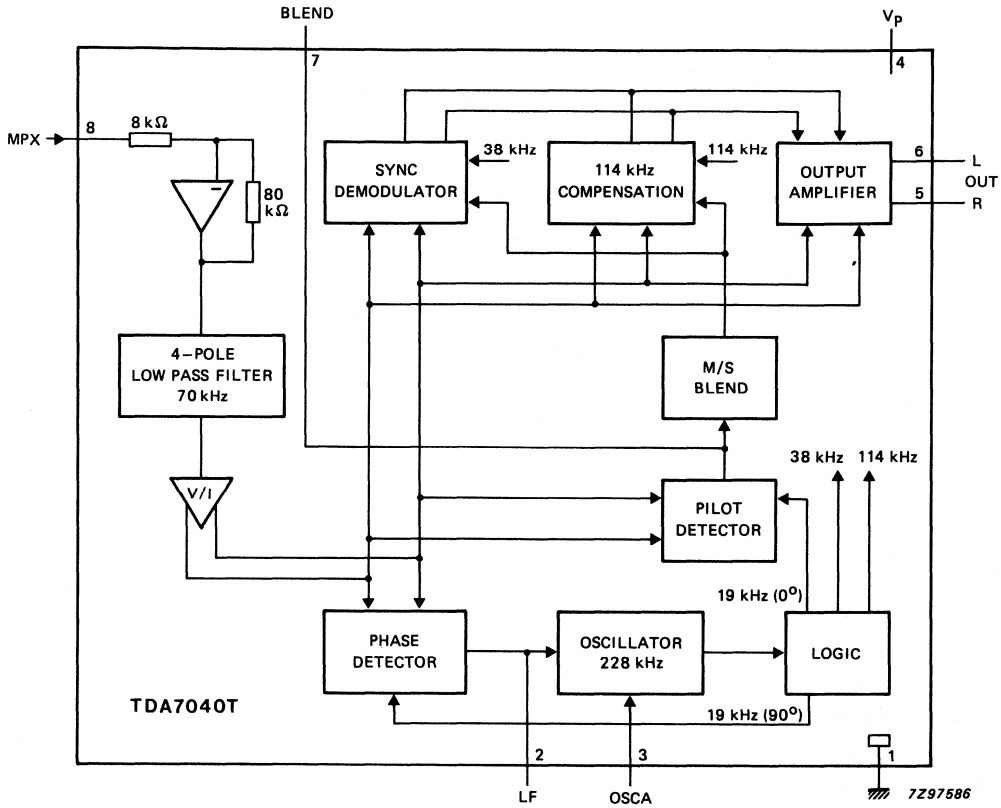


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	–	–	7	V
Operating ambient temperature	T_{amb}	−10	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_P	1,8	3,0	6,0	V
Supply current	I_P	–	3	4	mA
Output voltage (r.m.s. value) $V_{i(rms)}$ L and R 120 mV; f = 1 kHz	$V_{5,\,6\text{-}1}$	–	240	–	mV
Channel balance $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	ΔG_v	–	0	1	dB
Output resistance	R_O	–	5	–	kΩ
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz	THD	–	0,1	–	%
Total harmonic distortion $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	THD	–	0,3	–	%
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz	S/(S + N)	–	70	–	dB
Signal-to-noise ratio $V_{i(rms)}$ = 120 mV; f = 1 kHz $V_{p(rms)}$ = 12 mV	S/(S + N)	–	70	–	dB
Channel separation $V_{i(rms)}$ L and R 40 mV; f = 1 kHz; $V_{p(rms)}$ = 12 mV	α	–	40	–	dB
Capture range $V_{p(rms)}$ = 12 mV; deviation from centre frequency	Δf	–	± 3	–	%
Carrier leak $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz;					
f = 19 kHz		–	30	–	dB
f = 38 kHz		–	50	–	dB
SCA (Subsidiary Communications Authorization) rejection $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{SCA(RMS)}$ = 12 mV; f = 67 kHz	α_{67}	–	70	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
ACI (Adjacent channel interference) $V_{i(rms)}$ L and R 120 mV; $V_{p(rms)}$ = 12 mV; f = 1 kHz; $V_{ACI(RMS)}$ = 1,3 mV; f = 114 kHz $V_{ACI(RMS)}$ = 1,3 mV; f = 190 kHz	α_{114} α_{119}	– –	90 85	– –	dB dB
Traffic radio (V.W.F.) suppression $\alpha_{57(VWF)} = \frac{V_{o(signal)} \text{ (at 1 kHz)}}{V_{o(spurious)} \text{ (at 1 kHz} \pm \text{23 Hz)}}$ measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz, f_m = 23 Hz AM, m = 60%)	$\alpha_{57(VWF)}$	–	75	–	dB

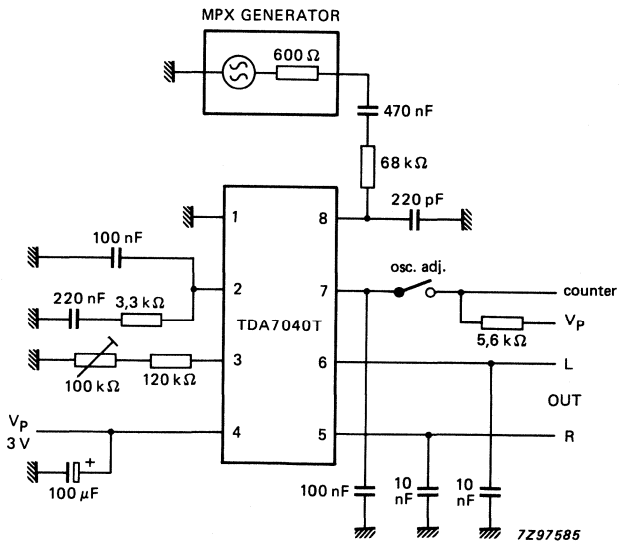


Fig. 2 Test circuit.

DEVELOPMENT DATA

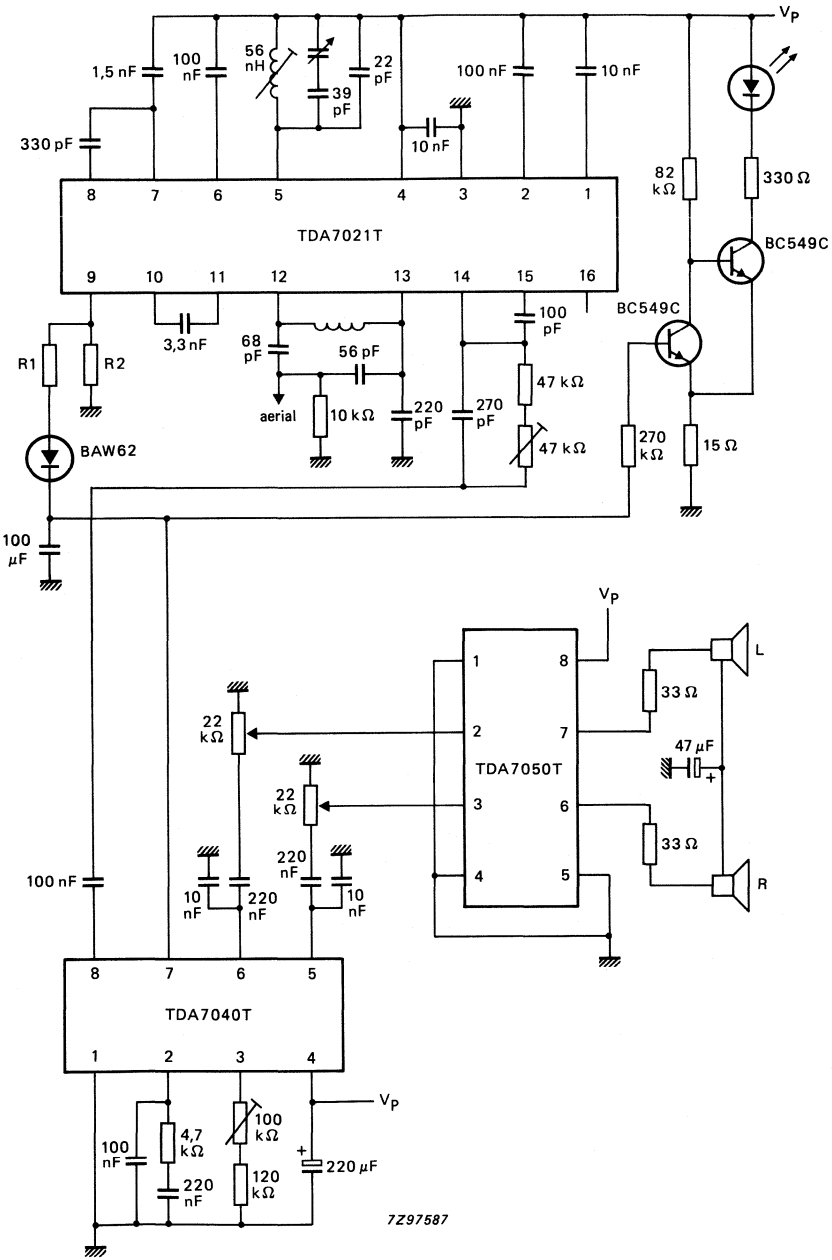


Fig. 3 Application diagram in combination with TDA7021T and TDA7050T.

CHARACTERISTICS

Of the combination TDA7021T, TDA7040T and TDA7050T (Fig. 3).
Conditions unless otherwise specified: $V_{vhf(rms)}$ = 1 mV; f_{hf} = 97 MHz; f_{dev} = 22,5 kHz; $f_{dev\ pilot}$ = 6,75 kHz; noise measured unweighted in a range from 400 Hz to 15 kHz.

parameter	symbol	min.	typ.	max.	unit
Total harmonic distortion (pilot on)					
V_i = (L + R) signal; f_{mod} = 1 kHz	THD	–	0,5	–	%
V_i = L signal; f_{mod} = 1 kHz	THD	–	1,0	–	%
Signal to noise ratio					
V_i = (L + R) signal; f_{mod} = 1 kHz					
pilot off	S/(S + N)	–	56	–	dB
pilot on	S/(S + N)	–	50	–	dB
Channel separation					
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 97 MHz	α	–	26	–	dB
V_i = L-signal, f_{mod} = 1 kHz; pilot on; f_{RF} = 87,5 MHz and 108 MHz	α	–	14	–	dB
Output voltage (pilot off)					
V_i = (L + R) signal, f_{mod} = 1 kHz	$V_{o(rms)}$	–	80	–	mV

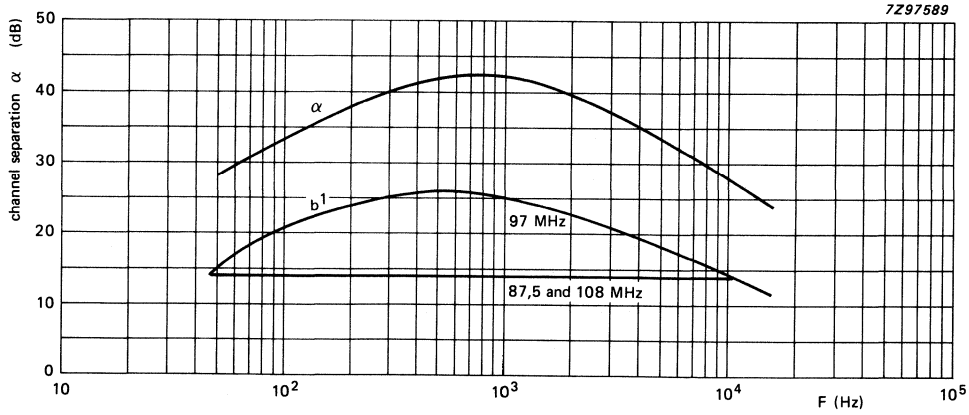


Fig. 4 Channel separation as a function of audio frequency.
a = measured in test circuit (Fig. 2)
b = measured in application diagram (Fig. 3)

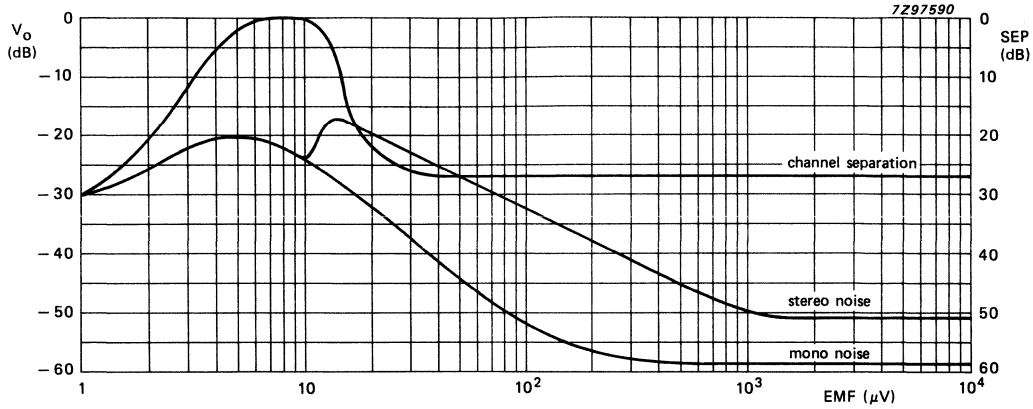


Fig. 5 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 270 kΩ and R2 = 13 kΩ; without diode BAW62.

DEVELOPMENT DATA

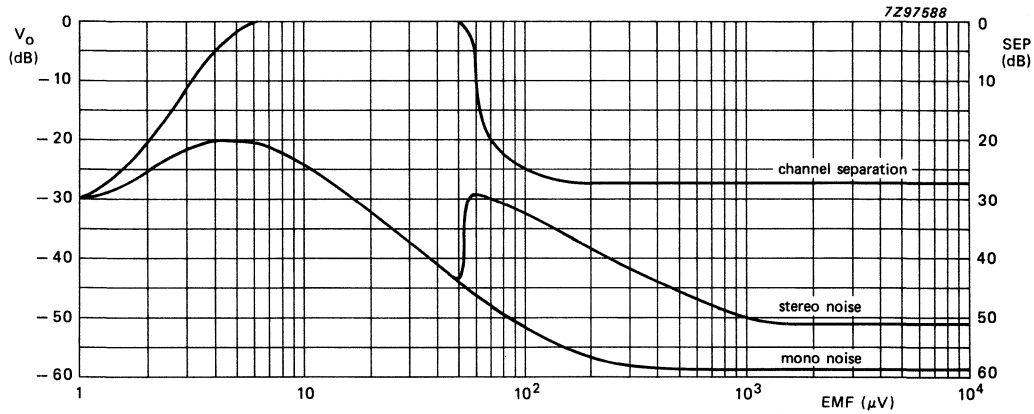


Fig. 6 Signal/noise and channel separation behaviour in Fig. 3. at R1 = 200 kΩ, R2 = 30 kΩ; with diode BAW62.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0		V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max.	70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

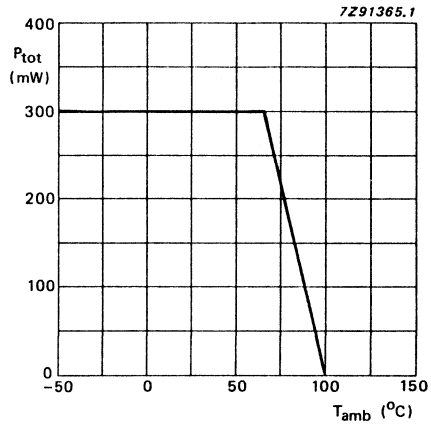


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

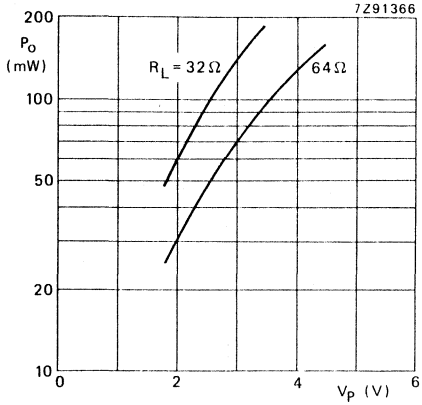


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

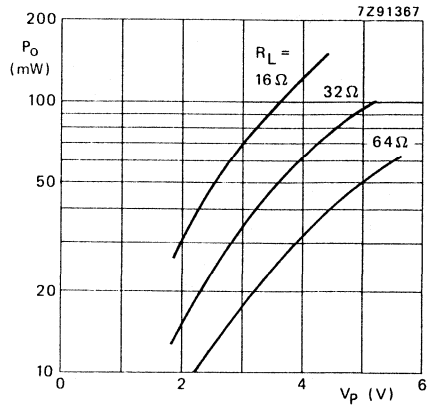


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

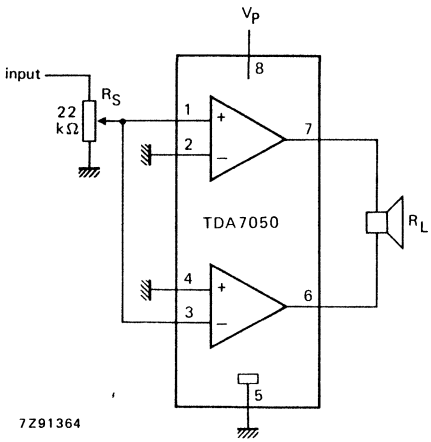


Fig. 4 Application diagram (BTL); also used as test circuit.

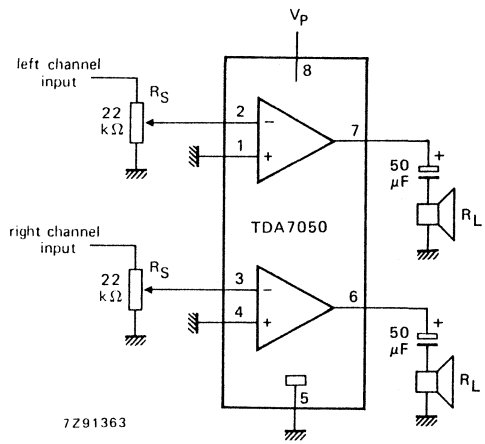


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

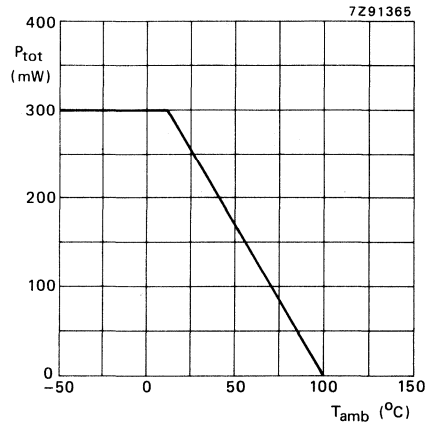


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

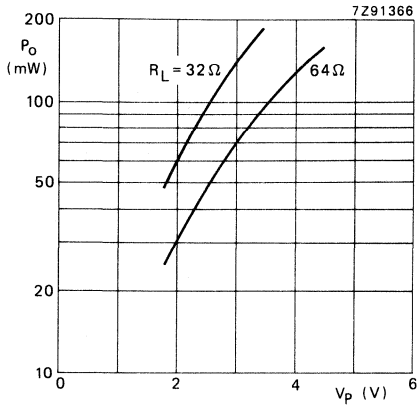


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

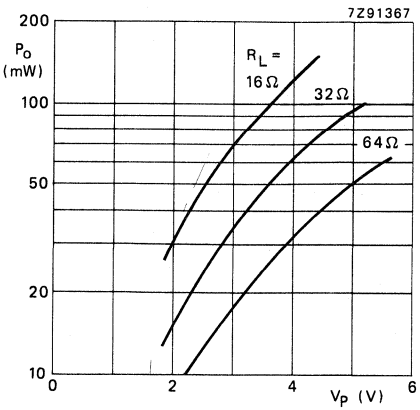


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

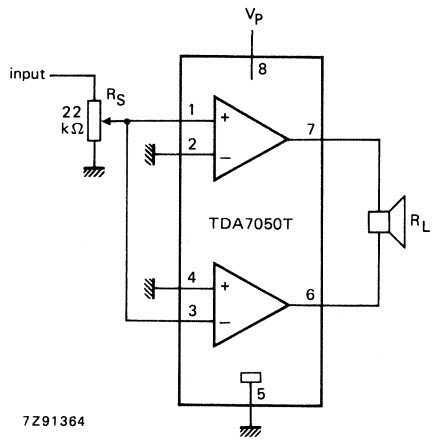


Fig. 4 Application diagram (BTL); also used as test circuit.

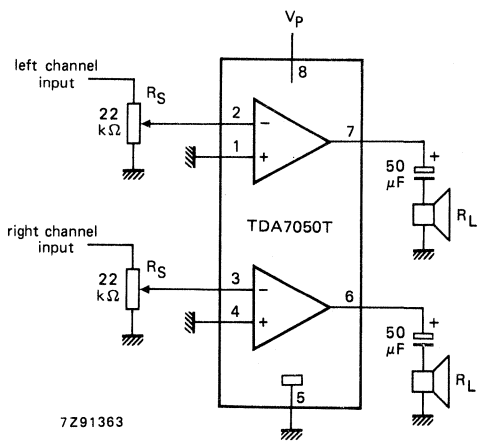


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

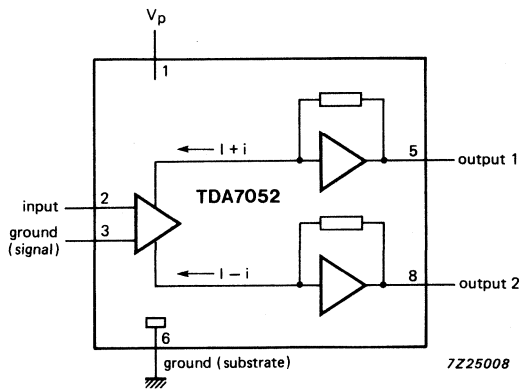


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−65	+150	°C

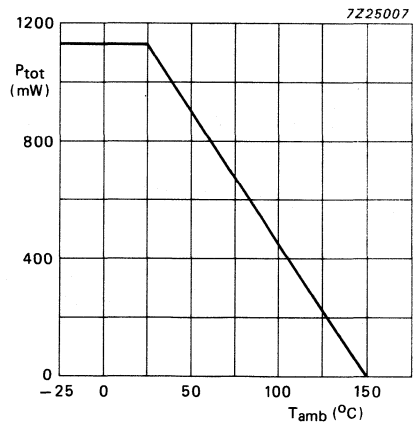


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%	P_o	–	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

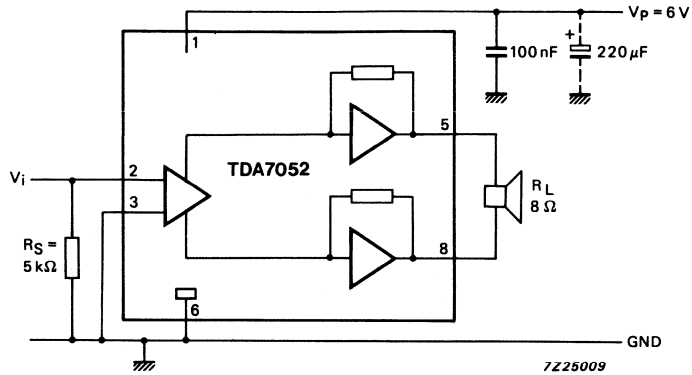


Fig. 3 Application diagram.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_v	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

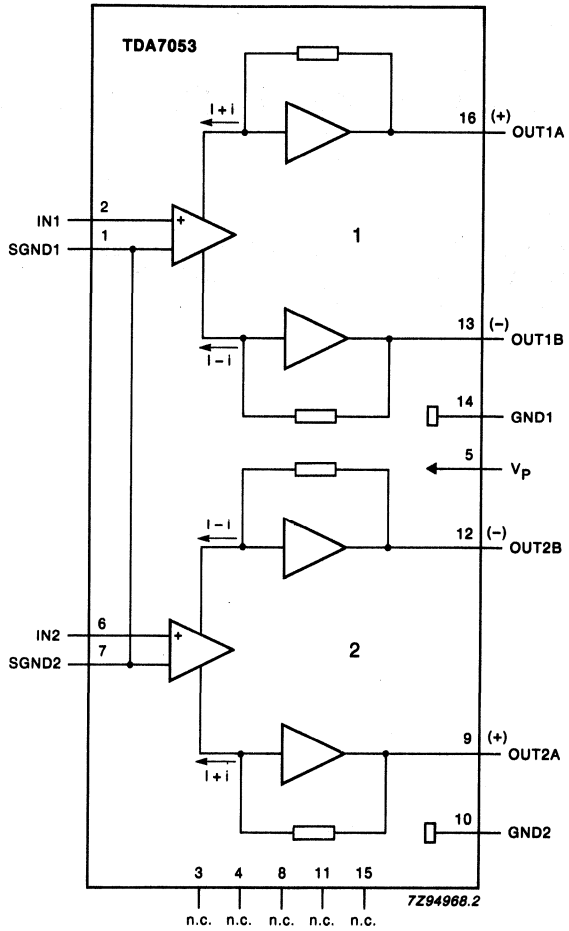


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	−65	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

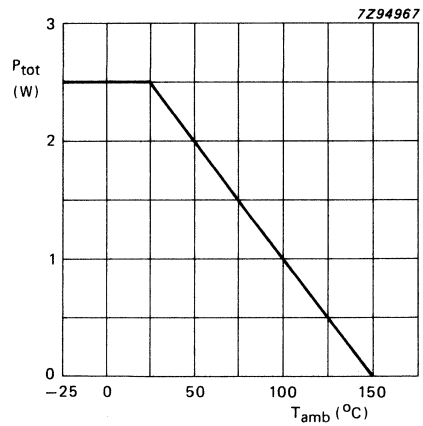


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_V	38	39	40	dB
Channel balance		ΔG_V	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

APPLICATION INFORMATION

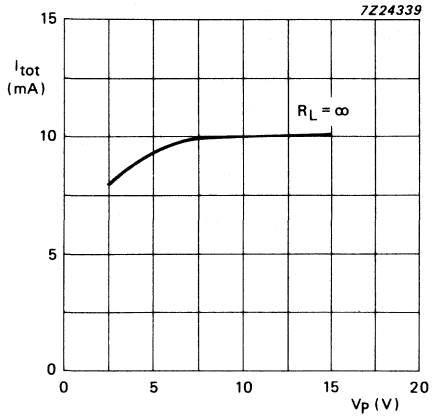


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

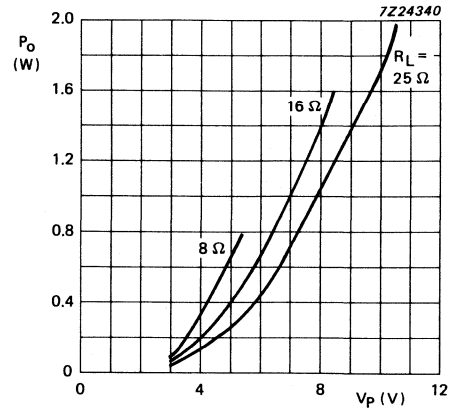
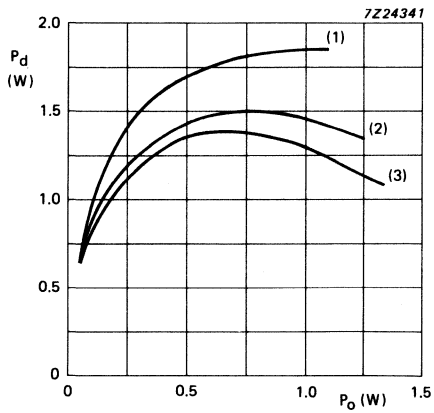
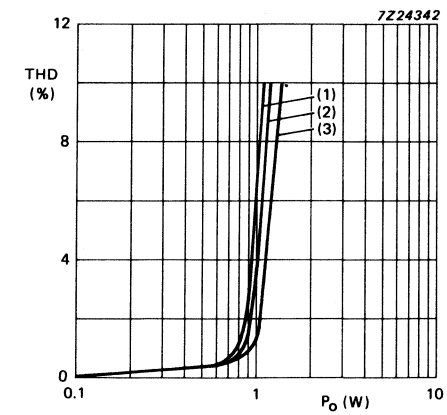


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

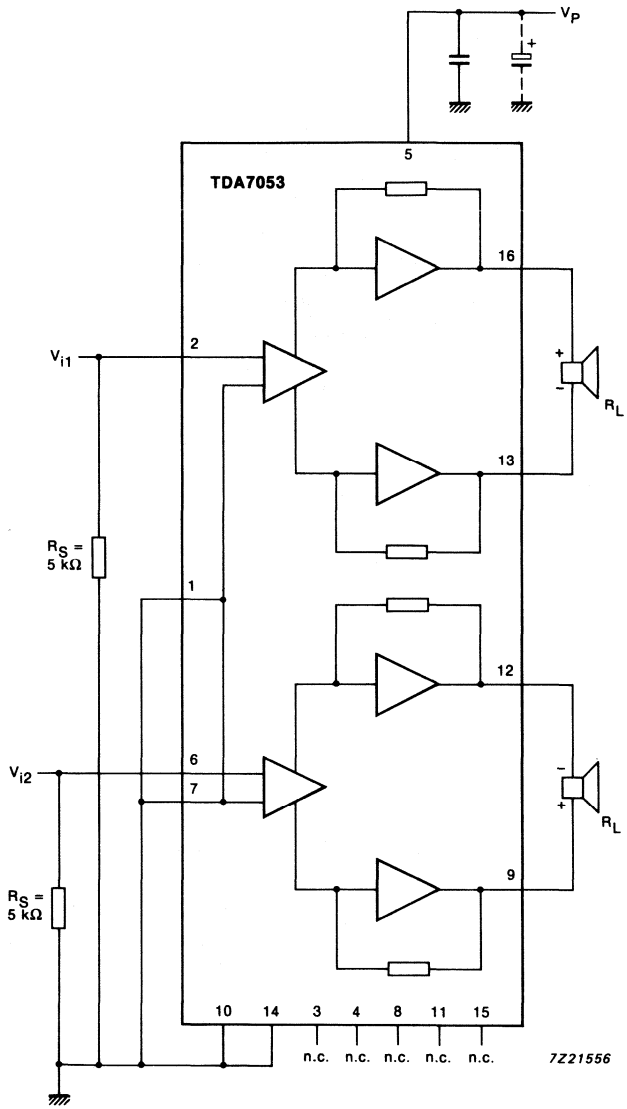


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

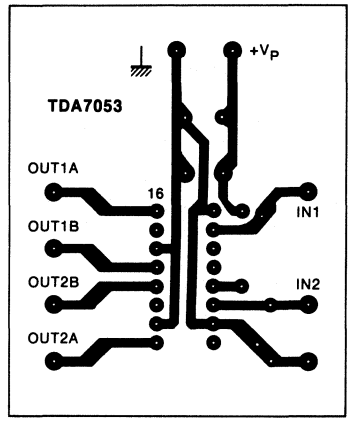


Fig. 8 Printed-circuit board, track side.

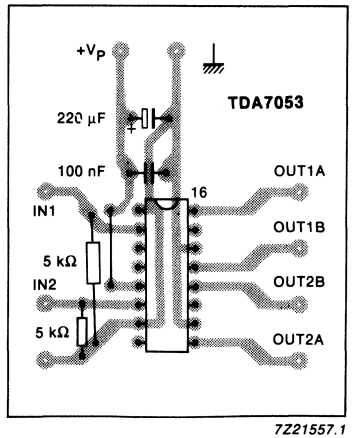


Fig. 9 Printed-circuit board, component side.

Philips Components

Data sheet	
status	Product specification
date of issue	September 1990

TDA7056

3 Watt mono BTL audio output amplifier

FEATURES

- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7056 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11 V	-	3	-	W
G_V	internal voltage gain		39	40	41	dB
I_P	total quiescent current	V_P = 11 V; $R_L = \infty$	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110B

3 Watt mono BTL audio output amplifier TDA7056

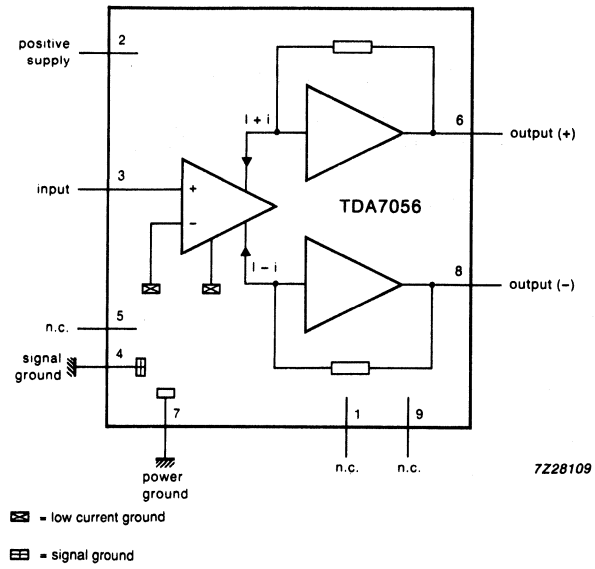


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	n.c.
2	V_P
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (-)
9	n.c.

FUNCTIONAL DESCRIPTION

The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television.
For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.
The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		-	18	V
I_{ORM}	Peak output current repetitive		-	1	A
I_{OSM}	Peak output current non-repetitive		-	1.5	A
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		-	150	°C
P_{tot}	total power dissipation	$T_{case} < 60$ °C	-	9	W
T_{sc}	short circuiting time	see note	-	1	hr

Note

The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	NOM.	UNIT
$R_{th\ j\text{-}c}$	from junction to case	10	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	K/W

POWER DISSIPATION

Assume: $V_P = 11$ V; $R_L = 16\ \Omega$.

The maximum sine-wave dissipation is 1.52 W.

The $R_{th\ j\text{-}a}$ of the package is 55 K/W.

T_{amb} max = 150 - 55 x 1.52 = 66.4 °C.

CHARACTERISTICS

At T_{amb} = 25 °C; f = 1 kHz; V_P = 11 V; R_L = 16 Ω (see Fig.2)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		3	11	18	V
I_{ORM}	repetitive peak output current		-	-	0.6	A
I_P	total quiescent current	note 1 $R_L = \infty$	-	5	7	mA
P_O	output power	THD = 10%	2.5	3	-	W
THD	total harmonic distortion	P_O = 0.5 W	-	0.25	1	%
G_v	voltage gain		39	40	41	dB
V_{no}	noise output voltage	note 2	-	180	300	μV
V_{no}	noise output voltage	note 3	-	60	-	μV
	frequency response		-	20 to 20.000	-	Hz
RR	ripple rejection	note 4	40	50	-	dB
ΔV	DC-output offset voltage	note 5	-	-	200	mV
$\|Z_i\|$	input impedance		-	100	-	kΩ
I_i	input bias current		-	100	300	nA

Notes to the characteristics

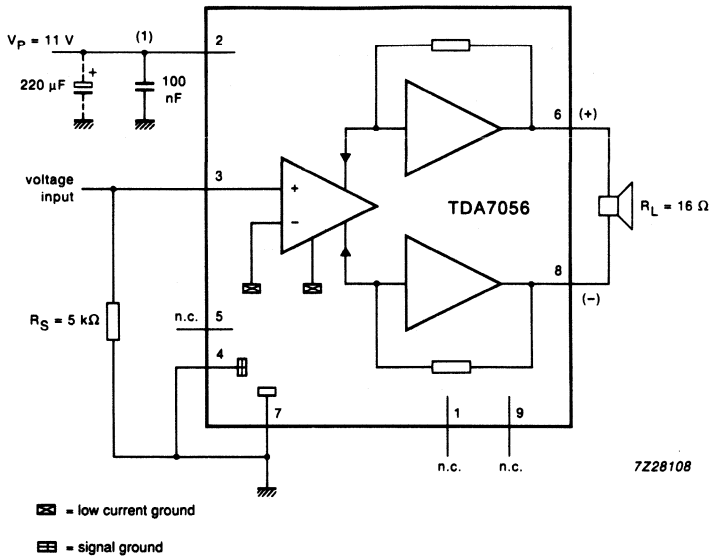
1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.

2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).

3. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz. With a practical load (R_L = 16 Ω, L_L = 200 μH) the noise output current is only 50 nA.

4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.

5. R_S = 5 kΩ



(1) This capacitor can be omitted if the supply electrolytic capacitor is placed closer to pin 2.

Fig.2 Test and application diagram.

SINGLE POWER DRIVER

GENERAL DESCRIPTION

The TDA7072 is a single power driver circuit in a Bridge-Tied-Load (BTL) configuration and is intended for use as a power driver in servo systems with a single supply. It has been primarily designed for use in compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Features

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suitable for handling pulse width modulated (PWM) signals up to 176 kHz
- Electrostatic discharge (ESD) protection on all pins

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Internal voltage gain		G_v	38	39	40	dB
Slew rate		SR	–	6	–	V/μs
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Input bias current		I_{bias}	–	100	300	nA
Cut-off frequency	–3 dB	f_h	–	1.5	–	MHz

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

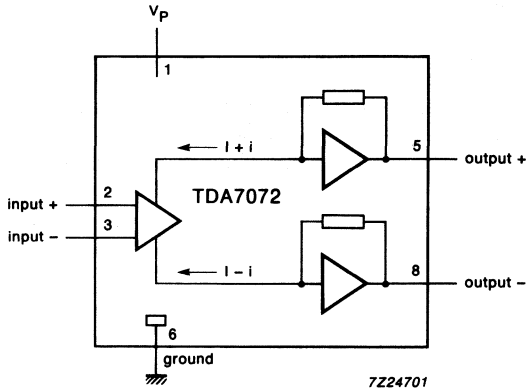


Fig.1 Block diagram.

PINNING

1. Positive supply voltage (V_P)
2. Positive input
3. Negative input
4. Not connected
5. Positive output
6. Ground
7. Not connected
8. Negative output

FUNCTIONAL DESCRIPTION

The TDA7072 is a single power driver circuit in a BTL configuration and is intended for use as a power driver for servo systems with a single supply. It has been primarily designed for compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Utilization of the BTL principle means the device can supply a bidirectional current to the load, with only a single supply voltage.

The voltage gain is fixed by internal feedback at 39 dB and the device operates in a wide supply voltage range (3 to 15 V).

The device can supply a maximum output current of 0.6 A, but the load can be short-circuited under all input conditions.

The differential inputs can handle common mode input voltages from ground (0 V) up to ($V_P - 2.2$) V.

The device has a very high slew rate and due to the very large bandwidth it can handle PWM signals up to 176 kHz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Peak output current					
repetitive		I_{ORM}	–	1	A
non-repetitive		I_{SOM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig.2		
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–65	+ 150	°C
Short-circuiting time	note 1	t_{sc}	–	1	hour

Note to the ratings

1. The load can be short-circuited for all input conditions.

DEVELOPMENT DATA

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 100 K/W

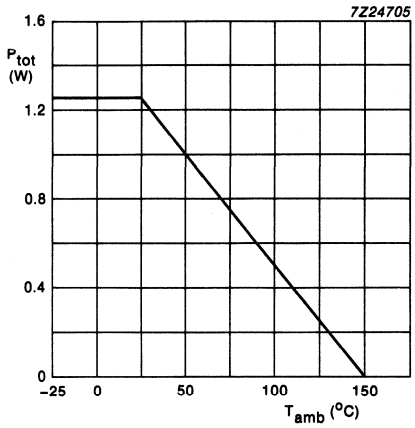


Fig.2 Power derating curve.

Power dissipation example

At T_{amb} = 60 °C the maximum power dissipation is: $\frac{150-60}{100}$ = 0.9 W

CHARACTERISTICS

V_P = 5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Output voltage swing (peak-to-peak value)	note 1	$V_{o(p-p)}$	–	5.6	–	V
Total harmonic distortion	$V_{o(rms)}$ = 1 V	THD	–	0.2	1	%
Voltage gain		G_v	38	39	40	dB
Noise output voltage (RMS value)	note 2	$V_{no(rms)}$	–	150	300	μV
Bandwidth		B	–	1.5	–	MHz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage	R_S = 500 Ω	$\lvert\Delta V_{5-8}\rvert$	–	–	100	mV
DC common-mode voltage range	note 4	V_{IC}	–	0–2.8	–	V
DC common-mode rejection ratio		CMRR	–	*	–	dB
Input impedance		$\lvert Z_I \rvert$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The output voltage swing is typically limited to 2 x (V_P – 2.2) V (see Fig.4).
2. The noise output voltage (RMS value) is measured with a source impedance (R_S) of 500 Ω, unweighted and a bandwidth of 20 Hz to 20 kHz.
3. The ripple rejection is measured with the source impedance R_S = 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage (200 mV, RMS value) is applied to the positive supply rail.
4. The DC common-mode voltage range is limited to (V_P – 2.2) V.

DEVELOPMENT DATA

* Value to be fixed.

TEST AND APPLICATION INFORMATION

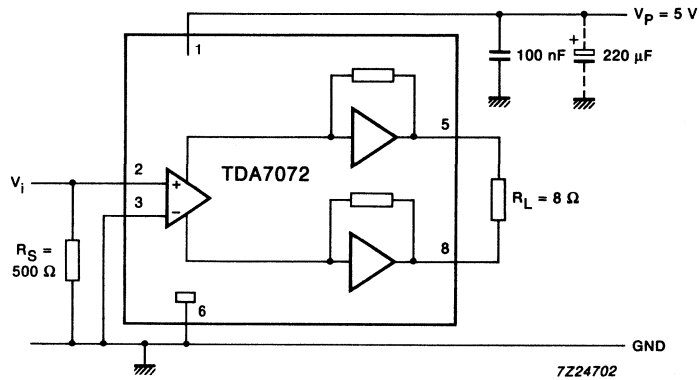


Fig.3 Test circuit diagram.

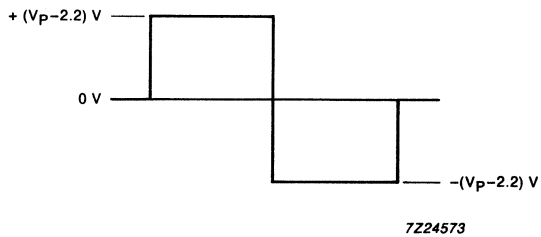


Fig.4 Maximum output voltage swing across R_L.

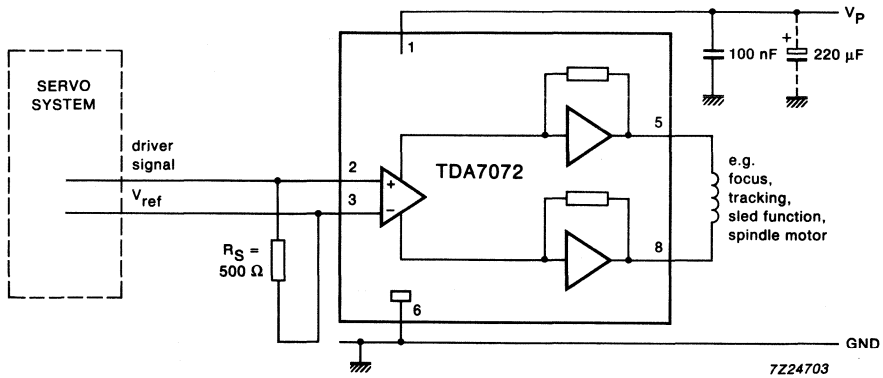


Fig.5 Application circuit diagram.

DEVELOPMENT DATA

DUAL POWER DRIVER

GENERAL DESCRIPTION

The TDA7073 is a dual power driver circuit in a Bridge-Tied-Load (BTL) configuration and is intended for use as a power driver in servo systems with a single supply. It has been primarily designed for use in compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Features

- No external components
- Very high slew rate
- Single power supply
- Short-circuit proof
- High output current (0.6 A)
- Wide supply voltage range
- Low output offset voltage
- Suitable for handling pulse width modulated (PWM) signals up to 176 kHz
- Electrostatic discharge (ESD) protection on all pins

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	8	16	mA
Internal voltage gain		G_v	38	39	40	dB
Slew rate		SR	–	6	–	V/μs
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Input bias current		I_{bias}	–	100	300	nA
Cut-off frequency	−3 dB	f_h	–	1.5	–	MHz

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

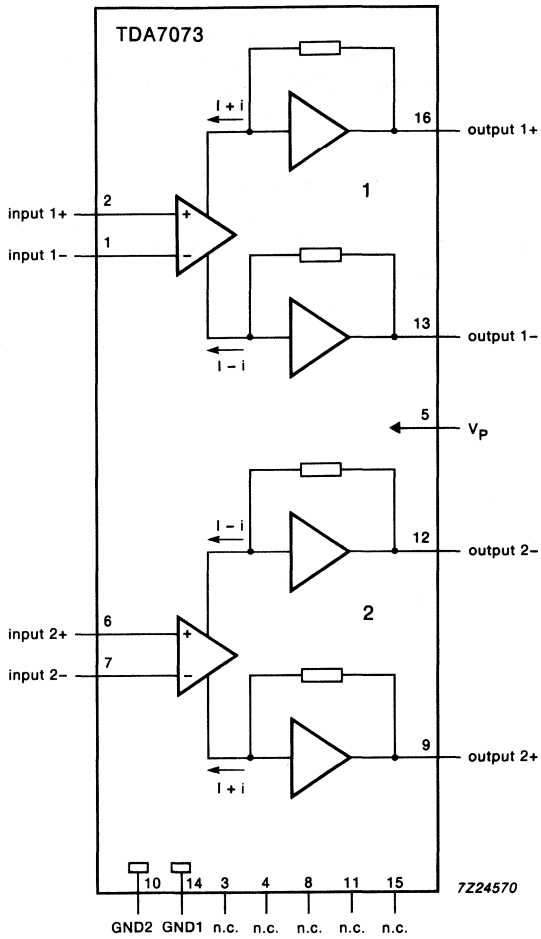


Fig.1 Block diagram.

PINNING

1. Negative input 1
2. Positive input 1
3. Not connected
4. Not connected
5. Supply voltage V_P
6. Positive input 2
7. Negative input 2
8. Not connected
9. Positive output 2
10. Ground 2
11. Not connected
12. Negative output 2
13. Negative output 1
14. Ground 1
15. Not connected
16. Positive output 1

FUNCTIONAL DESCRIPTION

The TDA7073 is a dual power driver circuit in a BTL configuration and is intended for use as a power driver for servo systems with a single supply. It has been primarily designed for compact disc players and is capable of driving focus, tracking, sled functions and spindle motors.

Utilization of the BTL principle means the device can supply a bidirectional current to the load, with only a single supply voltage.

The voltage gain is fixed by internal feedback at 39 dB and the device operates in a wide supply voltage range (3 to 15 V).

The device can supply a maximum output current of 0.6 A, but the load can be short-circuited under all input conditions.

The differential inputs can handle common mode input voltages from ground (0 V) up to ($V_P - 2.2$) V.

The device has a very high slew rate and due to the very large bandwidth it can handle PWM signals up to 176 kHz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Peak output current					
repetitive		I_{ORM}	–	1	A
non-repetitive		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig.2		
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−65	+150	°C
Short circuit time	note 1	t_{sc}	–	1	hour

Note to the ratings

1. The load can be short-circuited for all input conditions.

DEVELOPMENT DATA

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 50 K/W

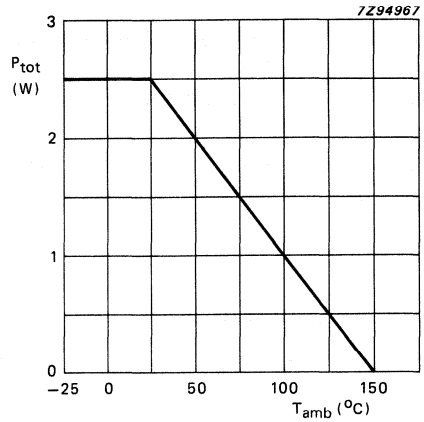


Fig.2 Power derating curve.

Power dissipation example

At T_{amb} = 60 °C the maximum allowable power dissipation is:

$$\frac{150 - 60}{50} = 1.8\ W$$

CHARACTERISTICS

V_P = 5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; see test circuit, Fig.3.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	5	15	V
Repetitive peak output current		I_{ORM}	–	–	0.6	A
Total quiescent current	$R_L = \infty$	I_{tot}	–	8	16	mA
Output voltage swing (peak-to-peak value)	note 1	$V_{o(p-p)}$	–	5.6	–	V
Total harmonic distortion	$V_{o(rms)}$ = 1 V	THD	–	0.2	–	%
Voltage gain		G_v	38	39	40	dB
Noise output voltage	note 2	$V_{no(rms)}$	–	150	300	μV
Bandwidth		B	–	1.5	–	MHz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage	R_S = 500 Ω	$\lvert\Delta V_{16-13}\rvert$	–	–	100	mV
		$\lvert\Delta V_{12-9}\rvert$	–	–	100	mV
DC common-mode voltage range	note 4	V_I	–	0 - 2.8	–	V
DC common-mode rejection ratio		CMRR	–	*	–	dB
Input impedance		$\lvert Z_I\rvert$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA
Channel separation		α	40	50	–	dB
Channel unbalance		$\lvert\Delta G_v\rvert$	–	–	1	dB

DEVELOPMENT DATA

Notes to the characteristics

1. The output voltage swing is typically limited to 2 x (V_P – 2.2) V, (see Fig.4).
2. The noise output voltage (RMS value) is measured with a source impedance (R_S) of 500 Ω, unweighted and a bandwidth of 20 Hz to 20 kHz.
3. The ripple rejection is measured with the source impedance R_S = 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage (200 mV, RMS value) is applied to the positive supply rail.
4. The DC common-mode voltage range is limited to (V_P – 2.2) V.

* Value to be fixed.

TEST AND APPLICATION INFORMATION

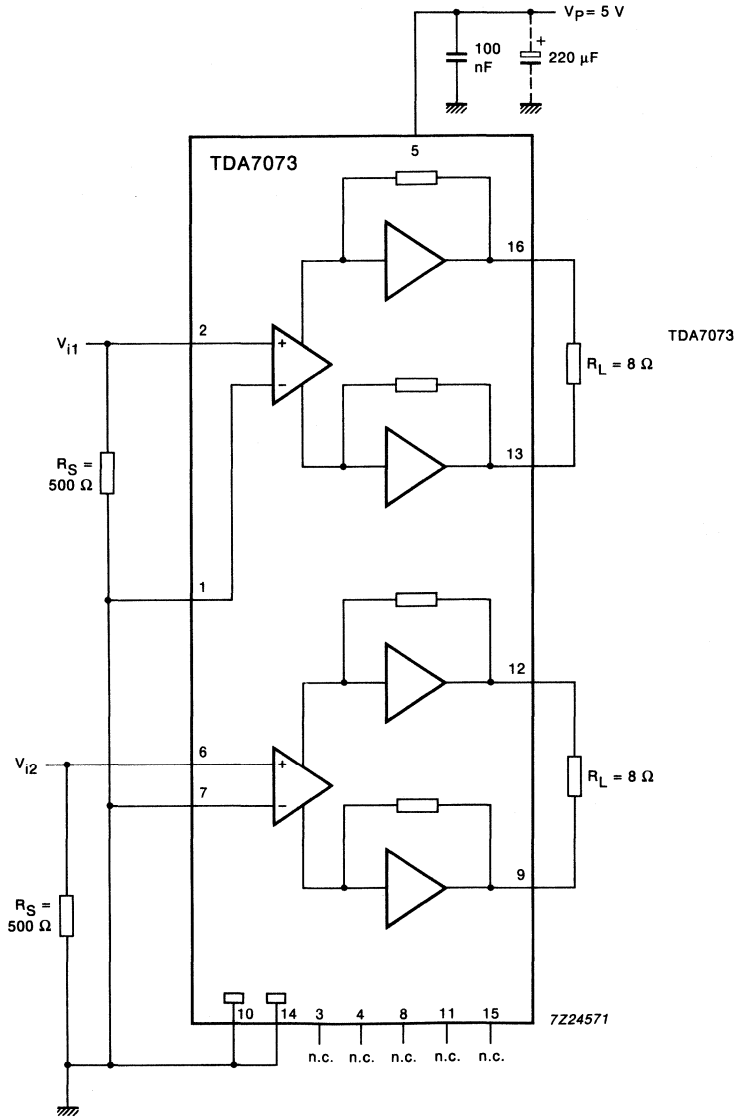


Fig.3 Test circuit diagram.

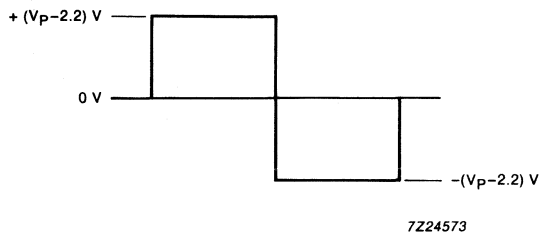


Fig.4 Maximum output voltage swing across R_L.

DEVELOPMENT DATA

TEST AND APPLICATION INFORMATION

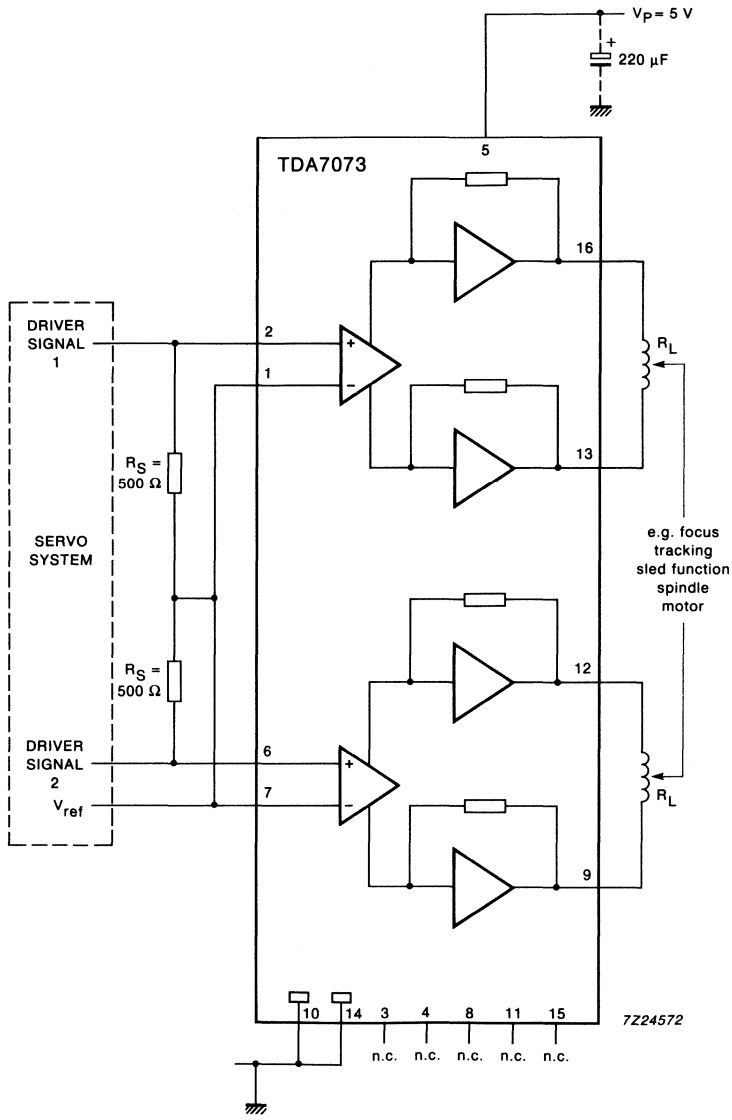


Fig.5 Application circuit diagram.

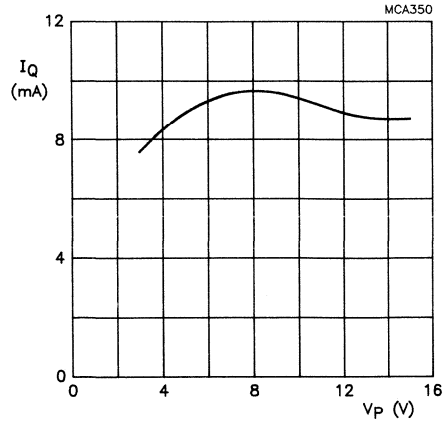


Fig.6 Quiescent current as a function of supply voltage; $R_L = \infty$.

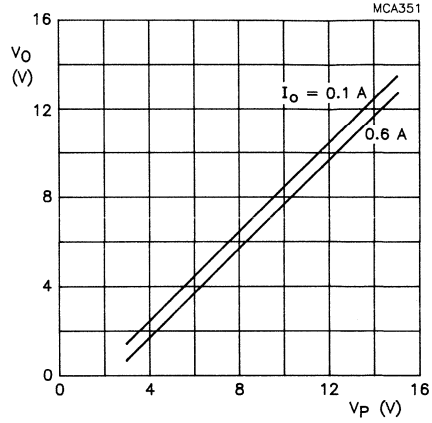


Fig. 7 Output voltage as a function of supply voltage.

DEVELOPMENT DATA

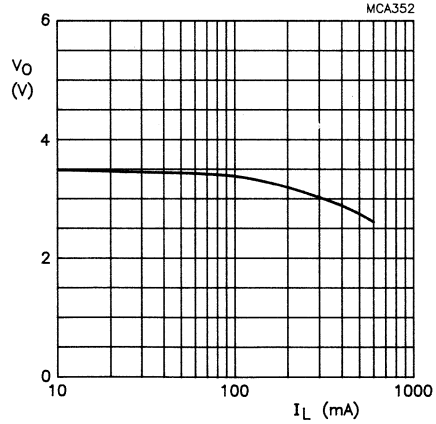


Fig.8 Output voltage as a function of output current; $V_P = 5$ V.

Data sheet	
status	Preliminary specification
date of issue	January 1991

TDA7088T
FM receiver circuit for battery supply

FEATURES

- Provided with all stages of a mono receiver from antenna to audio output
- Mute circuit
- Search tuning applicable with a single varicap diode
- Mechanical tuning with integrating AFC applicable
- AM application supported
- Power supply polarity protection
- Power supply voltage down to 1.8 V

GENERAL DESCRIPTION

The TDA7088T is a monolithic bipolar integrated circuit for mono portable and pocket radios, wherein a minimum of peripheral components (of small dimensions and low costs) are needed. The circuit is performed with a FLL system (frequency locked loop) and has an FM-IF of about 70 kHz. Selectivity is obtained by active RC-filters. Detuning referred to the IF and too weak input signals is suppressed by muting.

The circuit is applicable for mechanical as well as for electrical tuned radios. Whereas mechanical tuning is possible with or without integrating AFC circuit; electrical tuning is realized by one directional (band-up) search tuning facility, including RESET to the lower band limit.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 4)	1.8	3	5	V
I_P	supply current	4.2	5.2	6.6	mA
f_{iRF}	radio input frequency range	0.5	-	110	MHz
$V_{i\ (rms)}$	input sensitivity for –3 dB limiting (RMS value, mute disable) signal handling	- - 100	 3 200	 6 -	 µV mV
$V_{o\ (rms)}$	AF output signal (R_L = 22 kΩ)	-	85	-	mV
T_{amb}	operating ambient temperature	–10	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7088T	16	mini-pack	plastic	SOT109A

FM receiver circuit for battery supply

TDA7088T

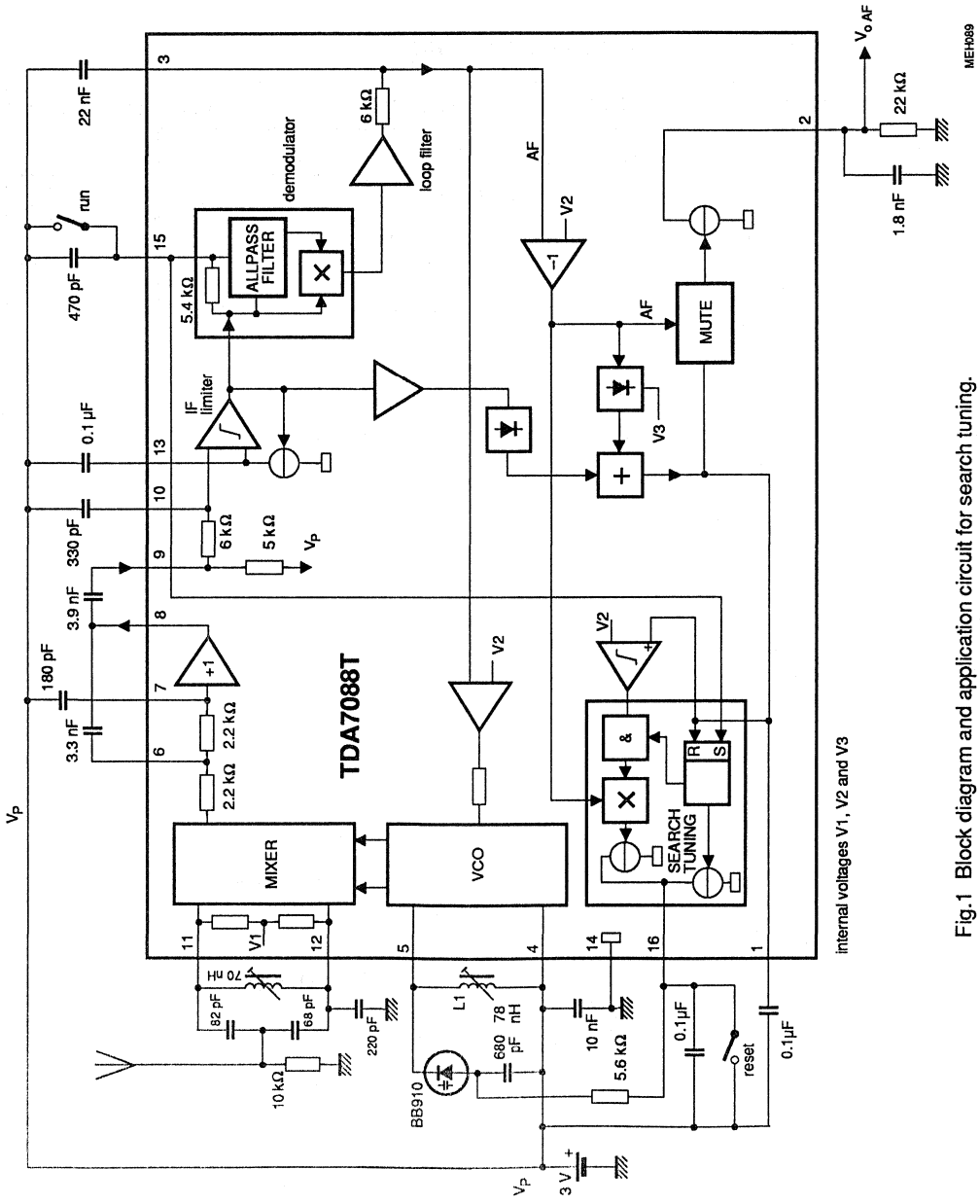


Fig.1 Block diagram and application circuit for search tuning.

FM receiver circuit for battery supply

TDA7088T

PINNING

SYMBOL	PIN	DESCRIPTION
MUTE	1	mute output
V_{oAF}	2	audio frequency output signal
LOOP	3	AF loop filter
V_P	4	+3 V supply voltage
OSC	5	oscillator resonant circuit
IFFB	6	IF feedback
C_{LP1}	7	low-pass capacitor of 1 dB amplifier
V_{oIF}	8	IF output to external coupling capacitor (high-pass)
V_{iIF}	9	IF input to limiter amplifier
C_{LP2}	10	low-pass capacitor of IF limitter amplifier
V_{iRF}	11	radio frequency input
V_{iRF}	12	radio frequency input
C_{LIM}	13	limiter offset voltage capacitor
GND	14	ground (0 V)
C_{AP}	15	all-pass filter capacitor / input for search tuning
TUNE	16	electrical tuning respectively AFC output

PIN CONFIGURATION

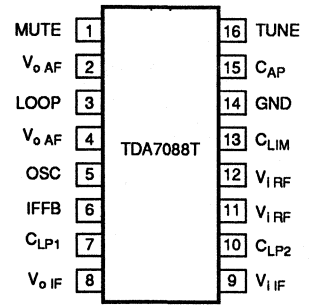


Fig.2 Pin configuration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 4)	0	5	V
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–10	+70	°C
V_{ESD}	electrostatic handling*		-	

* There is no special ESD protection circuit built in; ESD data on request.

FM receiver circuit for battery supply

TDA7088T

DC CHARACTERISTICS

V_P = 3 V and T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 4)		1.8	3	5	V
I_P	supply current		4.2	5.2	6.6	mA
V_1	DC voltage		2.50	2.55	2.60	V
V_3	DC voltage		2.64	2.69	2.74	V
$V_{6,7}$	DC voltage		2.38	2.44	2.50	V
V_8	DC voltage		1.60	1.67	1.74	V
$V_{9,10,13}$	DC voltage		2.42	2.47	2.52	V
$V_{11,12}$	DC voltage		0.91	0.94	0.98	V
V_{15}	DC voltage		2.06	2.12	2.18	V
V_{16}	DC voltage		t.b.n.	-	-	V
I_2	AF output current		45	60	80	µA
I_5	oscillator current		275	375	500	µA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C ; f_{iRF} = 96 MHz modulated with f_{mod} = 1 kHz and ±22.5 kHz deviation;
EMF = 400 µV (R_S = 75 Ω) and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i\,RF}$	input sensivity at –3 dB before limiting					
	(RMS value, pins 11–12, Fig.4)	mute-off	-	3	6	µV
	input sensivity	–3 dB muting	3	6	12	µV
		S/N = 26 dB	-	5	10	µV
	signal handling (RMS value, pins 11–12)	Δf = ±75 kHz; THD < 10%	100	200	-	mV
S/N	signal-to-noise ratio	Fig.4	52	56	-	dB
THD	total harmonic distortion	Δf = ±22.5 kHz	-	1	1.4	%
		Δf = ±75 kHz	-	2.4	3.3	%
α_{AM}	AM suppression:	FM: 1 kHz; ±75 kHz				
		AM: 1 kHz; m = 0.8	47	52	-	dB
RR_{1000}	ripple rejection, measurements taken with 100 mV (RMS) ripple on V_P	f = 1 kHz	7	10	-	dB
V_o	audio output signal (RMS value, pin 2)	R_L = 22 kΩ	60	85	120	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Search tuning with BB910 (Fig.1)		C_{16} = 0.1 µF				
V_{16}	minimum output voltage	limiting point	-	V_P–1.85	-	V
$\Delta V/\Delta t$	tuning steepness	voltage pin 16	95	210	420	mV/s
$\Delta f_{osc}/\Delta t$	oscillator steepness		1.25	2.83	5.6	MHz/s
$\Delta I_{AFC}/\Delta V_3$	AFC steepness	voltage pin 3	4.75	9.5	19	µA/V

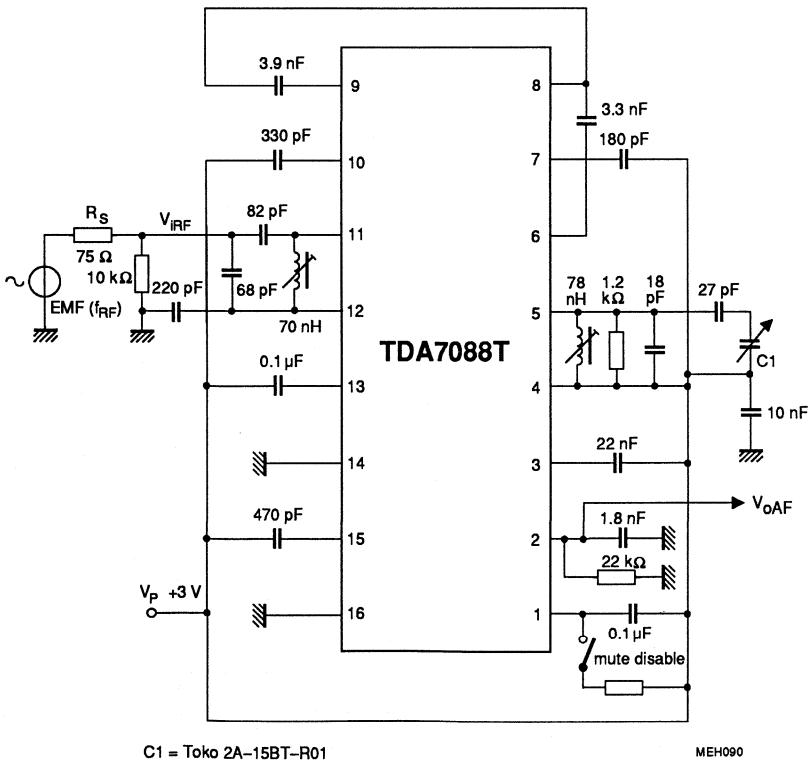


Fig.3 Test circuit and application for mechanical tuning.

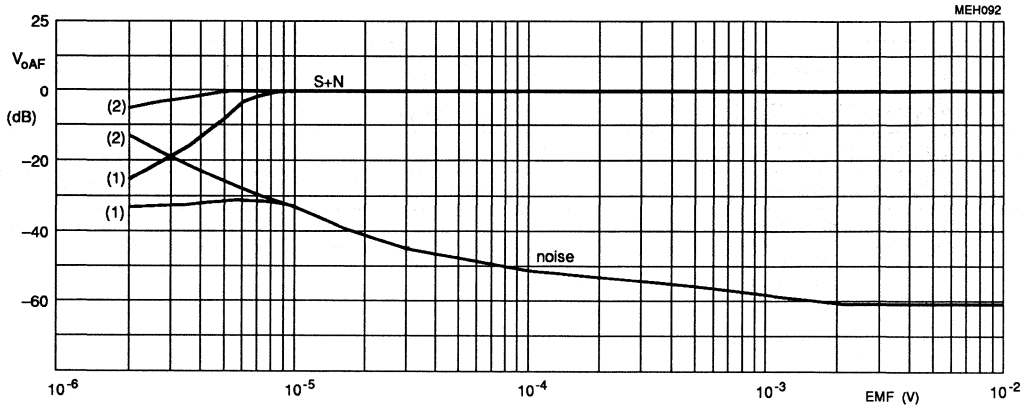


Fig.4 Input sensitivity: (1) mute-on; (2) mute-off.

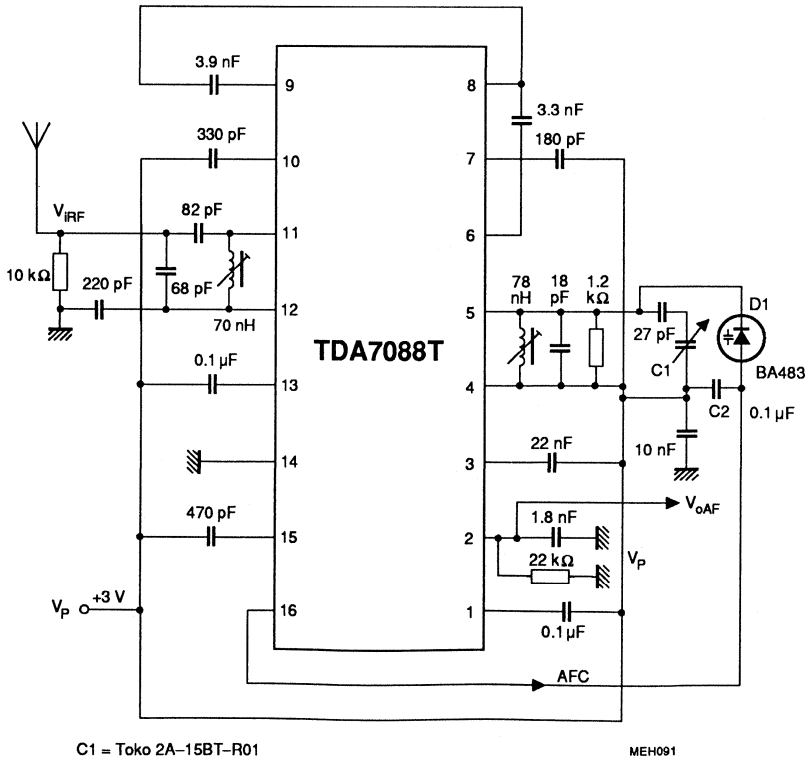


Fig.5 Application circuit with AFC for mechanical tuning.

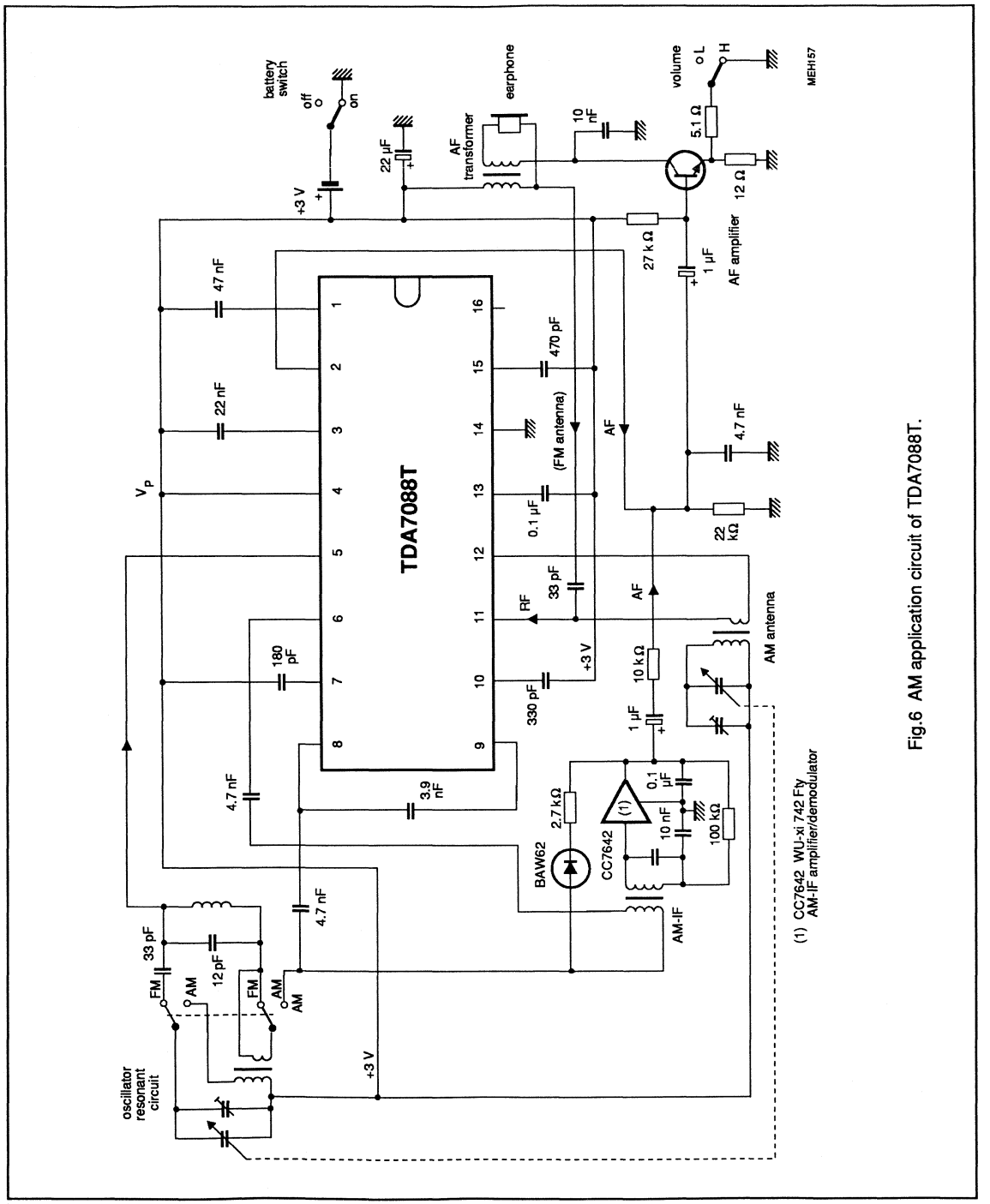


Fig.6 AM application circuit of TDA7088T.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

I²C-BUS INTERFACE FOR COLOUR DECODERS

GENERAL DESCRIPTION

The TDA8442 provides control of four analogue functions and has one high-current and two switching outputs. Control of the IC is performed via the two-line, bidirectional I²C-bus.

Features

- Four analogue control outputs
- One high-current output port (npn open emitter)
- Two switching output ports (npn collector with internal pull-up resistor)
- I²C-bus slave receiver
- Power-down reset

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	10.8	12.0	13.2	V
Supply current	no outputs loaded	I_P	8	13	18	mA
Total power dissipation	no outputs loaded	P_{tot}	–	–	1	W
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

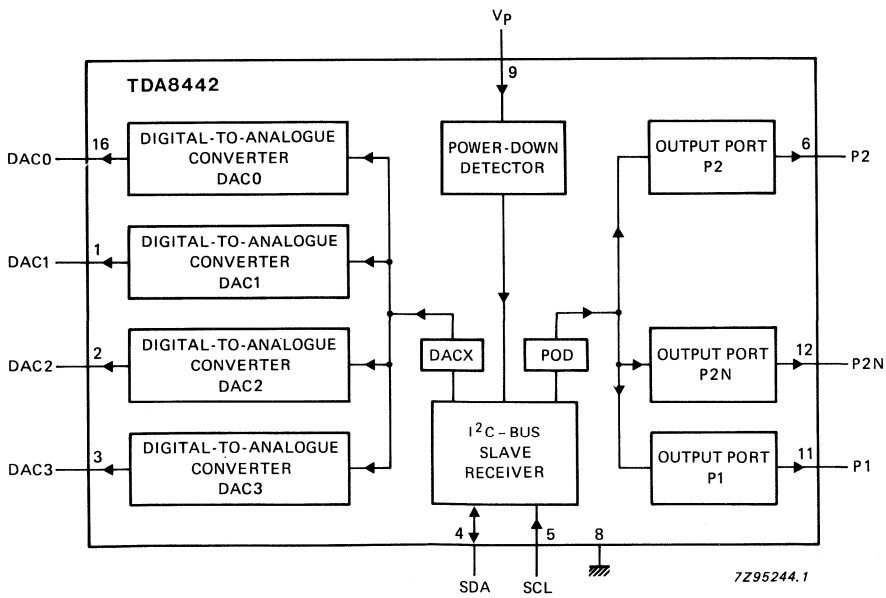


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

OCTUPLE 6-BIT DAC WITH I²C-BUS

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

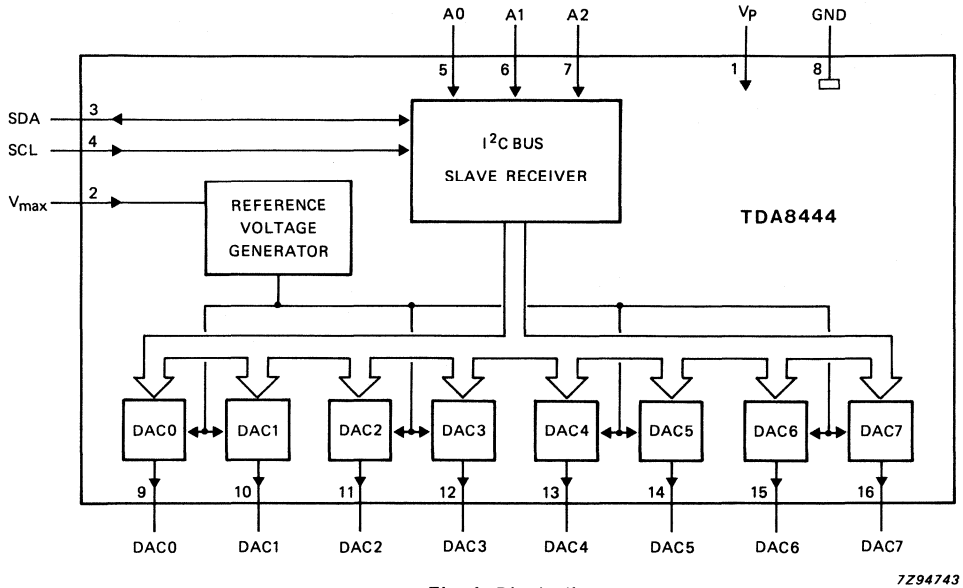


Fig. 1 Block diagram.

PINNING

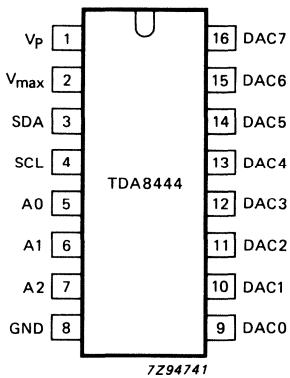


Fig. 2 Pinning diagram.

1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I^2C-bus serial data input/output
4	SCL	I^2C-bus serial data clock
5	A0	programmable address bits for I^2C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	Si/$\overline{RD}$ = 0 V	I_Q	7,5	10	12,5	mA
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
LF input current (for each diode input)		I_D	0	–	6	μA
Laser supply output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

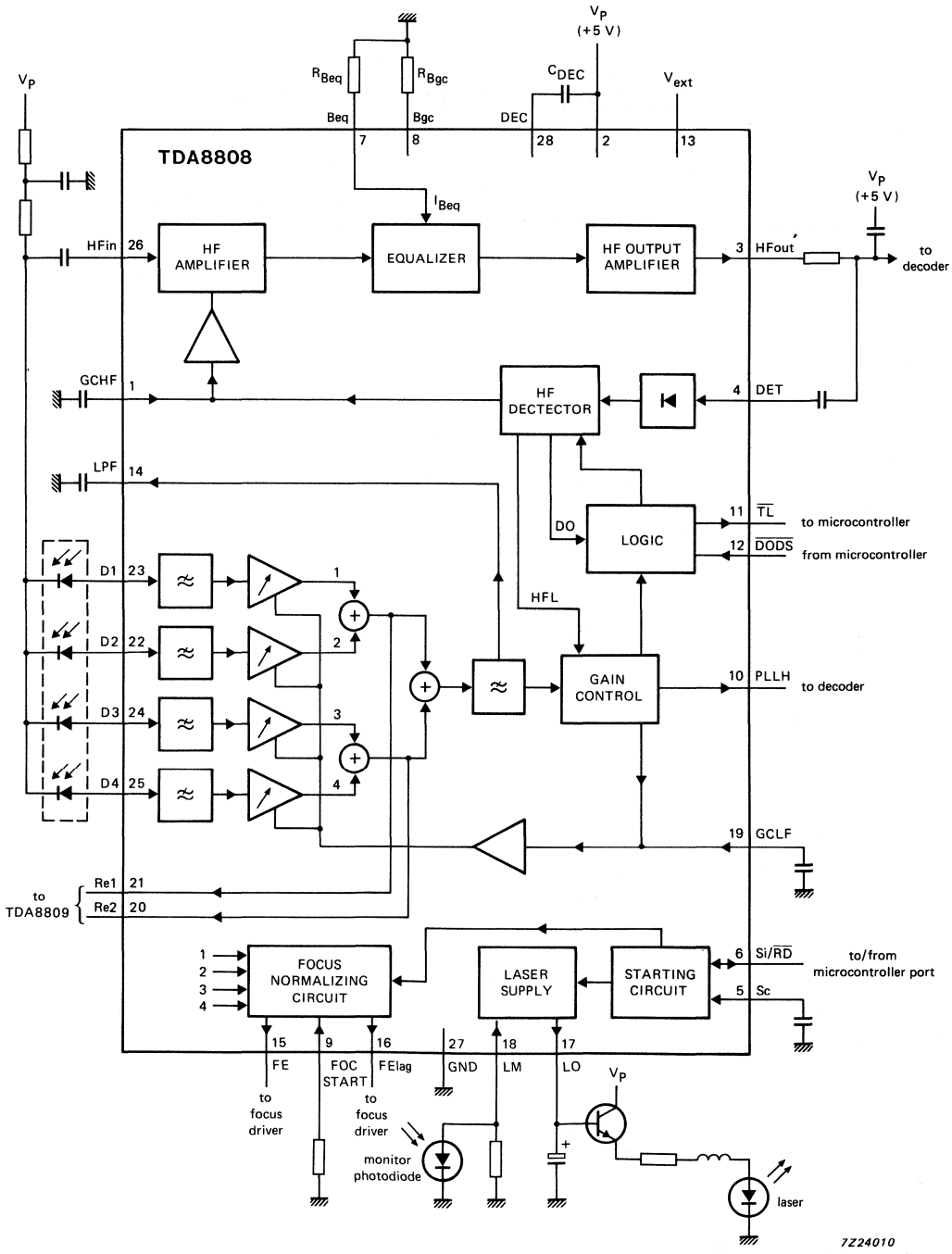


Fig. 1 Block diagram.

PINNING

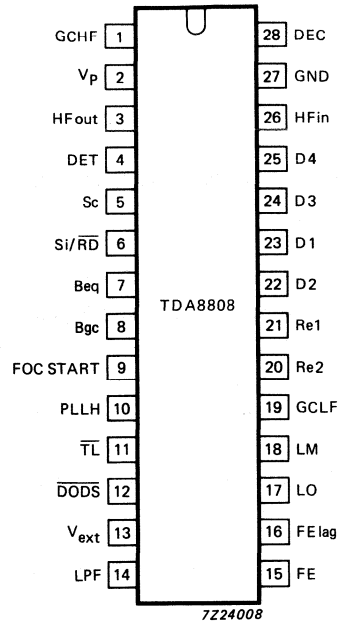


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Pin functions

pin	mnemonic	description
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V_P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T Negative supply connection for FE and FElag output stage; also substrate connection TDA8808AT Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
TDA8808T				
pin 2 to pin 13	$V_P - V_{(ext)}$	−0,3	13	V
pin 27 to pin 13	$V_{GND} - V_{(ext)}$	−0,3	13	V
TDA8808AT				
pin 13 to 27	$V_{ext} - V_{GND}$	−0,3	13	V
pin 2 to pin 27	$V_P - V_{GND}$	−0,3	13	V
Output voltage ranges				
except FE and FE_{lag}	V_O	0	V_P	V
FE and FE_{lag} (TDA8808T)	V_O	V_{ext}	V_P	V
FE and FE_{lag} (TDA8808AT)	V_O	V_{GND}	V_{ext}	V
LM (open loop)	V_O	V_{GND}	V_P	V
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

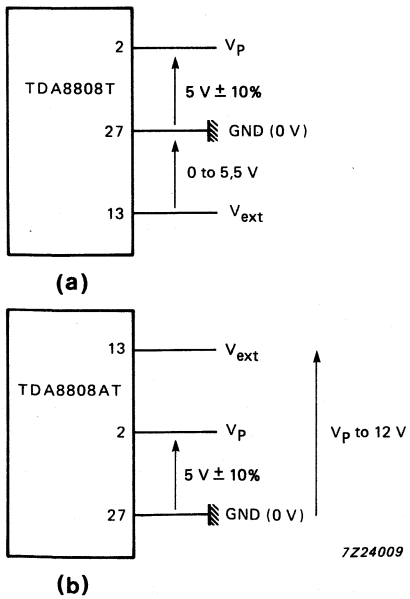


Fig. 3 Supply voltages; (a) TDA8808T (b) TDA8808AT.

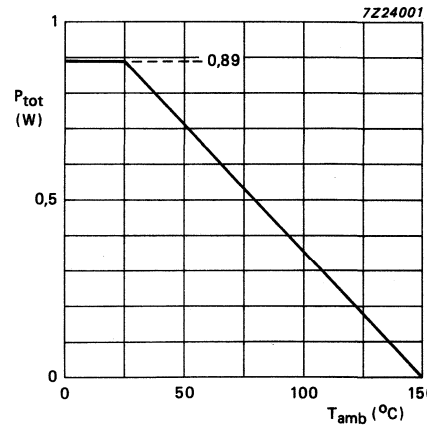


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; V_{ext} = –5 V (TDA8808T); V_{ext} = + 10 V (TDA8808AT); $V_{RE1} = V_{RE2}$ = 3,5 V; $V_{FE} = V_{FElag}$ = 0 V (TDA8808T); $V_{FE} = V_{FElag}$ = 5 V (TDA8808AT); $R_{FOC\ START}$ = 3,3 kΩ; $I_{Beq} = I_{Bgc}$ = 50 μA (current sources); T_{amb} = 25 °C; all voltages measured with respect to V_{GND}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	–5,5	–5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	$V_{Si/\overline{RD}}$ = 0 V	I_Q	7,5	10	12,5	mA
Reference input (Beq)						
Input voltage level		V_{Beq}	500	560	620	mV
Input current		I_{Beq}	–	–50	–	μA
Reference input (Bgc)						
Input voltage level		V_{Bgc}	1,15	1,25	1,35	V
Input current		I_{Bgc}	–	–50	–	μA
Decoupling input (DEC)						
Input voltage level		V_{DEC}	–	V_P–1,4	–	V
Input impedance		$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
HF input (HFin)						
Input voltage level		V_{HFin}	–	1,4	–	V
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance		$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$	I_{HFin} = ± 1 μA					
Maximum gain	V_{GCHF} = 4 V	G1(max)	390	480	570	mV/μA
Minimum gain	V_{GCHF} = 1,5 V	G1(min)	–5	0	5	mV/μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
HF part (continued)						
AC characteristics						
Gain (G2) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 1	G2	2	3,5	5	dB
Gain (G3) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 2	G3	4	5,5	7	dB
Phase of input/output signal at 1 MHz	note 3	ϕ	–	$\pi/2$	–	rad.
Group delay at f_{HFin} = 300 kHz + Δf	note 3	$\tau 300$	–	290	–	ns
Flatness between 0,1 and 1 MHz	note 3	$\Delta\tau$	*	9	*	ns
HF output (HFout)						
Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	V_{HFout}	1,5	2,4	3,3	V
Output voltage (peak-to-peak value)						
at $I_{HFin(p\text{-}p)}$ = 7 μA	note 4	$V_{O1(p\text{-}p)}$	1	1,20	–	V
at $I_{HFin(p\text{-}p)}$ = 4 to 10 μA	note 5	$V_{O(p\text{-}p)}$	–20%	M_1	+20%	V
Output impedance		$\lvert Z_{HFout}\rvert$	–	60	–	Ω
HF detector input (DET)	see Fig. 5					
DC voltage level	I_{DET} = 0	V_{DET0}	–	2,2	–	V
Positive reference voltage V_{DET} to V_{DET0}		V_{refp}	–10%	540	+10%	mV
Negative reference voltage V_{DET} to V_{DET0}		V_{refn}	–5%	$-V_{refp}$	+5%	mV
Input impedance		$\lvert Z_{DET}\rvert$	–	9	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (GCHF)						
Input voltage for:						
minimum HF gain		V_{GCHF}	–	1,8	–	V
maximum HF gain		V_{GCHF}	–	3,4	–	V
Input impedance						
at V_{GCHF} = 1,5 to 4 V		$\lvert Z_{GCHF}\rvert$	–	25	–	MΩ
Output current (see Fig. 5)						
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	90	100	110	μA
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	86	96	106	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	−0,65	−0,35	−0,2	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	−5,0	−4,4	−3,8	μA
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X*	I_{GCHF}	−0,65	−0,35	−0,2	μA
V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}			10	12,5	15	%
PLLH output (pin 10)						
Output voltage LOW						
I_{PLLH} = 400 μA (sink current)		V_{PLLHL}	–	–	0,4	V
Output voltage HIGH						
I_{PLLH} = −50 μA (source current)		V_{PLLHH}	2,4	–	–	V
Output sink current		I_{PLLH}	0,5	1,5	–	mA
Output source current		I_{PLLH}	–	−100	−50	μA
Threshold total LF current	V_{GCLF} = 3,5 V	I_{DT1}	–	2,0	–	μA
V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25)						
(values given for each input)						
DC voltage level		V_D	–	1,2	–	V
Input current range		I_D	0	–	6	μA
Input impedance at 1 MHz	I_D = 1 μA	$\lvert Z_D\rvert$	–	10	–	kΩ

* X = don't care.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain						
Maximum DC gain						
for: $A_1 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 3,5 V					
at I_{D1} = 0 μA; I_{D2} = 1 μA		A_{11}	S_1–10%	S_1	S_1	
at I_{D1} = 1 μA; I_{D2} = 0 μA		A_{12}	S_1 or 55	S_1	S_1	
for: $A_2 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 3,5 V					
at I_{D3} = 0 μA; I_{D4} = 1 μA		A_{21}	S_1–10%	S_1	S_1	
at I_{D3} = 1 μA; I_{D4} = 0 μA		A_{22}	S_1 or 55	S_1	S_1	
S_1 mean value of A_{11}, A_{12}, A_{21}, A_{22}			55	64	84	
Minimum DC gain						
for: $A_3 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	V_{GCLF} = 0,8 V					
at I_{D1} = 0 μA; I_{D2} = 1 μA		A_{31}	S_2–1	S_2	S_2+1	
at I_{D1} = 1 μA; I_{D2} = 0 μA		A_{32}	S_2–1	S_2	S_2+1	
for: $A_4 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	V_{GCLF} = 0,8 V					
at I_{D3} = 0 μA; I_{D4} = 1 μA		A_{41}	S_2–1	S_2	S_2+1	
at I_{D3} = 1 μA; I_{D4} = 0 μA		A_{42}	S_2–1	S_2	S_2+1	
S_2 mean value of A_{31}, A_{32}, A_{41}, A_{42}			–0,1	0,7	3	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain (continued)						
AC gain for:						
$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$						
at $I_{D1} = 0$; $I_{D2(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 6	G_4	−4,5	−3	−1,5	dB
at $I_{D1(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D2} = 0$	note 6	G_4	−4,5	−3	−1,5	dB
$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$						
at $I_{D3} = 0$; $I_{D4(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 7	G_5	−4,5	−3	−1,5	dB
at $I_{D3(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D4} = 0$	note 7	G_5	−4,5	−3	−1,5	dB
Gain control (GCLF)						
Input voltage for:						
minimum LF gain		V_{GCLF}	–	1	–	V
maximum LF gain		V_{GCLF}	–	2,8	–	V
Input impedance		$\lvert Z_{GCLF} \rvert$	–	25	–	MΩ
Threshold total LF current	I_{DT3}		–	1,6	–	mA
Output current (see Fig. 7)						
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	I_{GCLF}	–	$-0,6\ I_{Bgc}$	± 10	μA
	$I_{DT} > I_{DT3}$; note 8	I_{GCLF}	S_6-10	S_6	S_6+10	μA
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		I_{GCLF}	–	$-0,2\ I_{Bgc}$	± 2	μA
Re1, Re2 outputs (pin 21, pin 20)						
Output current	V_{GCLF} = 3,5 V					
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$		I_{Re1}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re1}	–	0	–	μA
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$		I_{Re2}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re2}	–	0	–	μA
Output voltage						
pin 21		V_{Re1}	1	–	V_P	V
pin 20		V_{Re2}	1	–	V_P	V
Output impedance						
pin 21		$\lvert Z_{Re1} \rvert$	–	1	–	MΩ
pin 20		$\lvert Z_{Re2} \rvert$	–	1	–	MΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Reference current (I_{ret})						
$I_{ret} = I_{Re1} = I_{Re2}$	note	I_{ret}	200	220	240	μA
LPF output (pin 14)						
DC voltage level	note 9	V_{LPF}	$V_P-2,1$	$V_P-1,7$	$V_P-1,4$	V
Input impedance		$\lvert Z_{LPF}\rvert$	–	3	–	kΩ
FOC START input (pin 9)						
Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	I_{ST}	75	150	500	μA
	Si/$\overline{RD}$ = LOW	I_{ST}	–	0	–	μA
Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	V_{ST}	430	530	630	mV
	Si/$\overline{RD}$ = LOW	V_{ST}	−20	0	20	mV
FElag output (pin 16)	see Fig. 8					
Output voltage						
TDA8808T		V_{FElag}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FElag}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\lvert Z_{FElag}\rvert$	–	8	–	MΩ
Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V					
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FElag} = I_O$	−10	0	+10	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
FE output (pin 15)	see Fig. 8					
Output voltage						
TDA8808T		V_{FE}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FE}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\|Z_{FE}\|$	–	8	–	MΩ
Output current	note 10					
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-2S_1-134-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-4S_1-67-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-2S_1-134+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−20%	$-2S_1+67+I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FE} = S_6$	−20%	67	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−15%	$-S_6$	+15%	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−10	0	+10	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	I_{FE}	−5	0	+5	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{DODS}}$ logic input (pin 12)						
Switching levels						
input voltage LOW		$V_{\overline{DODS}}$	–	–	+0,8	V
input voltage HIGH		$V_{\overline{DODS}}$	+2	–	–	V
Input source current		$I_{\overline{DODS}}$	–35	–25	–15	μA
Starting input (Sc)	see Fig. 9					
Output voltage	Si/$\overline{\text{RD}}$ = LOW	V_{Sc}	–	0	–	V
Output voltage	S1/$\overline{\text{RD}}$ = HIGH Z	V_{Sc}	–	–	Vp–0,5	V
Output impedance		$\lvert Z_{Sc} \rvert$	–	*	–	MΩ
Output source current	Si/$\overline{\text{RD}}$ = HIGH Z; V_{Sc} = 1,5 V	I_{Sc}	–1,2	–1	–0,8	μA
Output sink current	Si/$\overline{\text{RD}}$ = LOW	I_{Sc}	0,5	1,2	2,0	mA
Si/$\overline{\text{RD}}$ logic input/output (pin 20)	see Fig. 9					
Voltage "forced LOW"	$I_{Si/\overline{RD}}$ = 400 μA; V_{Sc} = 2,5 V; $V_{GCLF} < 2{,}8$ V	$V_{Si/\overline{RD}}$	–	0,15	0,4	V
Switching levels						
input voltage LOW		$V_{Si/\overline{RD}}$	–	–	+0,8	V
input voltage HIGH Z	$I_{Si/\overline{RD}}$ = –5 μA	$V_{Si/\overline{RD}}$	2,4	2,8	–	V
Input source current LOW		$I_{Si/\overline{RD}}$	–35	–25	–15	μA
$\overline{\text{TL}}$ logic output (pin 11)	see Fig. 6					
Output voltage level LOW	$I_{\overline{TL}}$ = 400 μA; (sink current)	$V_{\overline{TL}}$	–	0,15	0,4	V
Output voltage level HIGH	$I_{\overline{TL}}$ = –50 μA; (source current)	$V_{\overline{TL}}$	2,4	–	–	V
Threshold total LF current	I_{DT2}		–	3,9	–	μA
Output voltage	DODS = HIGH (≥ 2,4 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{TL}$ logic output (continued)						
Output voltage	$\overline{DODS}$ = LOW ($\leqslant$ 0,8 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V
Output sink current	$V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	1	2,2	–	mA
Output source current	$V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	–100	–50	μA
Delay times (see Fig. 10)	see Fig. 6	$\tau 1$	7	8,5	10	μs
		$\tau 2$	$\tau 1$–15% or 6,5	–	$\tau 1$+ 5% or 10	μs
		$\tau 3$	7	8,5	10	μs
		$\tau 4$	$\tau 3$–10% or 7	–	$\tau 3$+10% or 10	μs
LO output (pin 17)						
Output voltage		V_{LO}	–	–	V_P – 0,5	V
Output impedance		$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current	Si/$\overline{RD}$ = LOW	I_{LO}	–10	–0,1	0	μA
Maximum output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	–8	–4	–2	mA
LM input (pin 18)						
Input voltage	closed loop	V_{LM}	185	205	225	mV
Input bias current		I_{LM}	–2	–	–	μA
Laser supply						
Transconductance						
For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	G_{LDC}	–	0,5	–	A/V
	Si/$\overline{RD}$ = LOW	G_{LDC}	–	0	–	A/V
For AC (note 12) delay time		τLO	–	*	–	ns

* Value to be fixed.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)}$ = 1 μA; V_{GCHF} = 4 V.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50$ kHz.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.
4. HF part output vpltage for closed loop conditions; f_{HFin} = 500 kHz.
5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.
6. P_1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
7. P_2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
8. S_6, is the measured value of $S_1 \cdot \frac{I_{DT}}{4} - 1{,}1\ I_{Bgc}$

   Measurement taken at V_{GCLF} = 3,5 V.
9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.
10. FE output current measured at V_{GCLF} = 3,5 V and Si/$\overline{RD}$ = HIGH Z; $I_{ST} = \frac{V_{FOC\ START}}{R_{FOC\ START}}$.
11. Laser supply transconductance for DC

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2$ mA).
12. Laser supply transconductance for AC

    $G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$

    Where: S is the laplace operator in the frequency domain.

DEVELOPMENT DATA

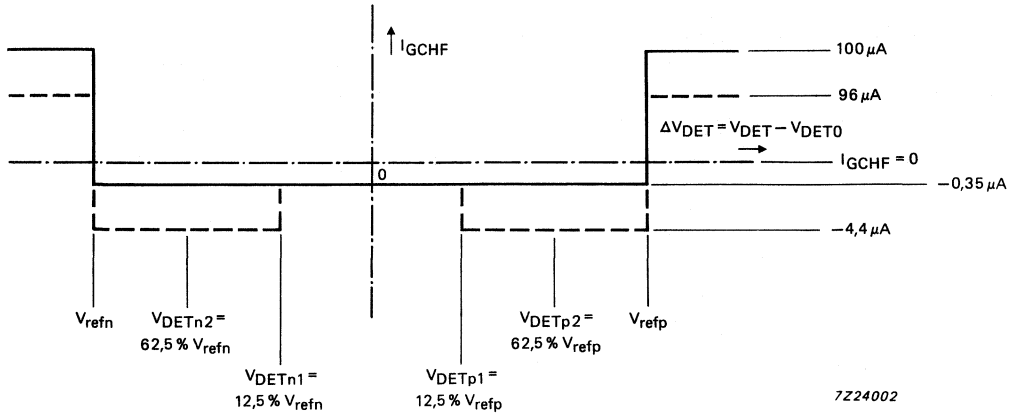
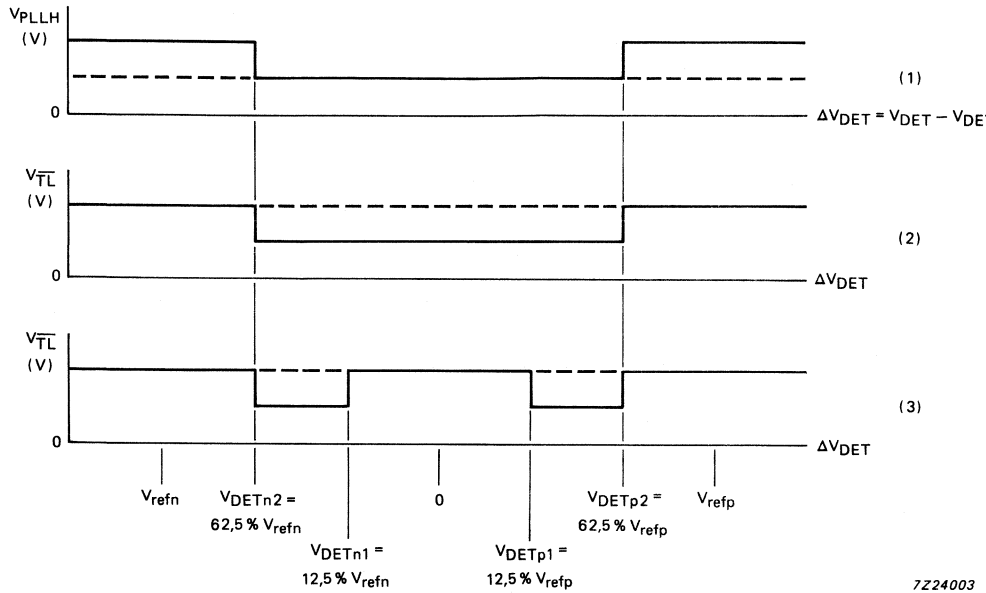


Fig. 5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.



DEVELOPMENT DATA

(1)

——— $I_{DT} > I_{DT1}$

--------- $I_{DT} < I_{DT1}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$

$I_{DT2} = 5\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(2)

——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = LOW

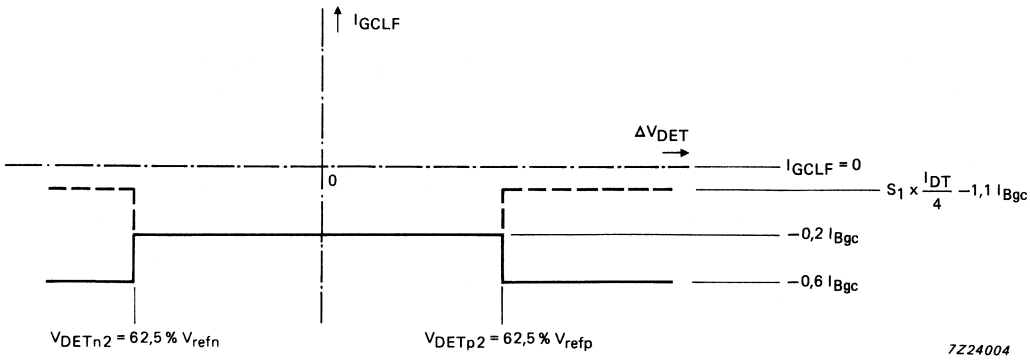
(3)

——— $I_{DT} > I_{DT2}$

--------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = HIGH

Fig. 6 $\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.



---------- $I_{DT} > I_{DT3}$

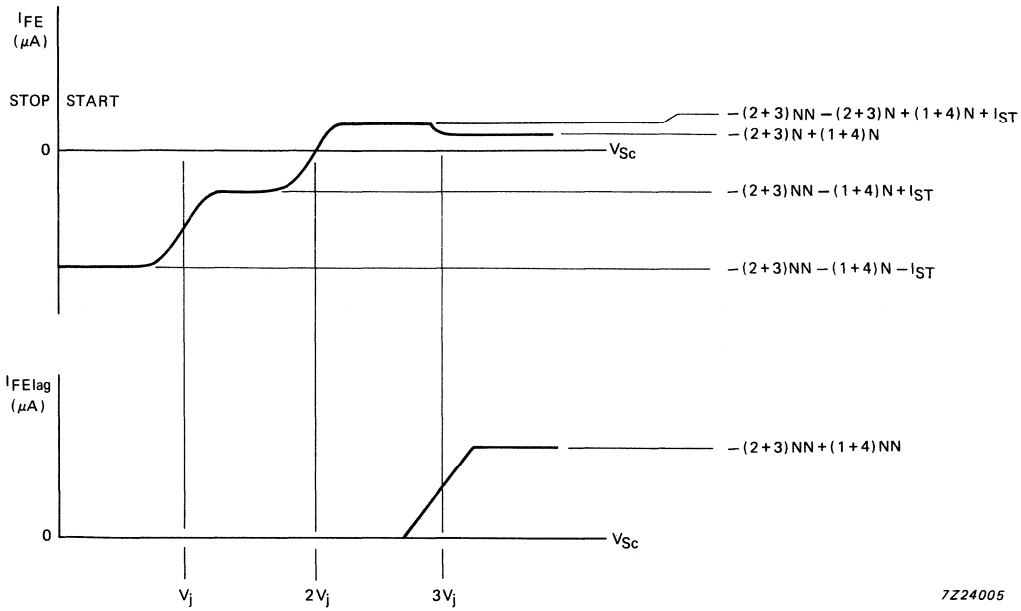
——— $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig. 7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.



DEVELOPMENT DATA

I_{ST} = $-I_{FOC\ START}$

I_{cont} = $2\ I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} = $I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} = $I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} = $2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(1 + 4)NN = not normalized currents = $(I_{D1} + I_{D4})\ S_1$

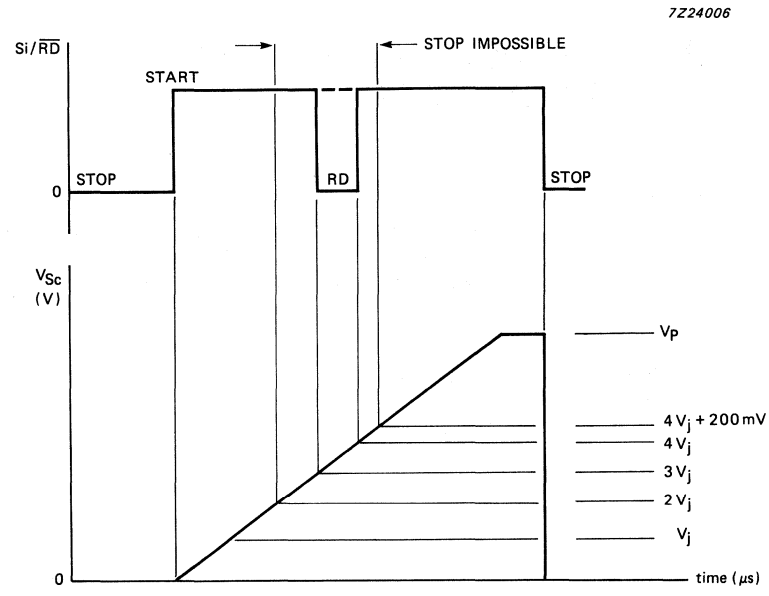
(2 + 3)NN = not normalized currents = $(I_{D2} + I_{D3})\ S_1$

(1 + 4)N = normalized currents = $\left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

(2 + 3)N = normalized currents = $\left(\frac{I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D3}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig. 8 FElag current output as a function of starting voltage input (V_{Sc}).



RD : Si/$\overline{RD}$ forced LOW for ready signal

——— $V_{GCLF} < 2{,}8$ V

--------- $V_{GCLF} > 3{,}5$ V

V_j is the junction voltage (0,7 V typ.)

Fig. 9 Si/$\overline{RD}$ signal as a function of V_{Sc}.

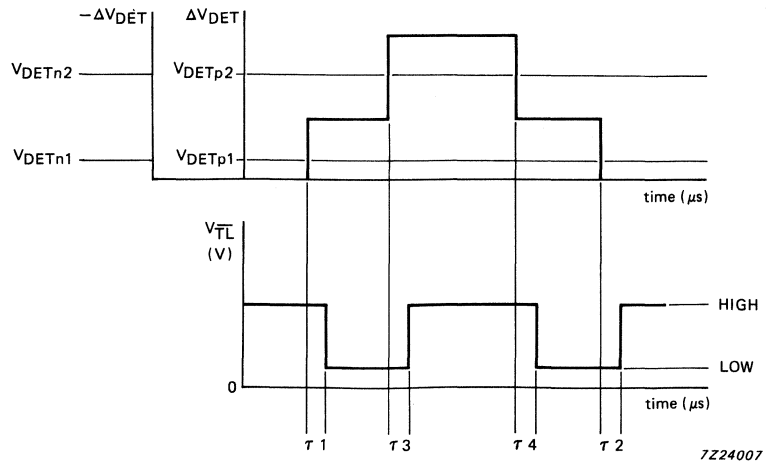


Fig. 10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.

RADIAL ERROR SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8809T is a bipolar integrated circuit which provides control signals for the radial motor. These control signals are generated from radial error signals received from a photo-diode signal processor (TDA8808), and velocity control signals from the control processor.

Features

- Tracking error processor with automatic asymmetry control
- AGC circuitry with automatic start-up and wobble generator
- Tracking control for fast forward/reverse scan, search, repeat and pause functions
- Radial polarity - 4 - tracks counting
- Possibility for car, home and portable applications

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	–	5,3	–	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

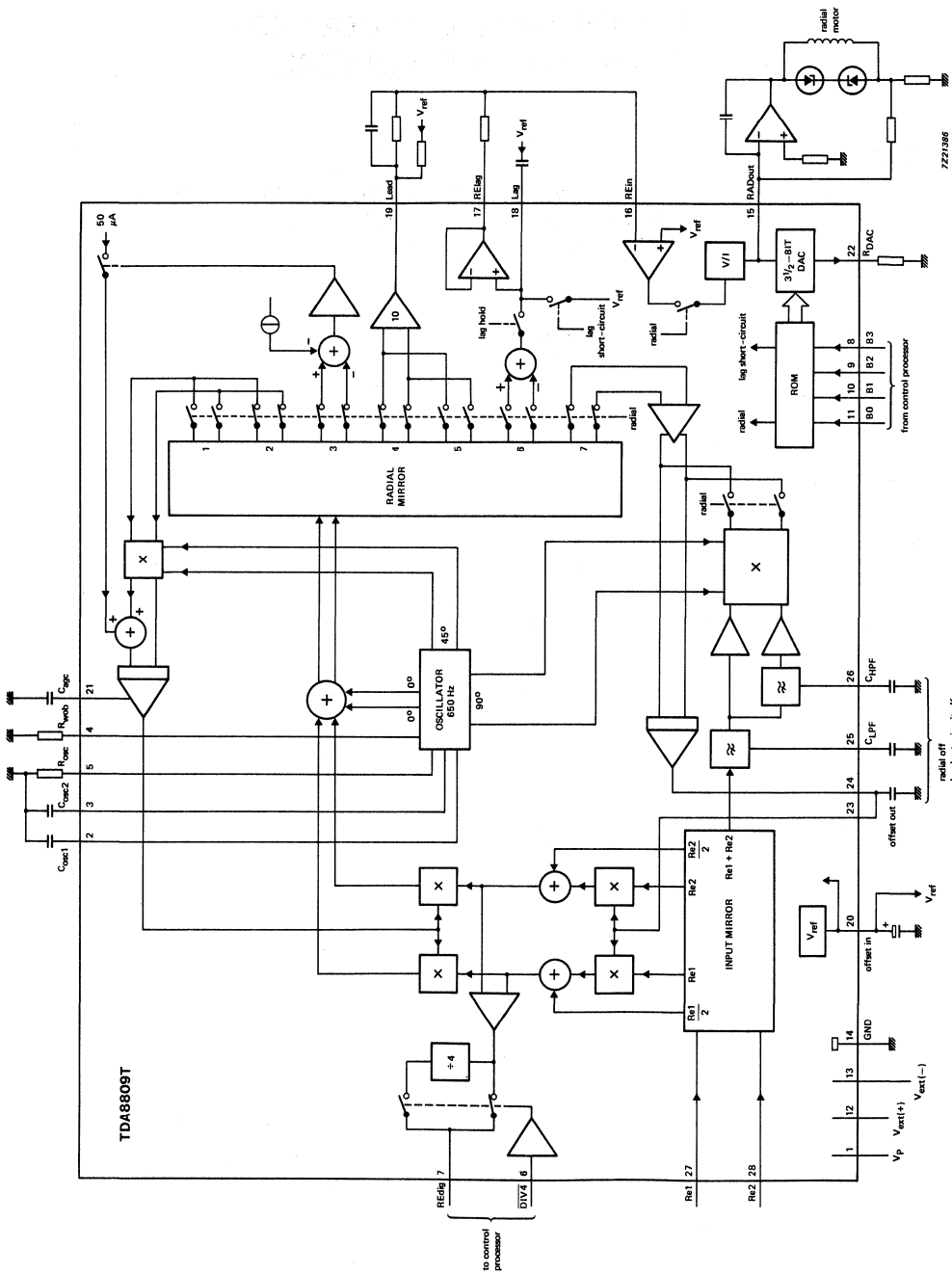


Fig. 1 Block diagram.

PINNING

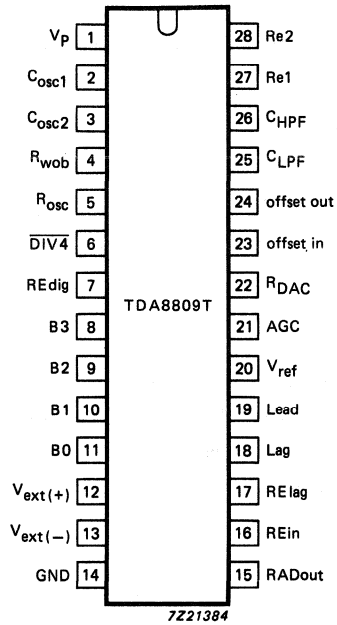


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Pin functions

pin	mnemonic	description
1	V_P	Positive supply voltage
2	C_{osc1}	Frequency setting capacitors for oscillator
3	C_{osc2}	
4	R_{wob}	Wobble generator input
5	R_{osc}	Biassing resistor for oscillator frequency and internal amplitude
6	$\overline{DIV4}$	Divide-by-4 input
7	REdig	Digital output of sign (Re2 - Re1)
8	B3	Input control bits for off-, catch-, play-status and DAC output current
9	B2	
10	B1	
11	B0	
12	$V_{ext(+)}$	Positive external voltage input
13	$V_{ext(-)}$	Negative external voltage input (also substrate connection)
14	GND	Negative supply connection
15	RADout	Current output of amplified (Re2 - Re1) input currents
16	REin	Radial error input
17	RElag	Voltage output of integrated (Re2 - Re1) input currents
18	Lag	Connection of integrator capacitor for (Re1 - Re2) input currents
19	Lead	Lead output
20	V_{ref}	Internal reference voltage output
21	AGC	Gain control input for radial error signal
22	R_{DAC}	Biassing resistor for current output for track jumping (3½ bits)
23	offset in	Offset control input for radial offset
24	offset out	Offset control output for radial offset
25	C_{LPF}	Low-pass filter for Re1 and Re2, used for radial offset control
26	C_{HPF}	High-pass filter for Re1 and Re2, used for radial offset control
27	Re1	Input for amplified currents from photo-diodes D1 and D2
28	Re2	Input for amplified currents from photo diodes D3 and D4

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
pin 1 to pin 14	V_P	−0,3	13	V
pin 12 to pin 13	V_{ext}	−0,3	13	V
pin 14 to pin 13	$V_{ext(-)}$	−0,3	13	V
Output voltage ranges				
except RADout	V_O	0	V_P	V
RADout	V_O	$V_{ext(-)}$	$V_{ext(+)}$	V
R_{DAC} current range	I_{RDAC}	50	250	μA
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+150	°C
Operating ambient temperature range	T_{amb}	−30	+85	°C
Operating junction temperature	T_j	−	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

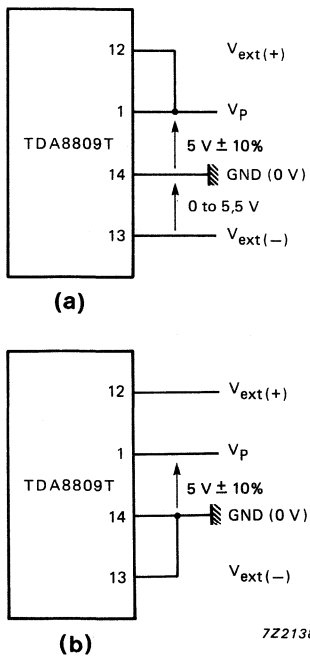


Fig. 3 Supply voltages;
(a) Home application (b) Car application.

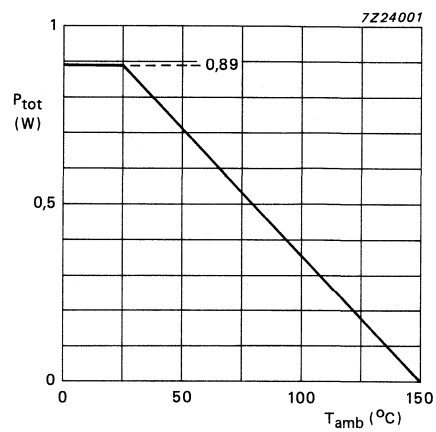


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; $V_{ext(+)}$ = + 5 V; $V_{ext(-)}$ = −5 V; I_{RDAC} (pin 22) = −75 μA; I_{Rwob} (pin 4) = −8 μA; I_{Rosc} (pin 5) = −50 μA; V_{RADout} = 0 V; $V_{offset\ in}$ = V_{lead} = V_{lag} = V_{Cosc1} = V_{Cosc2} = V_{ref}; $V_{offset\ in}$ is connected to $V_{offset\ out}$; T_{amb} = 25 °C; all voltages measured with respect to V_{GND}; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range (see Fig. 3)						
pin 12		$V_{ext(+)}$	V_P	10	12	V
pin 13		$V_{ext(-)}$	−5,5	−5,0	0	V
pin 12 to pin 13		$V_{ext(+)} - V_{ext(-)}$	4,5	–	12	V
Supply current		I_P	4,0	5,3	6,6	mA
Reference output (V_{ref})						
Output voltage	$I_{Vref} \leqslant \pm 1$ mA	V_{ref}	2,25	2,45	2,65	V
Output impedance		$\lvert Z_O \rvert$	–	25	–	Ω
Reference input (R_{osc})						
Input voltage level	I_{Rosc} = −50 μA	V_{Rosc}	1,1	1,24	1,3	V
Input current		I_{Rosc}	–	−50	–	μA
Reference input (R_{DAC})						
Input voltage level	I_{RDAC} = −75 μA	V_{RDAC}	1,1	1,23	1,3	V
Input current		I_{RDAC}	–	−75	–	μA
Reference input (R_{wob})						
Input voltage level	I_{Rwob} = −8 μA	V_{Rwob}	150	165	180	mV
Input current		I_{Rwob}	–	−8	–	μA
REdig output (REdig)						
Output source current	note 1 (A)	I_{REdig}	–	−160	−50	μA
Output sink current	note 1 (B)	I_{REdig}	0,4	3,5	–	mA
Output voltage HIGH	I_{REdig} = −50 μA; note 1 (A)	V_{REdig}	2,4	–	–	V
Output voltage LOW	I_{REdig} = 400 μA; note 1 (B)	V_{REdig}	0	0,13	0,4	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Digital inputs						
B0, B1, B2 and B3						
Input voltage HIGH	note 2	V_{IH}	2,0	–	V_P	V
Input voltage LOW	note 2	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	0,03	1,0	μA
Input source current LOW		I_{IL}	−3,0	−0,1	0	μA
Divide-by-4 input ($\overline{DIV4}$)						
Input voltage HIGH	divide-by-1	V_{IH}	2,0	–	V_P	V
Input voltage LOW	divide-by-4	V_{IL}	0	–	0,8	V
Input sink current HIGH		I_{IH}	0	5,0	*	μA
Input source current LOW		I_{IL}	−10	−3	0	μA
Input frequency at Re1 and Re2		f_i	–	10	50	kHz
Radial error inputs (Re1; Re2)						
Input voltage level	$I_{Re1} = I_{Re2} = -110\,\mu A$	V_{Re1}, V_{Re2}	$V_P-1,81$	$V_P-1,71$	$V_P-1,61$	V
Input current		I_{Re1}, I_{Re2}	–	−110	–	μA
Input impedance		$\lvert Z_{Re1}\rvert, \lvert Z_{Re2}\rvert$	–	2,5	–	kΩ
Gain control input (AGC)	rad on; lag hold off					
Offset current	$V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = 0$	I_{AGC}	−0,2	0	0,2	μA
Lag current for	$I_{Re1} = -85\,\mu A$; $I_{Re2} = -115\,\mu A$					
minimum radial gain	$V_{AGC} = 0,6$ V	I_{lag}	−2,5	−0,45	+ 1,5	μA
maximum radial gain	$V_{AGC} = 3,8$ V	I_{lag}	−42	−30	−18	μA
Input impedance		$\lvert Z_{AGC}\rvert$	–	*	–	MΩ
Gain	$V_{AGC} = 3,8$ V; $V_{Cosc2} = V_{ref} + 1,4$ V; $V_{Cosc1} = V_{ref}$; $I_{Re1} = -100\,\mu A$; $I_{Re2} = -100\,\mu A$	I_{AGC0}	–	−2	–	μA
	$I_{Re1} - I_{Re2} = 4\,\mu A - I_{AGC0}$ then $I_{Re1} - I_{Re2} = -4\,\mu A - I_{AGC0}$	$\frac{\Delta I_{AGC}}{\Delta(I_{Re1}-I_{Re2})}$	0,7	0,9	1,1	

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (continued)						
Radial error trackcrossing	rad off; V_{AGC} = 3,8 V $I_{Re2}-I_{Re1}$ = −12 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	−3	0	3	μA
	$I_{Re2}-I_{Re1}$ = −48 μA; $I_{Re2}+I_{Re1}$ = −200 μA	I_{AGC}	39	49	59	μA
Offset control (offset out)						
Offset current	rad on; I_{CHPF} = 0; $I_{Re1}=I_{Re2}$ = −110 μA	$I_{offset\ out}$	−0,1	0	0,1	μA
Offset lag current for	rad on; lag hold off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA					
minimum amplification Re1 maximum amplification Re2	$V_{offset\ in}$ = V_{ref} − 1,2 V	I_{lag}	−115	−100	−85	μA
minimum amplification Re2 maximum amplification Re1	$V_{offset\ in}$ = V_{ref} + 1,2 V	I_{lag}	+ 85	+100	+115	μA
Offset lag current	note 3	I_{lag}	−7	0	+ 7	μA
Transconductance factor						
	rad off; V_{AGC} = 3,8 V; $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot} = I_{Re1} + I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}$	0,17	0,21	0,25	$V_{range\ offset\ in}$
	rad off; $V_{AGC} = V_{GND}$ $I_{Re1}=I_{Re2}$ = −100 μA; $V_{range\ offset\ in}$ = 0,6 V (int.); $I_{tot} = I_{Re1} + I_{Re2}$	$\frac{\Delta I_{offset\ out}}{\Delta V_{offset\ in}.I_{tot}}$	−0,1	0	0,1	$V_{range\ offset\ in}$
Input impedance		$\lvert Z_{offset\ in}\rvert$	−	*	−	MΩ
High-pass filter (C_{HPF})						
Voltage level at I_{CHPF} = 0	$I_{Re1}=I_{Re2}$ = 0; I_{CLPF} = 0	V_{CHPF}	VP −0,82	VP −0,72	VP −0,62	V
Transresistance from Re1, Re2 to C_{HPF}	$I_{Re1}+I_{Re2}$ = −200 μA	$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}-I_{Re2})}$	−200	*	200	Ω
		$\frac{\Delta V_{CHPF}}{\Delta(I_{Re1}+I_{Re2})}$	6,2	8,8	11,5	kΩ
Input impedance		$\lvert Z_{CHPF}\rvert$	−	8	−	kΩ

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Low-pass filter (C_{LPF})						
Voltage level at $I_{CLPF} = 0$	$I_{Re1} = I_{Re2} = 0$	V_{CLPF}	4,7	–	V_P	V
Input impedance		$\|Z_{CLPF}\|$	–	8	–	kΩ
RElag output						
Output voltage range	$I_{RElag} = -200\ \mu A$; $V_{lag} = 4{,}25$ V	V_{RElag}	$V_P-1{,}1$	–	–	V
	$I_{RElag} = 200\ \mu A$; $V_{lag} = 0{,}9$ V	V_{RElag}	–	–	1,1	V
Maximum source current output	$V_{lag} = 4{,}1$ V	I_{RElag}	–6,0	–3,5	–1,0	mA
Maximum sink current output	$V_{lag} = 0{,}9$ V	I_{RElag}	2,5	4,1	5,5	mA
Output impedance	f = < 10 kHz	$\|Z_{RElag}\|$	–	–	50	Ω
Offset ($V_{RElag}-V_{ref}$)	lag short-circuit on; lag hold on	$V_{RElag\ offset}$	–10	–	10	mV
Transfer lag ⟶ RElag	f = < 10 kHz; lag short-circuit off; lag hold on	$\frac{V_{RElag}}{V_{lag}}$	–5%	1	5%	
Slew rate						
RElag output amplifier	lag short-circuit off; lag hold on	SR	–	0,4	–	V/μs
Lag push-pull current output, voltage input (pin 18)	note 4					
Output voltage	$I_{lag} = -20\ \mu A$; $V_{offset\ in} = V_{ref}-1{,}2$ V	V_{lag}	$V_P-1{,}5$	–	–	V
	$I_{lag} = 20\ \mu A$; $V_{offset} = V_{ref} + 1{,}2$ V	V_{lag}	–	–	1,5	V
Output impedance		$\|Z_{lag}\|$	–	*	–	MΩ
Switch lag short-circuit						
Impedance $\frac{\Delta V_{lag}}{\Delta I_{lag}}$	lag short-circuit on; lag hold on; $I_{lag} = \pm 100\ \mu A$	$\|Z_{lag\ sc}\|$	–	0,4	1	kΩ
Radial error input (REin)						
Input impedance	rad on	$\|Z_{REin}\|$	–	0	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RADout push-pull current output						
Output voltage	rad on I_{REin} = 180 μA; I_{RADout} = −50 μA	V_{RADout}	$V_{ext(+)}-1,5$	–	–	V
	I_{REin} = −180 μA; I_{RADout} = 50 μA	V_{RADout}	–	–	$V_{ext(-)}+1,5$	V
Current gain	rad on; I_{REin} = ± 100 μA	$\frac{I_{RADout}}{I_{REin}}$	−10%	1	10%	
Slew rate		SR	–	0,4	–	V/μs
Output impedance		$\lvert Z_{RADout} \rvert$	–	*	–	MΩ
Ratio of output current to reference current	I_{REin} = 0; I_{RDAC} = −75 μA; see also Table 1	$\frac{I_{RADout}}{I_{RDAC}}$	−5%	−0,5	+ 15%	
			−8%	−2	+ 12%	
			−0,02	0	0,02	
			−0,02	0	0,02	
			−14%	0,5	+ 6%	
			−12%	2	+ 8%	
			−0,1	0	0,1	
			−0,1	0	0,1	
			−5%	−0,5	+ 15%	
			−5%	−0,375	+ 15%	
			−5%	−0,25	+ 15%	
			−4%	−0,125	+ 16%	
			−14%	+ 0,5	+ 6%	
			−13%	+ 0,375	+ 7%	
			−13%	+ 0,25	+ 7%	
			−13%	+ 0,125	+ 7%	
Lead output	V_{AGC} = 3,8 V					
Output voltage	I_{Re1} = −90 μA; I_{Re2} = −100 μA; I_{lead} = −20 μA	V_{lead}	$V_P-1,5$	–	–	V
	I_{Re1} = −100 μA; I_{Re2} = −90 μA; I_{lead} = 20 μA	V_{lead}	–	–	1,5	V
Offset current	$I_{Re1} = I_{Re2}$ = −100 μA	$I_{lead\ offset}$	−100	0	100	μA

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Lead output (continued)						
Current gain	$I_{Re1} = -120\ \mu A$; $I_{Re2} = -100\ \mu A$	$\frac{\Delta I_{lead}}{\Delta(I_{Re1}-I_{Re2})}$	−11,2	−9,9	−8,8	
Output impedance		$\lvert Z_{lead}\rvert$	–	*	–	MΩ
Oscillator						
(C_{osc1} and C_{osc2} connected to 12 nF capacitors)						
Amplitude oscillation (peak-to-peak value)						
C_{osc1}		$V_{osc1(p-p)}$	1,05	1,25	1,45	V
C_{osc2}		$V_{osc2(p-p)}$	1,05	1,25	1,45	V
Operating frequency	$I_{Re1} = I_{Re2} = -110\ \mu A$	f_{osc}	690	740	790	Hz
Output voltages (peak-to-peak value)						
0° injection						
lead (pin 19)	$R_{lead} = 10\ k\Omega$	$V_{lead(p-p)}$	0,85	1,05	1,25	V
C_{lag} (pin 18)	$R_{lag} = 10\ k\Omega$; rad on; lag hold off	$V_{lag(p-p)}$	85	105	125	mV
	rad on; lag hold on	$V_{lag(p-p)}$	–	0	20	mV
90° injection						
offset out	$I_{CHPF} = -100\ \mu A$; $R_{offset\ out} = 10\ k\Omega$; rad on	$V_{offset\ out}$ (p-p)	90	110	130	mV
45° injection						
AGC	$R_{agc} = 10\ k\Omega$; $V_{offset\ in} = V_{ref} + 1\ V$; rad on	$V_{AGC(p-p)}$	200	250	300	mV

Notes to the characteristics

1. REdig output conditions:
   (A) $I_{Re1} > I_{Re2} + 5\ \mu A$; (B) $I_{Re2} > I_{Re1} + 5\ \mu A$.
2. Input voltage HIGH indicates logic 1; Input voltage LOW indicates logic 0; see also Table 1.
3. $\overline{DIV4}$ = HIGH; $V_{offset\ in}$ adjusted for $V_{REdig} = 1,4$ V; rad on; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$.
4. Output voltage conditions are:
   rad on; lag short-circuit off; lag hold off; $V_{AGC} = 3,8$ V; $I_{Re1} = I_{Re2} = -100\ \mu A$; $V_{offset} = V_{ref} - 1,2$ V.

Table 1 Truth table for DAC output current

functions	DAC output	logical inputs				internal switches		
	I_{REout}/I_{DAC}	B3	B2	B1	B0	lag s/c	rad	lag hold
PUSH	−1/2	0	0	0	0	off	off	on
(kick)	−2	0	0	0	1	off	off	off
OFF	0	0	0	1	0	off	off	on
OFF	0	0	0	1	1	on	off	off
PULL	1/2	0	1	0	0	off	off	on
(kick)	2	0	1	0	1	off	off	off
CATCH	0	0	1	1	0	off	on	on
PLAY	0	0	1	1	1	off	on	off
PUSH	−1/2	1	0	0	0	on	off	on
PUSH	−3/8	1	0	0	1	on	off	off
PUSH	−1/4	1	0	1	0	on	off	on
PUSH	−1/8	1	0	1	1	on	off	off
PULL	1/2	1	1	0	0	on	off	on
PULL	3/8	1	1	0	1	on	off	off
PULL	1/4	1	1	1	0	on	off	on
PULL	1/8	1	1	1	1	on	off	off

Where:

0 = input voltage LOW; 1 = input voltage HIGH.

Philips Components

Data sheet	
status	Product specification
date of issue	September 1990

TEA0655

Dual Dolby* B-type noise reduction circuit for playback applications

FEATURES

- Dual noise reduction channels
- Head preamplifiers
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV

GENERAL DESCRIPTION

The TEA0655 is an integrated circuit that provides two Dolby B-type noise reduction channels for playback applications in car radios. The TEA0655 includes head and equalization amplifiers with electronically switched time constants. The device will operate with power supplies in the range 9 to 15 volts, the output overload level increasing with an increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF, therefore it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range	8	–	15	V
I_{CC}	supply current	–	20	25	mA
(S+N)/N	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0655	20	DIL	plastic	SOT146

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

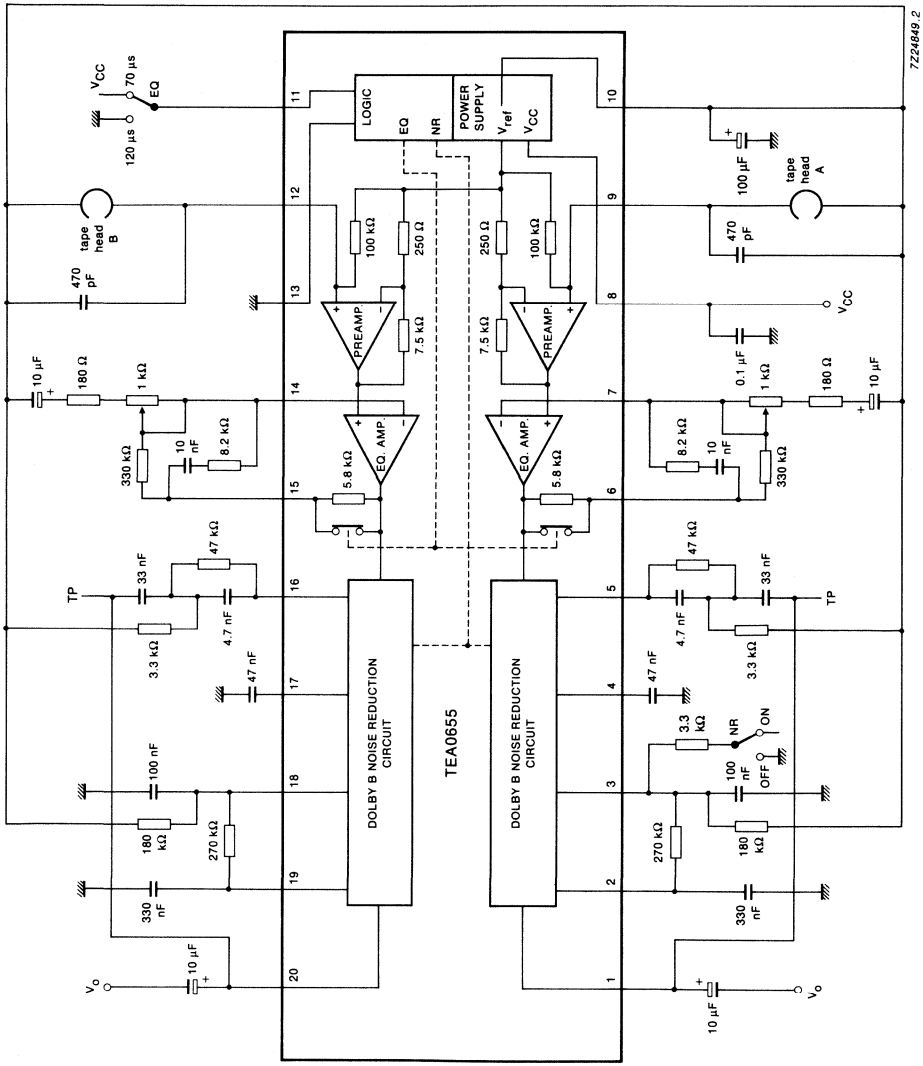


Fig.1 Block and application diagram.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 3 is open-circuit and disabled when pin 3 is connected to GRD (pin 13) via a 3.3 kΩ resistor (see Fig.1).

Pin 3 performs the functions of a logic input for noise reduction switching for both channels. It also provides smoothing for the control signal in one channel. It is important that no voltage is applied to pin 3 when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel. Time constant switching is achieved by applying a DC voltage to pin 11.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
EQA	6	equalizing output channel A
EQFA	7	equalizing input channel A
V_{CC}	8	voltage supply
INA	9	input channel A
V_{ref}	10	reference voltage
SWEQ	11	equalizing switch
INB	12	input channel B
GRD	13	ground
EQFB	14	equalizing input channel B
EQB	15	equalizing output channel B
SCB	16	side chain channel B
HPB	17	high-pass filter channel B
CONTRB	18	control voltage channel B
INTB	19	integrating filter channel B
OUTB	20	output channel B

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	16	V
V_I	input voltage (pins 1 to 20)	−0.3	V_{CC}	V
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C
V_{es}	electrostatic handling *	–	–	–

* Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V = ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels referenced to 387.5 mV RMS (0 dB) at test point (TP) (pin 1 or 20); test circuit Fig.1; NR ON; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8	10	15	V
I_{CC}	supply current		–	20	25	mA
	channel matching	NR OFF	–0.5	–	+0.5	dB
THD	distortion 2nd and 3rd harmonic	f = 1 kHz; 0 dB	–	0.08	0.15	%
		f = 10 kHz; +10 dB	–	0.15	0.3	%
	signal handling	V_{CC} = 8 V; 1% distortion at 1 kHz	12	15	–	dB
(S+N)/N	signal-plus-noise to noise ratio (see Fig.2; decode mode)	internal gain 40 dB linear; CCIR/ARM weighted	78	84	–	dB
PSRR	power supply ripple rejection	f = 1 kHz; 250 mV; see Fig.3	52	57	–	dB
	frequency response measured in encode mode see Fig.2 referenced to test point	note 1				
		f = 1 kHz; 0 dB	–1.5	0	+1.5	dB
		f = 1 kHz; –25 dB	–17.8	–19.3	–20.8	dB
		f = 0.2 kHz; –25 dB	–22.9	–24.4	–25.9	dB
		f = 5 kHz; –25 dB	–18.1	–19.6	–21.1	dB
		f = 10 kHz; –35 dB	–24.4	–25.9	–27.4	dB
α_{CR}	channel separation	f = 1 kHz; see Fig.4	57	63	–	dB
R_{Lmin}	minimum load resistance on output (pins 1 and 20)	12 dB; 1 kHz; 1% THD	10	–	–	kΩ
G_V	voltage gain (pin 9 to 7 or pin 12 to 14)	1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance pins 9 and 12		60	100	–	kΩ

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_V	open loop gain pins 12/15 and pins 9/6	10 kHz	80	86	–	dB
		400 kHz	104	110	–	dB
	DC output voltage pins 1 and 20	NR OFF with reference to $V_{CC}/2$	–	–	±0.15	V
Z_O	output impedance		–	50	70	Ω
I_{OGRD}	DC output current capability	to ground	–	–	–2	mA
I_{OVCC}		to V_{CC}	–	–	300	μA
En	equivalent input noise voltage (RMS value)	NR OFF; unweighted; 20 Hz to 20 kHz; $R_S = 0\ \Omega$	–	0.7	1.4	μV
Switching thresholds						
V_{OFF}	NR switch OFF (pin 3)		0	–	$0.2V_{CC}$	V
I_3	NR switch ON		–	open	–100	nA
	equalizing (EQ) switch (pin 11) at 70 μs		$0.5V_{CC}$	–	V_{CC}	V
	equalizing switch at 120 μs		0	–	$0.2V_{CC}$	V
I_{11}	input current		–	–	–1	μA

Note to the characteristics

1. Equals the corresponding decode mode cut with reference to test point level, see Fig.1.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

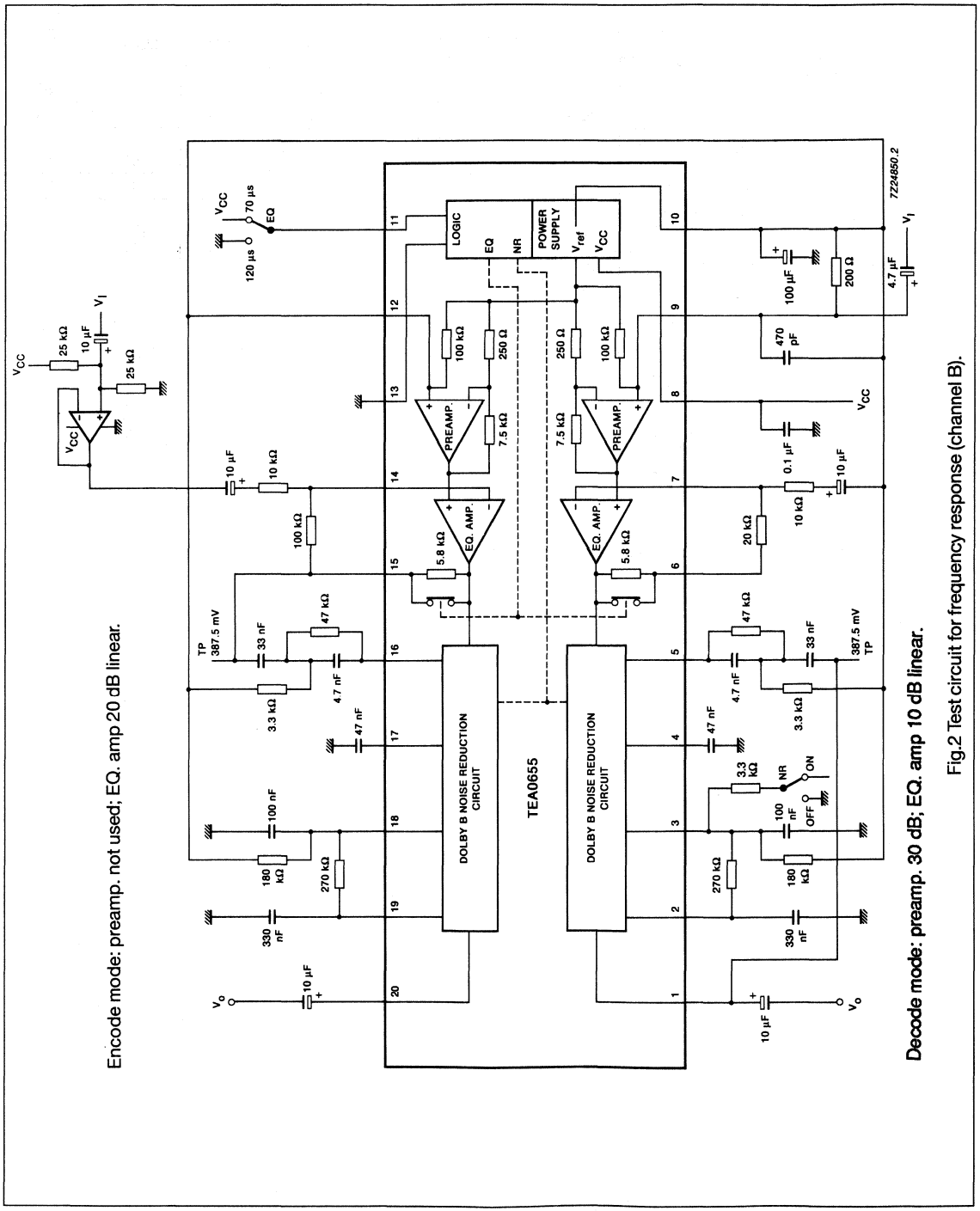


Fig.2 Test circuit for frequency response (channel B).

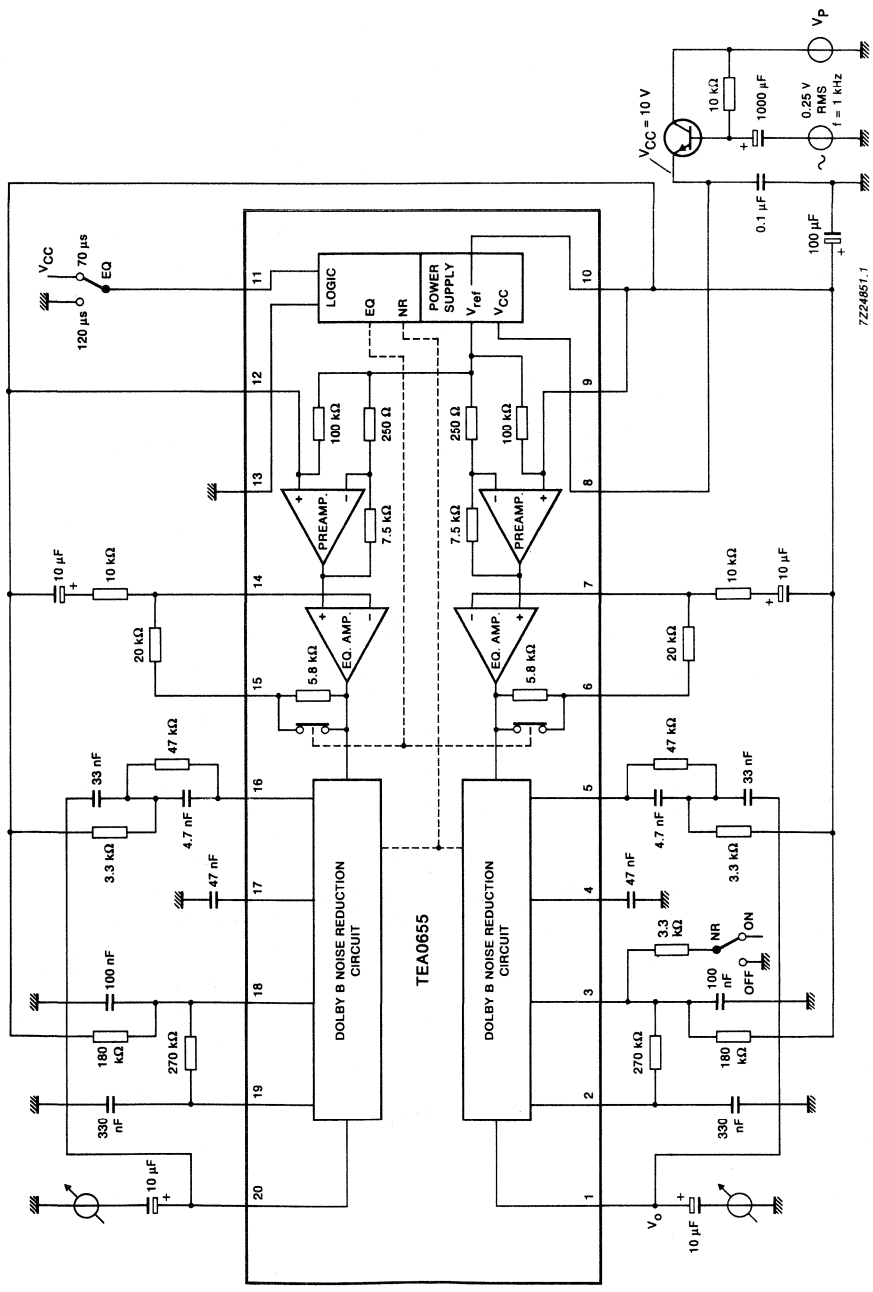


Fig.3 Test circuit for power supply ripple rejection (PSRR).

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

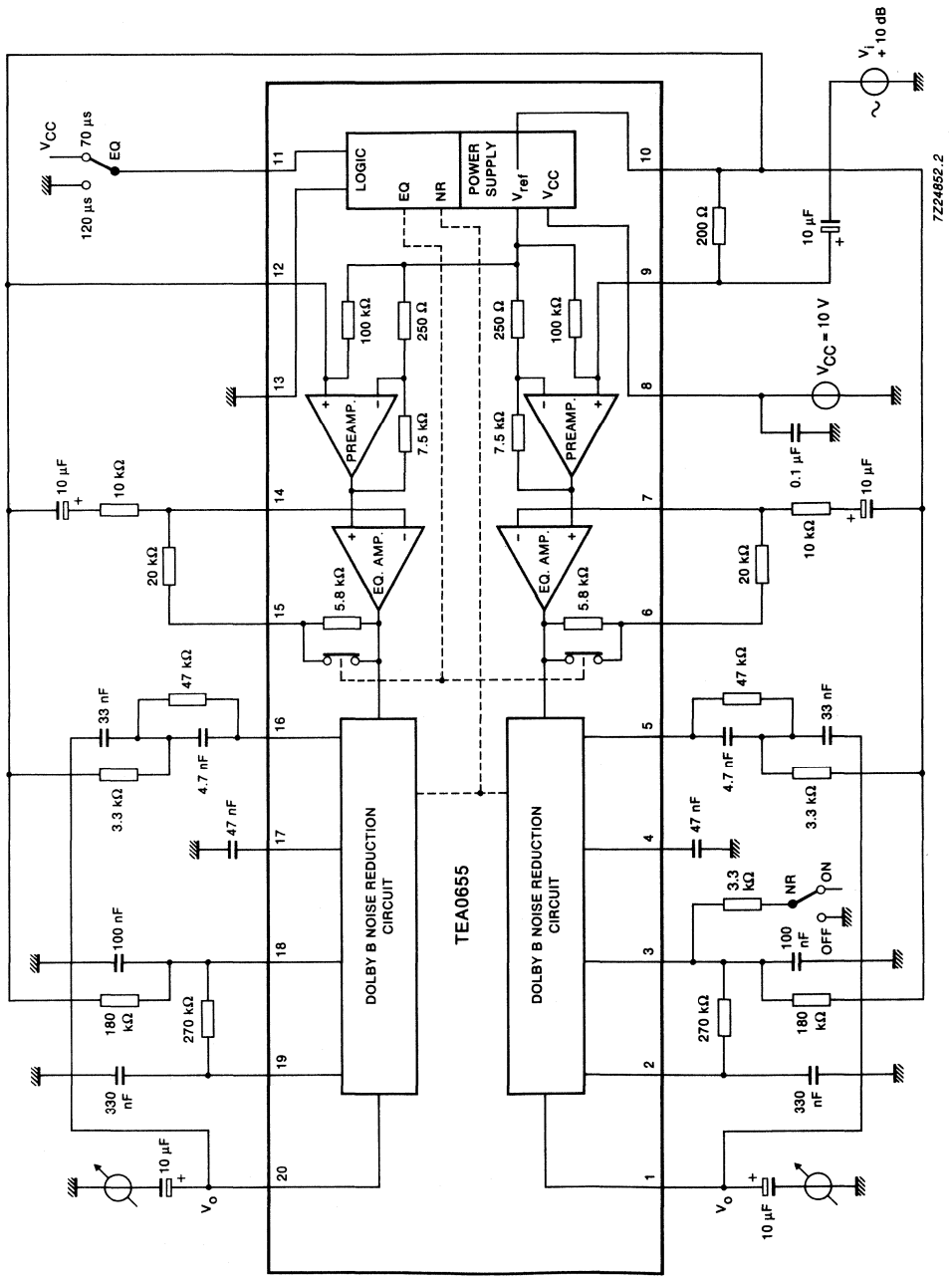


Fig.4 Test circuit for channel separation (α_{CS}).

DUAL DOLBY* B–TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0657 is a monolithic bipolar integrated circuit providing two channels of Dolby B-type noise reduction. The circuit contains all internal electronic switching to provide playback or record functions.

In addition the TEA0657 includes preamplifiers for the playback and record modes and multiplex filter buffers for both channels.

The device will operate with power supplies in the range of 9.0 V to 15.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF so it is advisable to use a regulated power supply or, a supply with a long time constant.

Features

- Dual noise reduction channels
- Full playback/record switching
- Separate playback/record inputs
- Multiplex filter buffers
- Simultaneous switching on both channels
- Dual or single supply operations
- Dolby reference level = 580 mV
- Input sensitivity = 30 mV

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{CC}	9.0	–	15.0	V
Supply current	I_{CC}	–	19	–	mA
Signal plus noise to noise ration					
record mode	(S+N)/N	–	72	–	dB
playback mode	(S+N)/N	–	90	–	dB

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
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PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

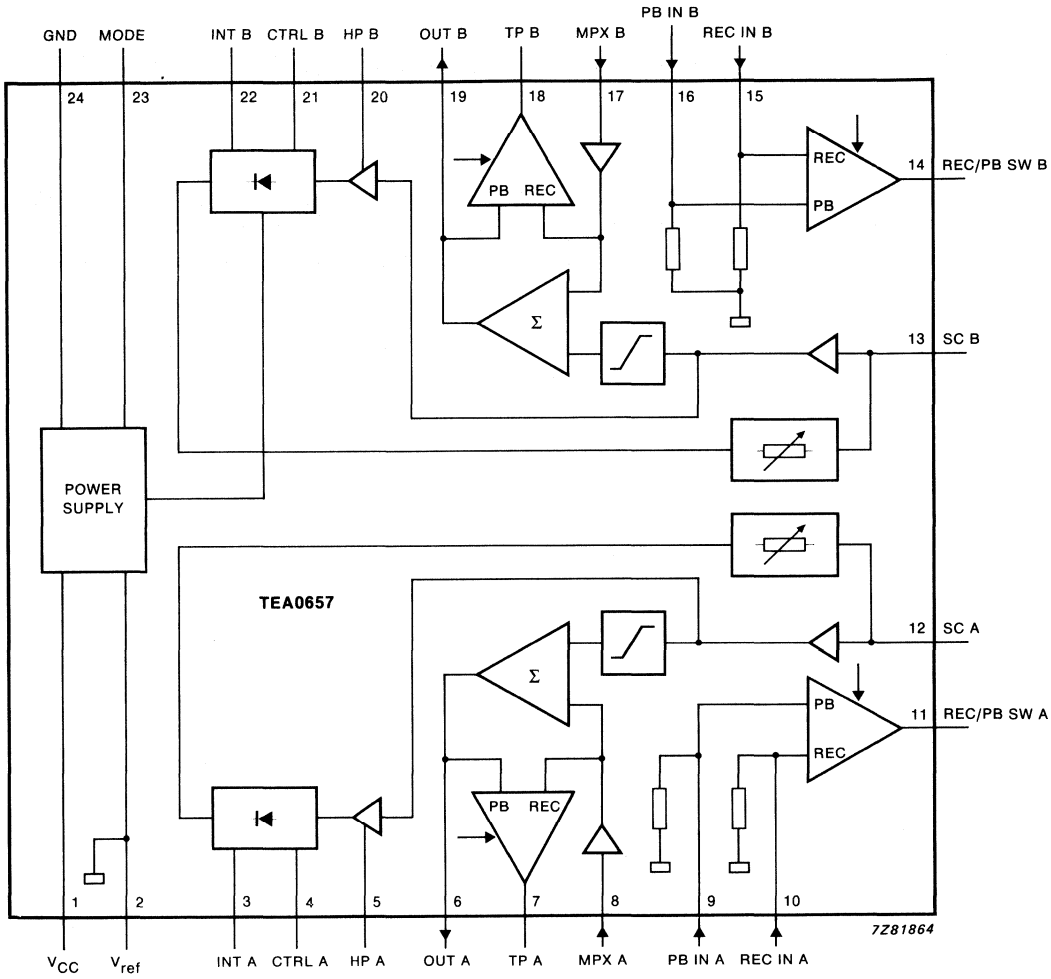


Fig. 1 Block diagram.

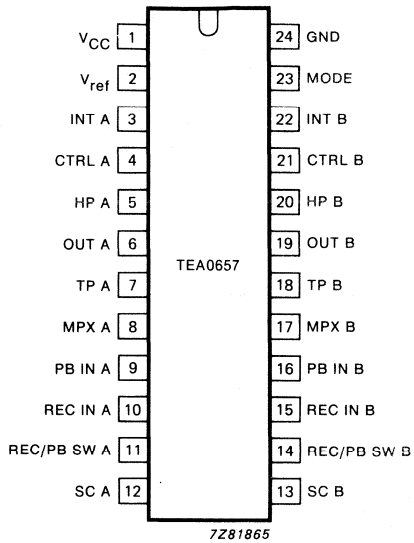


Fig. 2 Pinning diagram.

1	V_{CC}	supply voltage
2	V_{ref}	reference voltage
3	INT A	integrating filter channel A
4	CTRL A	control voltage channel A
5	HP A	high-pass filter channel A
6	OUT A	output channel A
7	TP A	test point channel A, line output channel A
8	MPX A	multiplex buffer channel A
9	PB IN A	playback input channel A
10	REC IN A	record input channel A
11	REC/PB SW A	record/playback switch channel A
12	SC A	side chain channel A
13	SC B	side chain channel B
14	REC/PB SW B	record/playback switch channel B
15	REC IN B	record input channel B
16	PB IN B	playback input channel B
17	MPX B	multiplex buffer input channel B
18	TP B	test point channel B, line output channel B
19	OUT B	output channel B
20	HP B	high-pass filter channel B
21	CTRL B	control voltage channel B
22	INT B	integrating filter channel B
23	MODE	record/playback select switch
24	GND	ground

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 22 is open-circuit and OFF when connected to pin 24 via a 5.1 kΩ resistor (see Fig. 3).
Pin 24 performs the functions of a logic input for noise reduction switching in both channels and provides smoothing for the control signal in one channel. It is important that no voltage is applied to this pin when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel.

Record/playback is achieved by applying a DC voltage to pin 23. The circuit will enable the appropriate input for the selected mode.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{CC}	–	16.0	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	–	+ 150	°C
Input voltage (pin 1)	V_I	−0,3	V_{CC}	V
Electrostatic handling (note 1)				

Note to the ratings

Note 1, Classification A:

Human body model; C = 100 pF; R = 1.5 kΩ; V ⩾ 2 kV.
Charge device model; C = 200 pF; R = 0 Ω; V ⩾ 500 V.

CHARACTERISTICS

V_{CC} = 12 V; f = 20 Hz to 20 kHz; T_{amb} = + 25 °C; all levels referenced to 580 mV RMS (0 dB) at TP (pin 7 or 18); test circuit Fig. 4; Record mode; NR ON; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	9	12	15	V
Supply current		I_{CC}	–	19	–	mA
Voltage gain (pins 9 or 10 to 11)	f = 1 kHz	G_v	–	20	–	dB
Voltage gain (pins 8 to 7)	f = 1 kHz	G_v	–	9	–	dB
Channel matching	NR OFF		−0.5	–	+ 0.5	dB
Distortion						
2nd and 3rd harmonic	f = 1 kHz, 0 dB	THD	–	0.08	0.15	%
	f = 10 kHz, + 10 dB	THD	–	0.15	0.3	%
Signal handling; (V_{CC} = 9 V)	1% distortion at 1 kHz		12	–	–	dB
Signal-to-noise plus noise ratio						
record mode	internal CCIR ARM weighted	(S+N)/N	–	72	–	dB
playback mode	R_S = 10 kHz	(S+N)/N	–	90	–	dB
Supply voltage ripple rejection	f = 1 kHz; 250 mV	SVRR	–	40	–	dB
Frequency response; (referenced to TP)	f = 1 kHz;					
	0 dB	Δf	−1.5	–	−1.5	dB
	−20 dB	Δf	−17.3	−15.8	−14.3	dB
	f = 5 kHz					
	−30 dB	Δf	−23.3	−21.8	−20.3	dB
	−40 dB	Δf	−30.2	−29.7	−28.2	dB
	f = 10 kHz					
	0 dB	Δf	−1.1	0.4	1.9	dB
	−30 dB	Δf	−25.0	−23.5	−22.5	dB
Input resistance; (pins 9, 10, 15 and 16)		R_I	–	50	–	kΩ
Channel separation	0 dB at TP; f = 1 kHz	α_{cr}	–	65	–	dB
Back-to-back frequency response shift;						
as a function of T_{amb}	0 to −70 °C		–	± 0.5	–	dB
as a function of V_{CC}	9 V to 15 V		–	± 0.5	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
PB/REC separation	30 mV; 1 kHz; at playback input, measure V_{OUT}	$\alpha_{PB/REC}$	–	72	–	dB
Minimum load resistance on output; (pins 6 and 9)	12 dB; 1 kHz; 1% THD	R_{Lmin}	10	–	–	kΩ
Switching thresholds playback; pin 23	V_{PB}	V_{PB}	0.7 V_{CC}	V_{CC}	–	V
record; pin 28		V_{REC}	–	GND	0.4 V_{CC}	V
NR OFF; pin 22		V_{OFF}	–	–	0.2 V_{CC}	V

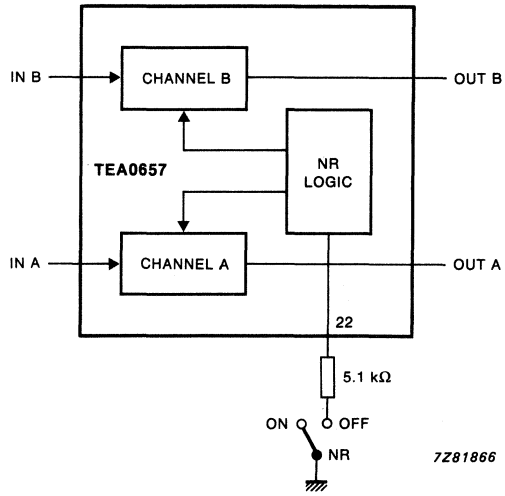
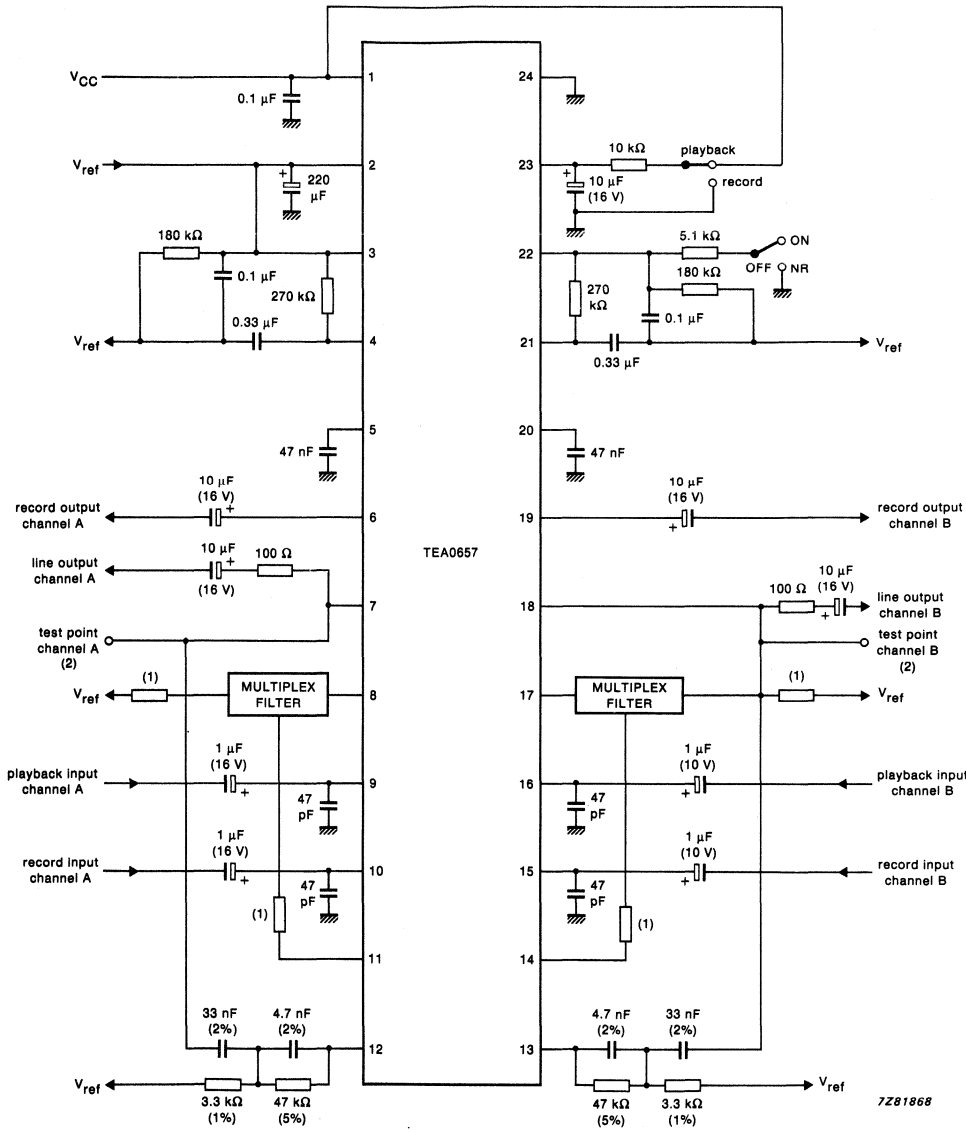


Fig. 3 External NR switch circuit for TEA0657.



All values within ± 10% unless otherwise specified.

Notes:

(1) Value determined by multiplexer in use.
(2) Dolby level = 580 mV at test points.

Fig. 4 Test and application circuit.

DOLBY* B and C TYPE NOISE REDUCTION CIRCUIT

GENERAL DESCRIPTION

The TEA0665 is designed for use in Dolby B and Dolby C type audio Noise Reduction (NR) systems. The device provides the high and low level stages for one channel of a Dolby C-type NR system, including NR ON/OFF switching and all electronic switching necessary for Dolby C-type systems. In addition the TEA0665 includes a preamplifier for the record and playback functions and a multiplex buffer amplifier. The circuit offers two different line-output levels (−6 and 0 dBm) and a low-pass filter, which can be fed into the signal path in playback mode.

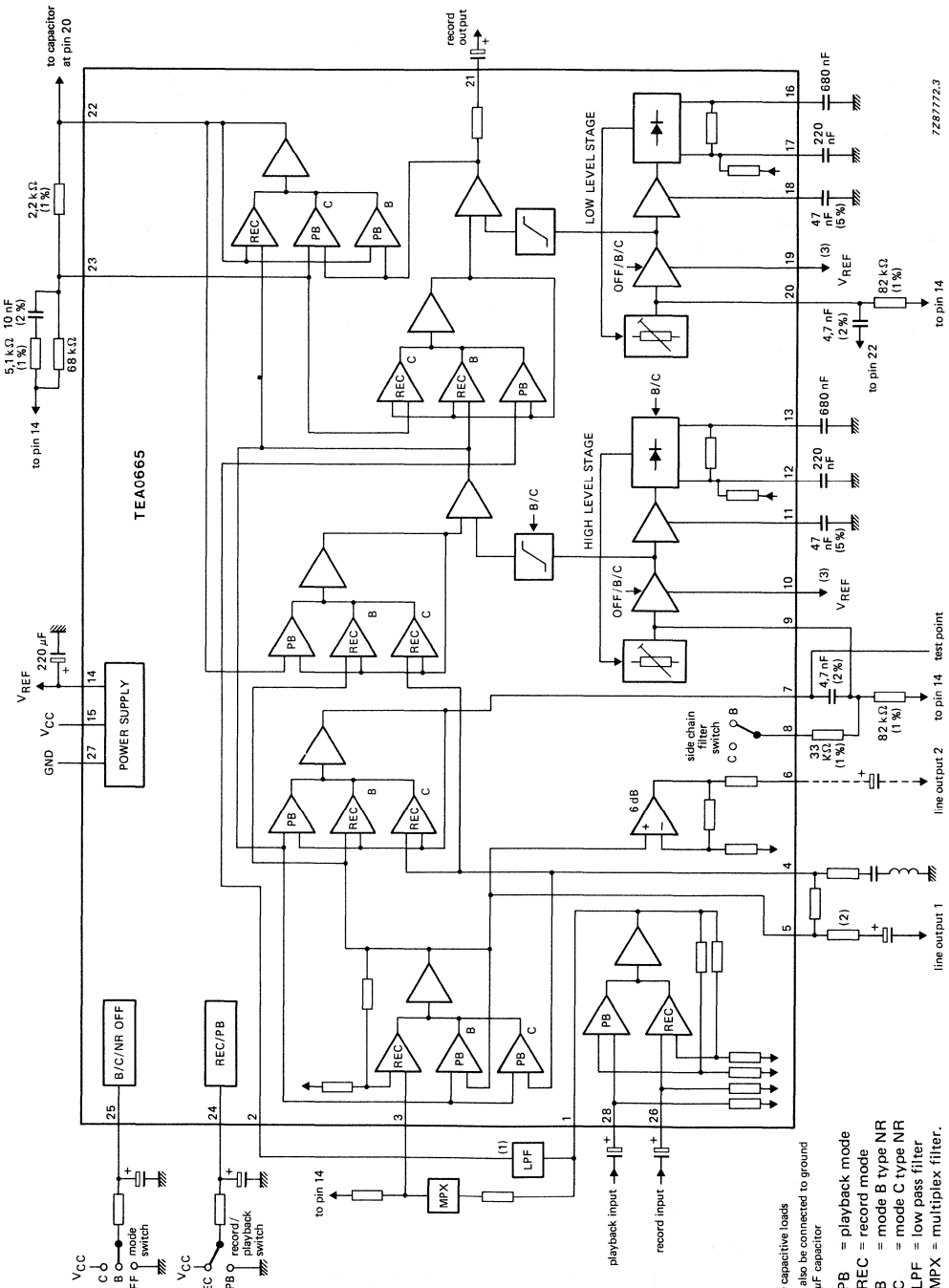
Features

- Few external components required
- Included RECORD/PLAY preamplifiers plus multiplex filter buffer amplifier
- Two different line-output levels
- All electronic switching

PACKAGE OUTLINES

TEA0665: 28-lead DIL; plastic (SOT117).
TEA0665T: 28-lead mini-pack; plastic (SO28; SOT136A).

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, U.S.A., from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.



(1) optional
(2) for large capacitive loads
(3) pin may also be connected to ground via a 10 µF capacitor

Where: PB = playback mode
REC = record mode
B = mode B type NR
C = mode C type NR
LPF = low pass filter
MPX = multiplex filter.

Fig. 1 Block diagram and application circuit.

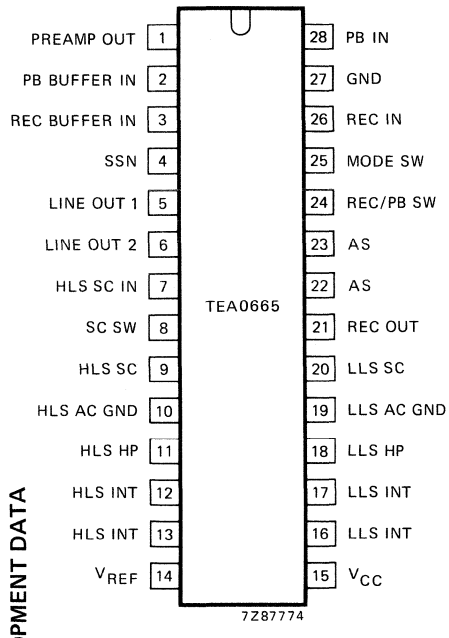


Fig. 2 Pinning diagram.

PINNING

1	PREAMP OUT	record/playback preamplifier output
2	PB BUFFER IN	playback amplifier input buffer
3	REC BUFFER IN	record amplifier input buffer
4	SSN	spectral skewing network
5	LINE OUT 1	line output 1
6	LINE OUT 2	line output 2
7	HLS SC IN	high level stage side chain input
8	SC SW	side chain filter switch
9	HLS SC	high level stage side chain
10	HLS AC GND	high level stage AC ground
11	HLS HP	high level stage high pass filter
12	HLS INT	high level stage integrating filter
13	HLS INT	high level stage integrating filter
14	V_{REF}	reference voltage
15	V_{CC}	positive supply voltage
16	LLS INT	low level stage integrating filter
17	LLS INT	low level stage integrating filter
18	LLS HP	low level stage high pass filter
19	LLS AC GND	low level stage AC ground
20	LLS SC	low level stage side chain
21	REC OUT	record output
22	AS	anti-saturation filter
23	AS	anti-saturation filter
24	REC/PB SW	record/playback switch input
25	MODE SW	mode switch input
26	REC IN	record input
27	GND	ground
28	PB IN	playback input

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_{CC}	max. 18	V
Input voltage (pins 26 and 28)	V_I	max. −0,3 to V_{CC}	V
Total power dissipation	P_{tot}	600	mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 15 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point pin 7; test circuit Fig. 5; record mode; unless otherwise specified.

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Supply								
Supply voltage range	C	–	note 1					
single				V_{CC}	8	14	16	V
(split)				V_{CC}	(±4)	(±7)	(±8)	V
Supply current	OFF	–	no input signal	I_{CC}	–	17	25	mA
Input sensitivity	C		note 2					
of record amplifier			pin 26	V_i	43	50	57	mV
of playback amplifier			pin 28	V_i	25	30	35	mV
Signal handling	C	1	V_{CC} = 8 V					
of record output			THD = 1%		12	15	–	dB
(note 3; see Fig. 8)		1	V_{CC} = 14 V					
			THD = 1%		–	20	–	dB
Line output 1			note 3		−0,5	0	+ 0,5	dB
Line output 2; amplifier gain V_o/V_i (pin 6 to pin 5)				G_v	+ 5,5	+ 6	+ 6,5	dB
Total harmonic distortion	OFF	1	TPL = 0 dB*	THD	–	0,02	0,1	%
			TPL = + 10 dB	THD	–	0,05	0,3	%
Total harmonic distortion	B	1	TPL = 0 dB	THD	–	0,1	0,15	%
			TPL = + 10 dB	THD	–	0,08	0,3	%
		10	TPL = 0 dB	THD	–	0,06	0,1	%
Total harmonic distortion	C	1	TPL = 0 dB	THD	–	0,15	0,3	%
			TPL = + 10 dB	THD	–	0,13	0,5	%
Signal plus noise-to-noise ratio	C		R_S = 10 kΩ CCIR/ARM weighted	(S+N)/N	62	66	–	dB

* TPL is Test Point Level.

DEVELOPMENT DATA

parameter	conditions			symbol	min.	typ.	max.	unit
	mode	f (kHz)						
Frequency response	B	2	TPL = −25 dB		−19,0	−18,0	−17,0	dB
		5	TPL = −40 dB		−30,7	−29,7	−28,7	dB
		10	TPL = −30 dB		−24,5	−23,5	−22,5	dB
	C	0,2	TPL = −40 dB		−33,4	−31,9	−30,4	dB
		1	TPL = −30 dB		−20,1	−18,6	−17,1	dB
		1	TPL = −20 dB		−16,1	−14,1	−12,1	dB
		5	TPL = −0 dB		−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB		−19,1	−17,1	−15,1	dB
		5	TPL = −40 dB		−28,5	−26,5	−24,5	dB
Switching thresholds			note 4; pin 24					
for record				V_{24-27}	8,5	–	14	V
for playback				V_{24-27}	0	–	4	V
Switching thresholds			note 5; pin 25					
	OFF			V_{25-27}	0	–	3,5	V
(switch in open position)	B			V_{25-27}	–	7	–	V
(external voltage)	B			V_{25-27}	6,3	7	7,7	V
	C			V_{25-27}	10,8	–	14	V
Switch input current			pin 25					
	OFF		$V_{25-27} = 0$ V	$-I_{25}$	–	–	40	μA
	C		$V_{25-27} = V_{CC}$	I_{25}	–	–	40	μA
Frequency response shift as a function of temperature deviation, range −40 to + 85 °C, measured as deviation from 25 °C	C			Δf	–	± 0,5	–	dB
as a function of voltage deviation, range 8 to 16 V, measured as deviation from 14 V				Δf	–	± 0,1		dB
Input resistance								
			pin 26	R_{26-27}	35	50	65	kΩ
			pin 28	R_{28-27}	35	50	65	kΩ
Output resistance								
			pin 6	R_{6-27}	–	160	220	Ω
			pin 21	R_{21-27}	–	60	100	Ω

Notes to the characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 7 V.
2. Attenuation between pins 1 and 3 is 3,5 dB (MPX-filter).
   Playback input sensitivity is 45 mV if a switchable MPX-low pass filter is used in playback mode (pins 2 and 3 short-circuited).
3. System headroom is determined by the line output channel in use.
   For low supply voltages line output 2 (pin 6) will saturate at high signal levels. Headroom for line output 1 (pin 5) tracks with record output (pin 21).
4. The equation for REC/PB switch input voltage is:

   REC: $V_{24\text{-}27} > 0{,}55\ V_{CC} - V_{BE} + 1{,}5\ V$,

   PB: $V_{24\text{-}27} < 0{,}45\ V_{CC} - V_{BE} - 1{,}5\ V$.
5. The equation for C/B/OFF mode switch input voltage is:

   OFF: $V_{25\text{-}27} < 0{,}38\ V_{CC} - V_{BE} - 1\ V$,

   B: $0{,}45\ V_{CC} < V_{25\text{-}27} < 0{,}55\ V_{CC}$ (external voltage),

   B: $0{,}5\ V_{CC}$ (switch in open position),

   C: $V_{25\text{-}27} > 0{,}75\ V_{CC} - V_{BE} + 1\ V$.

   The voltage drop across the external time constant resistor must be taken in to account.

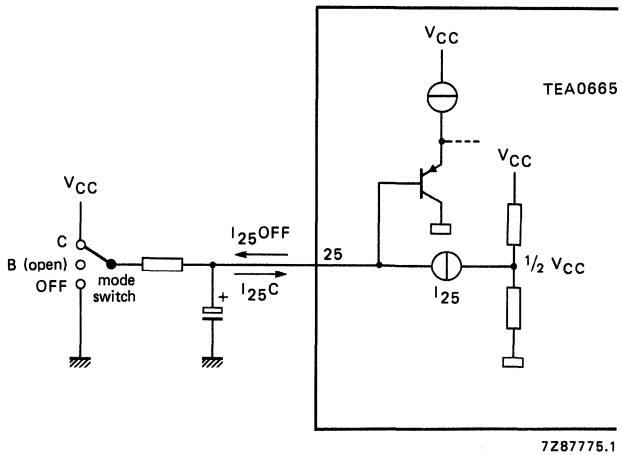


Fig. 3 Mode switch input configuration.

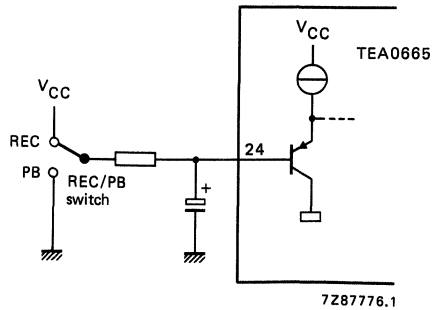
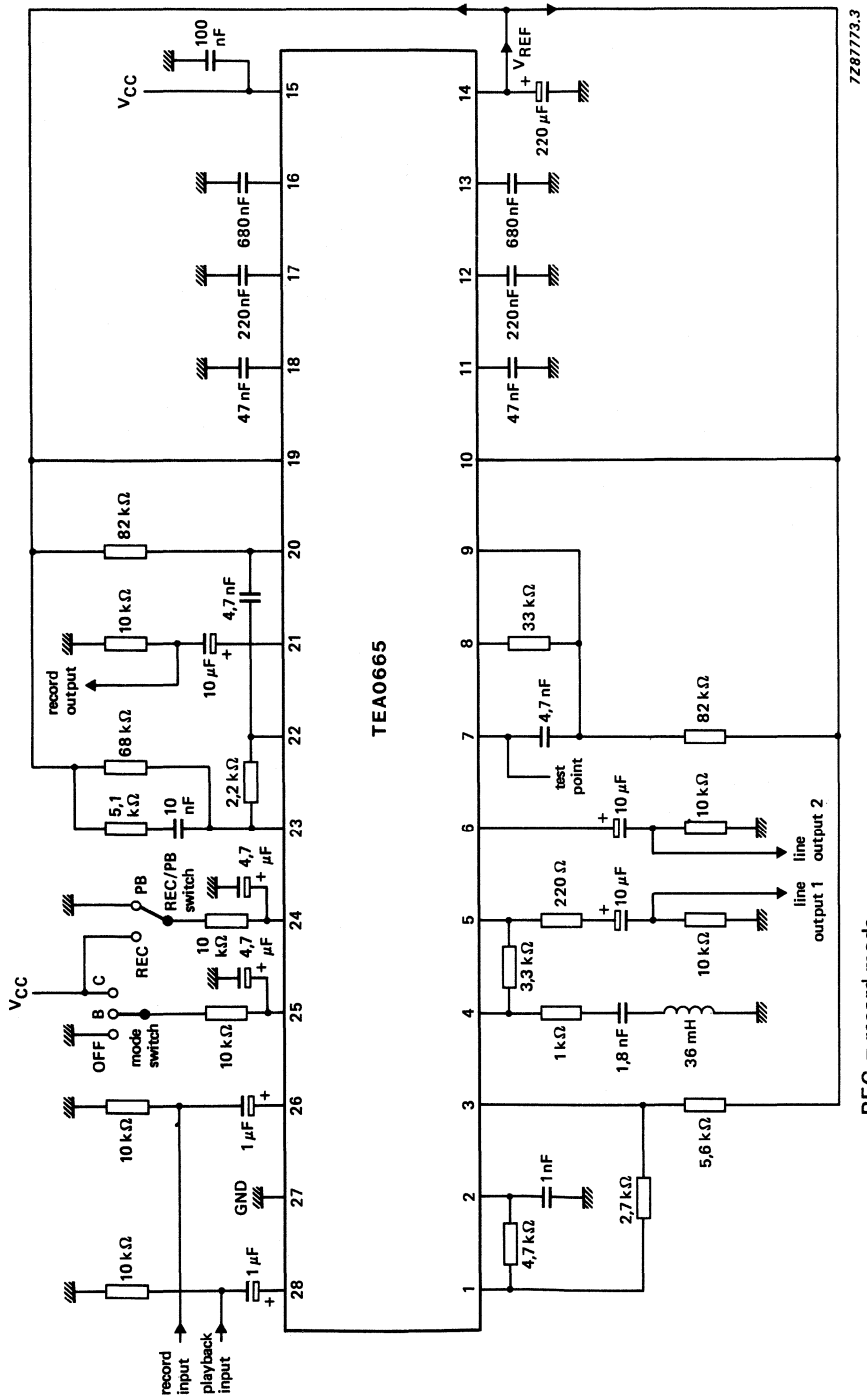


Fig. 4 REC/PB switch input configuration.

DEVELOPMENT DATA



REC = record mode
PB = playback mode

Tolerances: resistors 1%
capacitors 1%

Fig. 5 Test circuit.

SYSTEM GRAPHS

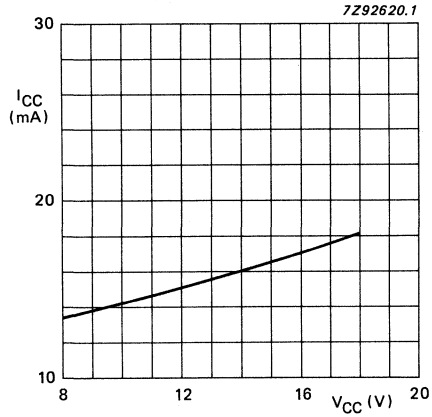


Fig. 6 Supply current as a function of supply voltage; $I_{CC} = f(V_{CC})$; no input signal.

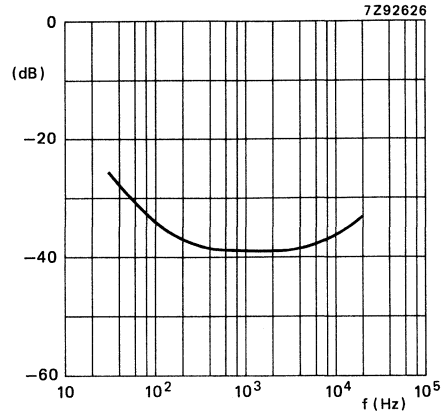


Fig. 7 Power supply ripple rejection measured at REC OUT as a function of frequency; level at pin 15 = 100 mV (rms). R_G = 10 kΩ; record mode; NR OFF.

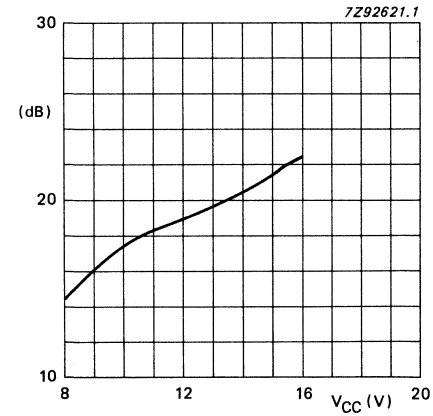


Fig. 8 Signal handling = $f(V_{CC})$ measured at REC OUT as a function of the supply voltage; THD = 1%.

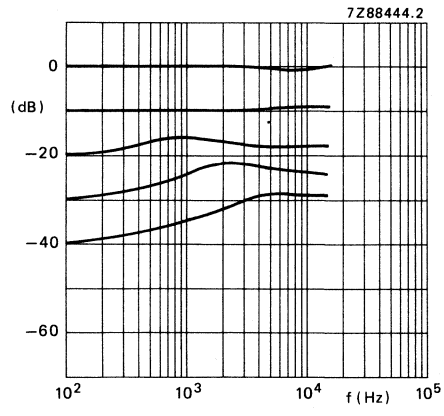


Fig. 9 Encoder frequency response for B-mode.

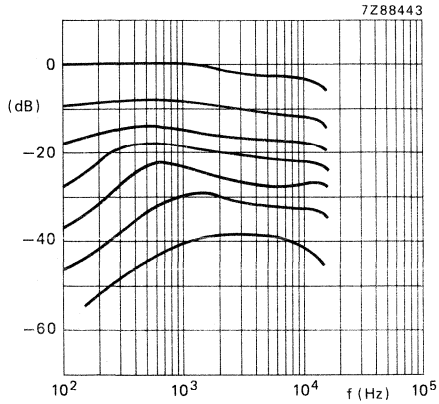


Fig. 10 Encoder frequency response for C-mode.

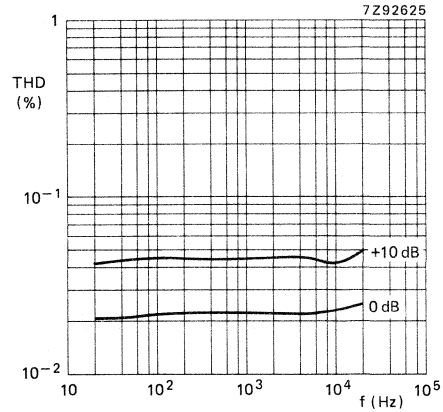


Fig. 11 Total harmonic distortion measured at REC OUT as a function of frequency; for NR OFF mode; V_{CC} = 14 V; LPF 80 kHz.

DEVELOPMENT DATA

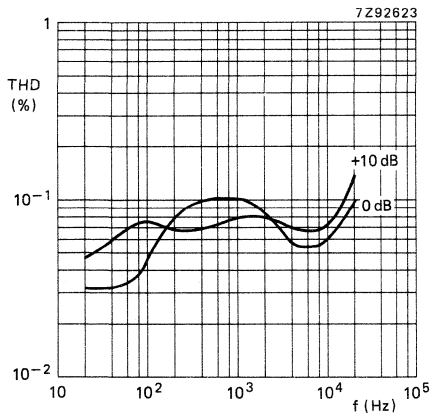


Fig. 12 Total harmonic distortion measured at REC OUT as a function of frequency; for B-mode; V_{CC} = 14 V; LPF 80 kHz.

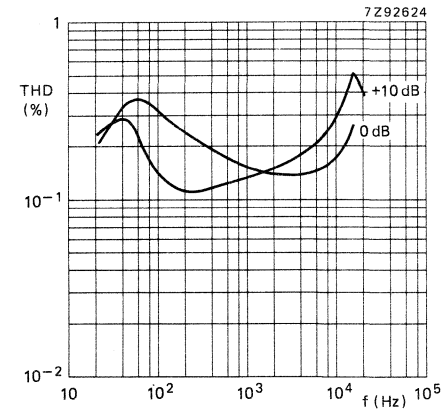


Fig. 13 Total harmonic distortion measured at REC OUT as a function of frequency; for C-mode; V_{CC} = 14 V; LPF 80 kHz.

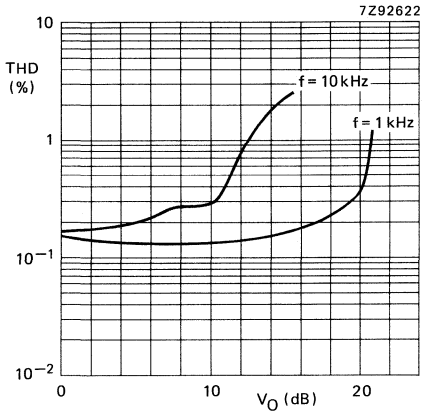


Fig. 14 Total harmonic distortion as a function of the record output level (pin 21); for C-mode; V_{CC} = 14 V; LPF 80 kHz.

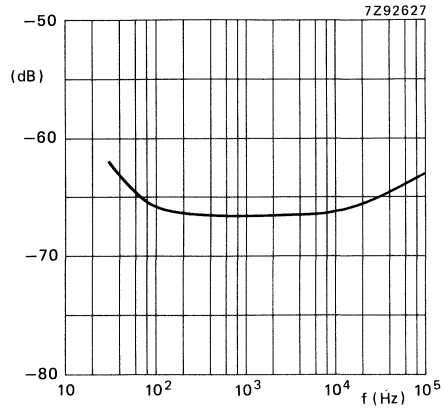


Fig. 15 Crosstalk from record input (pin 26) to line output as a function of frequency in playback mode; record input level is 50 mV; NR OFF; R_G = 10 kΩ.

1-CHIP AM RADIO

GENERAL DESCRIPTION

The TEA5551T is a 1-chip monolithic integrated radio circuit which is designed for use as a pocket receiver with headphones in a supply voltage range (V_S) of 1.8 V to 4.5 V.
The circuit consists of a complete AM part and dual AF amplifier with low quiescent current. The AF part has low radiation (HF noise) and good overdrive performance. The dual AF amplifier makes the device suitable for operation in an AM/FM stereo receiver with or without stereo cassette player.
The IC has a 1-pin switch for AM or other applications.

Features

- Low voltage operation (V_S = 1.8 V to 4.5 V)
- Low current consumption (I_{tot} = 5 mA at V_S = 3 V)
- All pins provided with ESD protection

AM part

- High sensitivity (V_i = 1.5 μV for V_o = 10 mV)
- Good IF suppression
- Good signal handling ($V_{i(max)}$ = 80 mV)
- Switch for AM or other applications
- Short waveband (> 40 MHz)

AF part

- A fixed integrated gain of 32 dB
- Few external components required
- Very low quiescent current
- Low HF radiation and good AF overdrive performance
- 0 to 20 kHz limited frequency response
- 25 mW per channel output power in 32 Ω

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_S	1.8	3.0	4.5	V
Supply current		$I_5 + I_{10}$	–	6	–	mA
AM part	m = 0.3					
RF sensitivity						
RF input voltage						
	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
	S/N = 26 dB	$V_{i(RF)}$	–	15	–	μV
	S/N = 50 dB	$V_{i(RF)}$	–	10	–	mV
AF output voltage	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
Total harmonic distortion	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
Signal handling capability	m = 0.8; THD = 10%	$V_{i(RF)}$	–	80	–	mV
AF part	both channels driven					
Output power	R_L = 32 Ω; THD = 10%					
at V_S = 3.0 V		P_o	–	25	–	mW
at V_S = 4.5 V		P_o	–	60	–	mW
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Channel separation	1 kHz	α	–	50	–	dB

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).

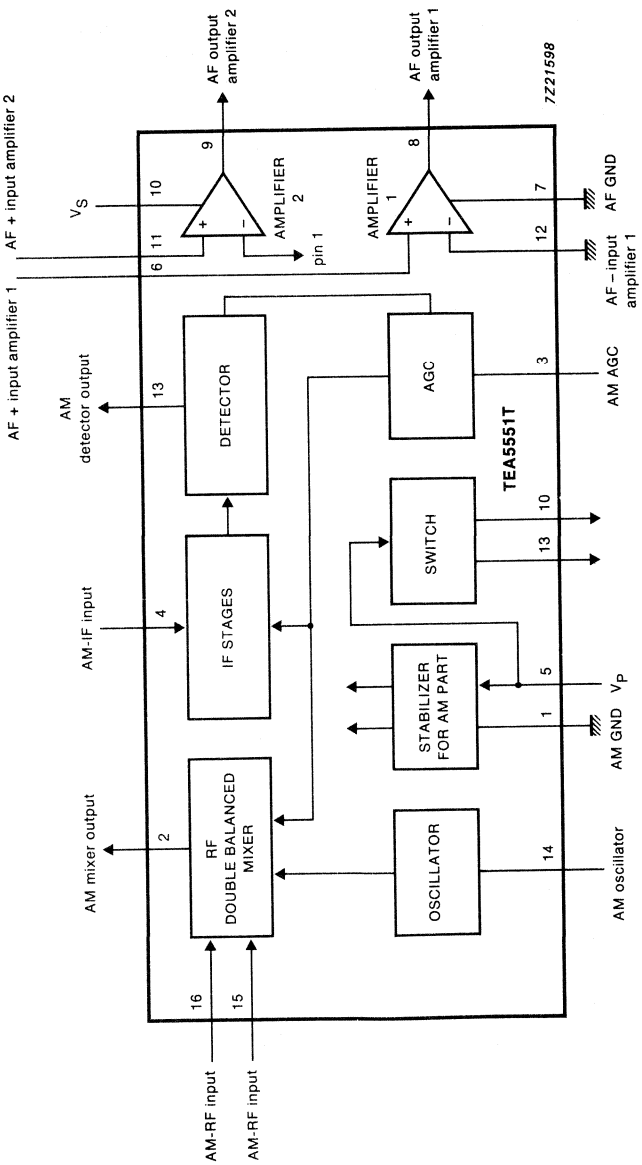


Fig. 1 Block diagram.

PINNING

1	AM GND	9	AF output amplifier 2
2	AM mixer output	10	AF supply voltage (V_S)
3	AM AGC	11	AF + input amplifier 2
4	AM–IF input	12	AF – input amplifier 1
5	AM supply voltage (V_P)	13	AM detector output
6	AF + input amplifier 1	14	AM oscillator
7	AF GND	15	AM–RF input
8	AF output amplifier 1	16	AM–RF input

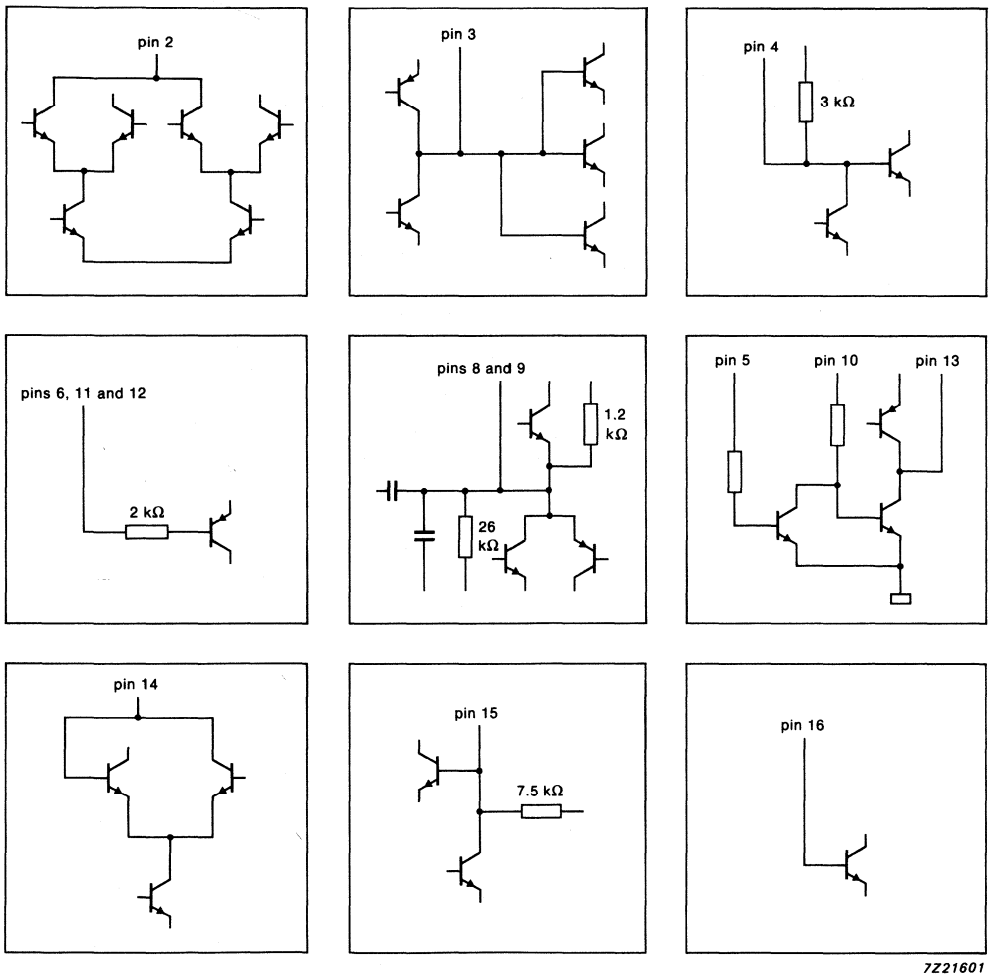


Fig. 2 All pins provided with ESD protection diodes to substrate.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_S	–	6	V
Supply current (peak)		I_M	–	150	mA
Crystal temperature		T_c	–	150	°C
Short-circuit protection	V_S = 4.5 V	t_{sc}	–	5	s
Total power dissipation		P_{tot}	see Fig. 3		
Storage temperature range		T_{stg}	–65	+150	°C
Operating ambient temperature range		T_{amb}	–25	+60	°C

QUALITY

In accordance with UZW-BO/FQ-0601.
Operating life endurance verified 2000 hours at T_j = 85 °C.
The product meets the 600 V ESD on all pins (HBM specification UZW-BO/FQ-A302).

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 110 K/W

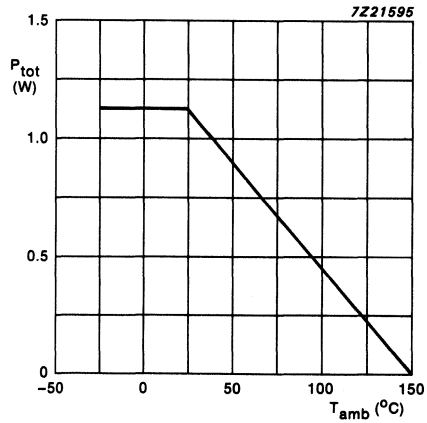


Fig. 3 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 1 and pin 7; all input currents are positive; all parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	1.8	3.0	4.5	V
Voltages					
pin 5	V_5	1.6	2.8	4.3	V
pin 10	V_{10}	1.8	3.0	4.5	V
HF part					
Total current consumption (pin 5)	I_5	–	2.2	–	mA
Oscillator current (pin 14)	I_{14}	–	100	–	μA
Mixer current (pin 2)	I_2	–	200	–	μA
Voltages					
pin 3	V_3	–	150	–	mV
pin 13	V_{13}	–	600	–	mV
pin 15	V_{15}	–	1.1	–	V
pin 16	V_{16}	–	1.1	–	V
AF part					
Total current consumption (pin 10)	I_5	–	4.0	–	mA
Input bias current (pin 11 connected to pin 16)	$I_{11} + I_{16}$	–	40	–	nA
DC output voltage					
pin 8	V_8	–	1.5	–	V
pin 9	V_9	–	1.5	–	V

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input voltage	$V_{o(AF)}$ = 10 mV	$V_{i(RF)}$	–	1.5	–	μV
Loss in sensitivity	$V_{o(AF)}$ = 10 mV; V_S = 1.8 V	$\Delta V_{i(RF)}$	–	6	–	dB
Noise						
Signal-to-noise ratio for RF input signal voltage of						
$V_{i(RF)}$ = 2 μV		S/N	–	6	–	dB
$V_{i(RF)}$ = 15 μV		S/N	–	26	–	dB
$V_{i(RF)}$ = 1 mV		S/N	–	46	–	dB
AF output voltage						
	$V_{i(RF)}$ = 1 mV	$V_{o(AF)}$	–	80	–	mV
	$V_{i(RF)}$ = 1 mV; V_S = 1.8 V	$V_{o(AF)}$	–	55	–	mV
Total harmonic distortion						
	$V_{i(RF)}$ = 100 μV to 30 mV	THD	–	0.8	–	%
	$V_{i(RF)}$ = 80 mV; m = 0.8	THD	–	10	–	%
AGC range						
Change in RF input voltage for 10 dB change in AF output voltage	$V_{i(RF1)}$ = 50 mV	$V_{i(RF1)}/V_{i(RF2)}$	–	86	–	dB
Optimum source impedance		Z_{source}	–	3	–	kΩ
IF suppression						
at $V_{o(AF)}$ = 10 mV	note 1	α	–	20	–	dB
Oscillator (pin 14)	f_{osc} = 1468 kHz					
Oscillator voltage		V_i	–	100	–	mV
	V_5 = 1.5 V	V_i	–	*	–	mV

Note to the AC characteristics

1. $\alpha = \frac{V_i \text{ at } f_i = 468 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit of Fig. 6 at V_S = 3 V; T_{amb} = 25 °C unless otherwise specified

AF conditions: f = 1 kHz; R_L = 32 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power						
	THD = 10%	P_o	–	25	–	mW
	THD = 10%; V_S = 1.8 V	P_o	–	8	–	mW
	THD = 10%; V_S = 4.5 V	P_o	–	60	–	mW
Total harmonic distortion	P_o = 10 mW	THD	–	0.5	–	%
Voltage gain	P_o = 10 mW	G_v	–	32	–	dB
Noise						
Noise output voltage	R_S = 5 kΩ; B = 15 kHz	V_{no}	–	240	–	μV
HF noise output voltage	R_S = 5 kΩ; B = 5 kHz; f = 500 kHz	$V_{no(RF)}$	–	20	–	μV
Input circuit						
Input impedance	pin 11 connected to pin 12	Z_i	–	3	–	MΩ
Mute switch						
AC impedance (pin 13 to ground)	V_5 = 0 V; I_{13} = 0.32 mA	R_S	–	200	–	Ω

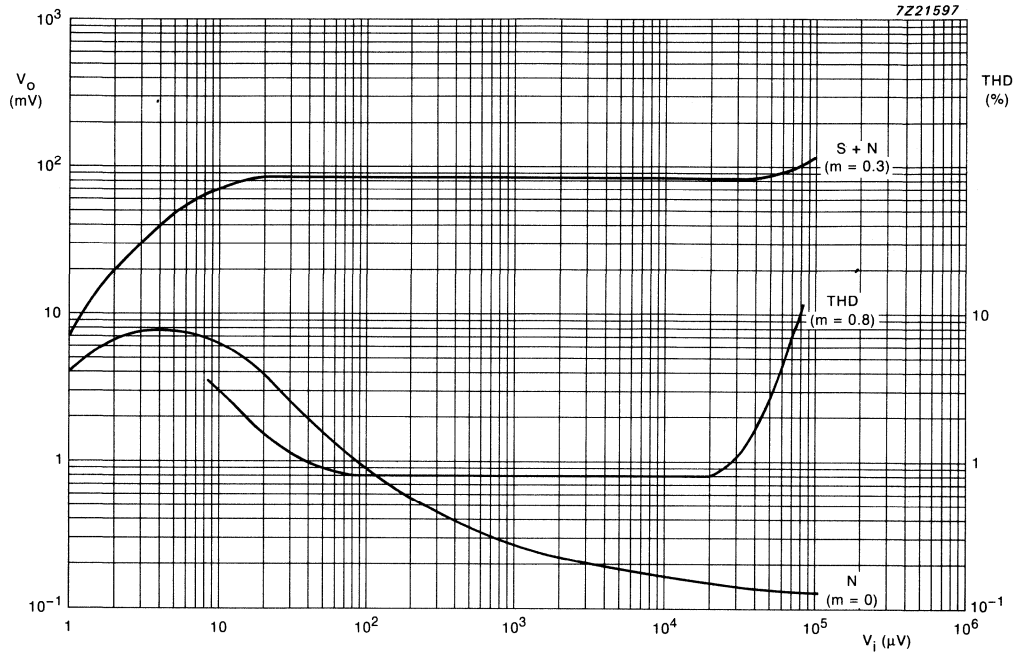


Fig. 4 Typical signal (S) and noise (N) output voltages, where V_o is the AF output voltage at pin 13, as a function of the input voltage V_i. V_i is the input voltage at pin 16. Also shown is the total harmonic distortion (THD).
Conditions: f_o = 1 MHz; f_m = 1 kHz; V_S = 3 V; R_g = 50 Ω; m = 0.3 (unless otherwise specified).

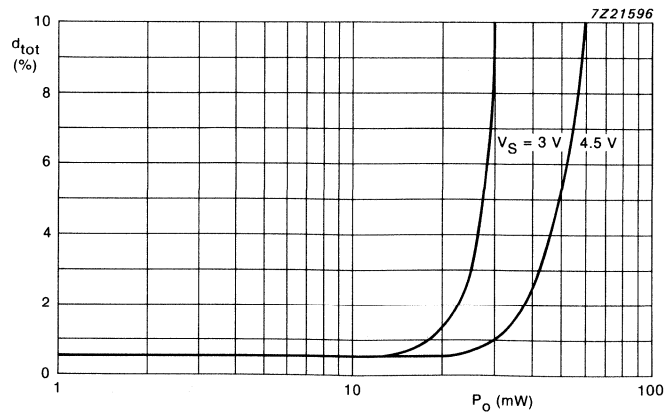


Fig. 5 Total distortion (d_{tot}) as a function of output power (P_o).
Conditions: V_S = 3 V and 4.5 V; R_L = 32 Ω; f = 1 kHz.

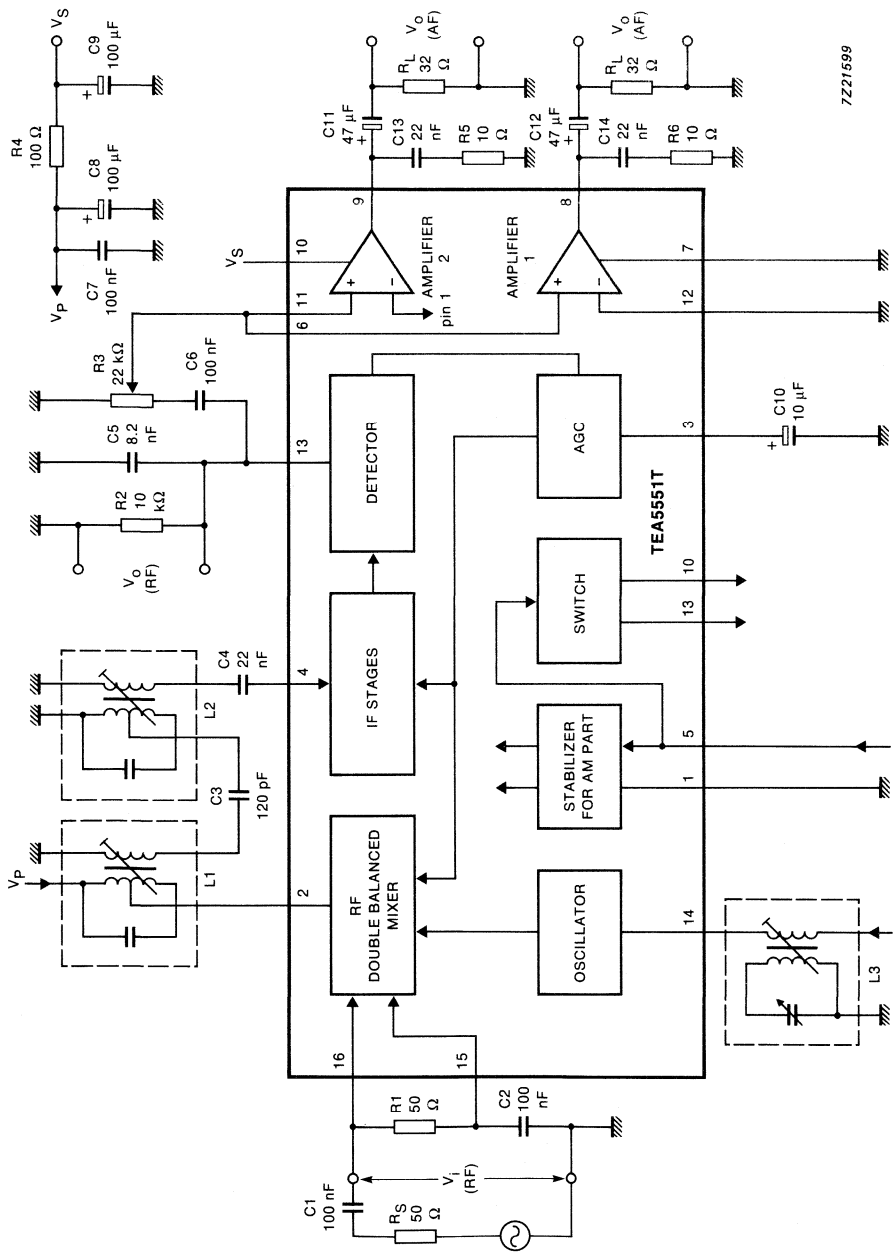
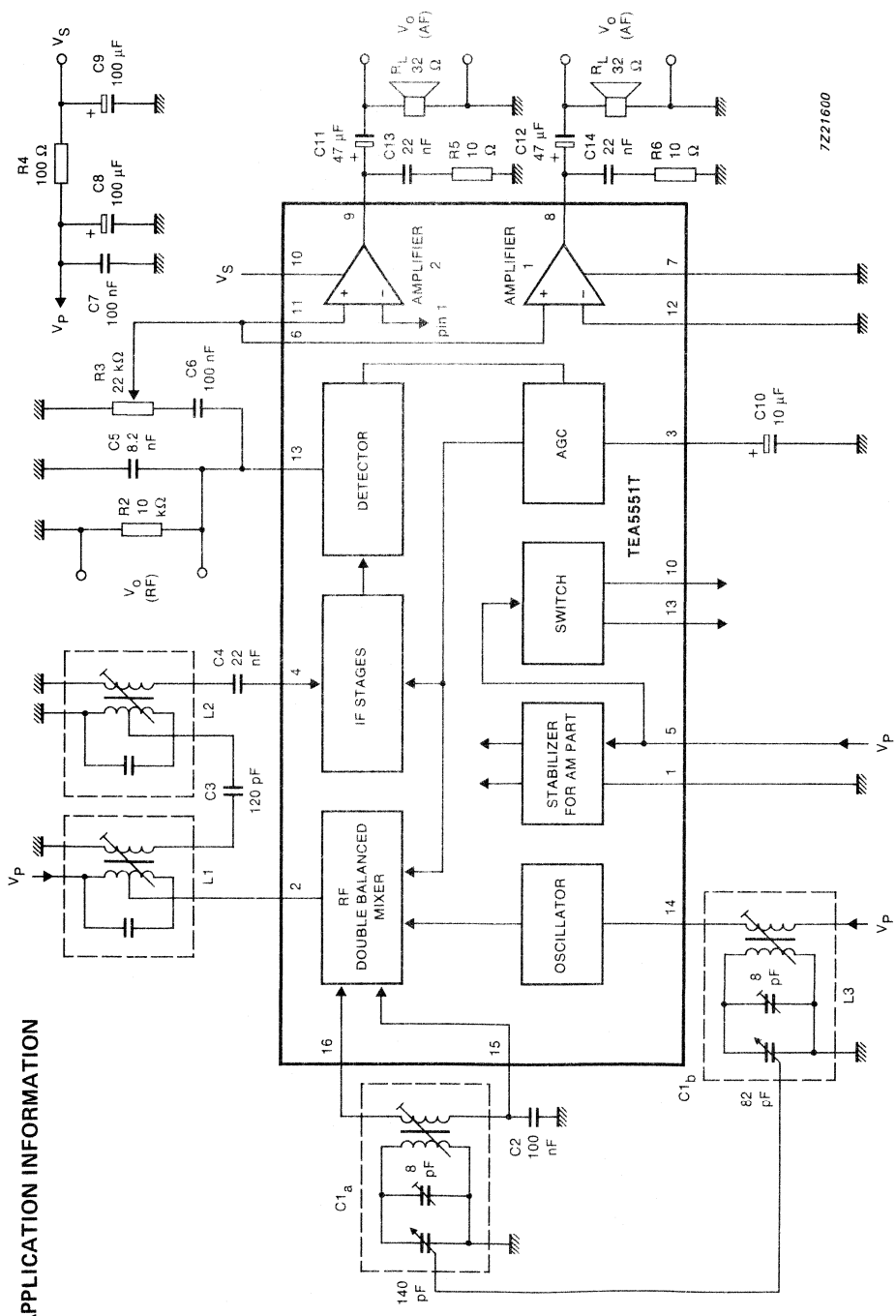


Fig. 6 Test circuit.

Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

APPLICATION INFORMATION

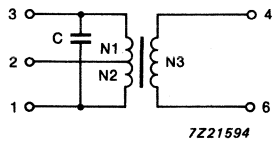


Coil data: L1 7MCS2199
L2 7MCS2197
L3 7BRS10869X

Fig. 7 Application circuit.

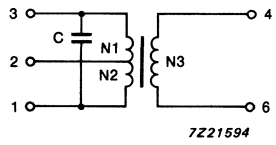
COIL DATA

AM coils (Figs 6 and 7)



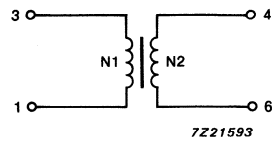
N1 = 60
N2 = 80
N3 = 15
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 8 IF bandpass filter (L1). TOKO sample no. 7MCS2199.



N1 = 125
N2 = 15
N3 = 6
C = 180 pF (internal)
L1–L3 = 643 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7MC

Fig. 9 IF bandpass filter (L2). TOKO sample no. 7MCS2197.



N1 = 90
N2 = 6
L1–L3 = 295 μH
Qo = 110
Wire = 0.07 mm dia.
Coil type 7P–TOKO
Material 7BR

Fig. 10 Oscillator coil (L3). TOKO sample no. 7BRS10869X.

SUPERSEDES DATA OF DECEMBER 1982

RF/IF CIRCUIT FOR AM/FM RADIO

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	I_7	typ.	6,2 mA
AM performance (pin 2) for m = 0,3			
Sensitivity			
at V_o = 10 mV	V_i	typ.	1,7 μV
at S/N = 26 dB	V_i	typ.	16 μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5 %
FM performance (pin 1) for Δf = ± 22,5 kHz			
limiting sensitivity, −3 dB	V_i	typ.	110 μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65 dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3 %
AM suppression at V_i = 10 mV	AMS	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

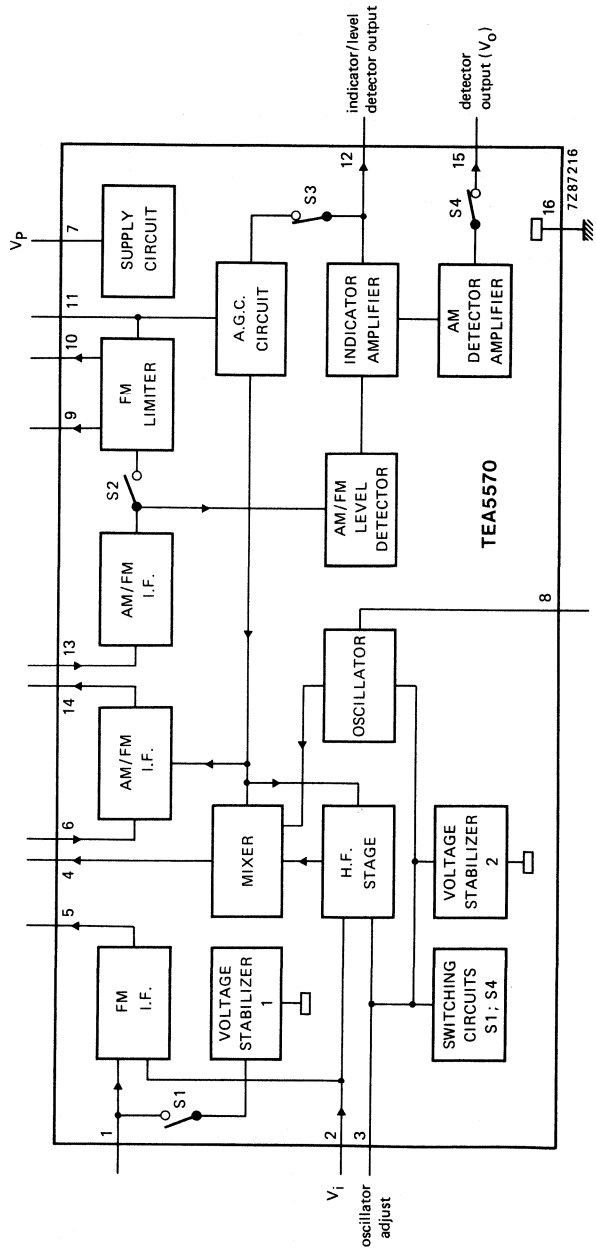


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	V_{n-16}	max.	12 V
Voltage range at pin 8	V_{8-16}		$V_P \pm 0{,}5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	W
Storage temperature range	T_{stg}		−55 to +150 °C
Operating ambient temperature range	T_{amb}		−30 to +85 °C

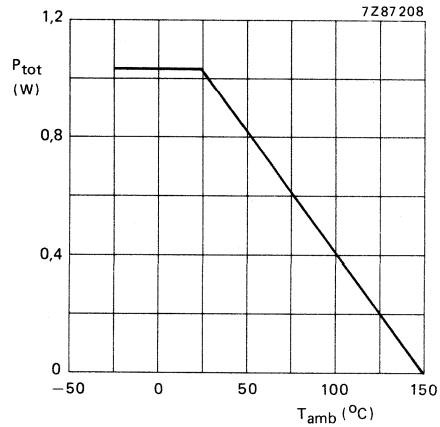


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7\text{-}16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	$V_{1\text{-}16}$	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	$V_{1\text{-}16}$	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3\text{-}16}$	–	1,42	–	V
at pin 6	$V_{6\text{-}16}$	–	0,7	–	V
at pin 11	$V_{11\text{-}16}$	–	1,4	–	V
at pin 13	$V_{13\text{-}16}$	–	0,7	–	V
at pin 14	$V_{14\text{-}16}$	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	–	1,3		μV
at S + N/N = 26 dB	V_i	–	16	20	μV
at S + N/N = 50 dB	V_i	–	1	–	mV
Signal handling (THD ⩽ 10% at m = 0,8)	V_i	200	–	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	–	0,5	–	%
at V_i = 2 mV (m = 0,8)	THD	–	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	–	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	–	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	–	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at –3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	–	6	–	μV
at S + N/N = 65 dB	V_i	–	1	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	–	0,3	–	%
AM suppression (note 5)	AMS	–	50	–	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	–	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	–	0,25	–	V
at V_i = 2 mV	$V_{12\text{-}16}$	–	1,0	–	V
AM to FM switch					
Switching current at $V_{3\text{-}16} < 1$ V	$-I_3$	–	–	400	μA

Notes to characteristics

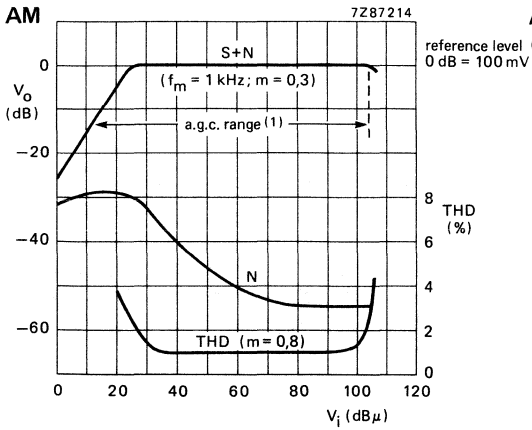
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
   $I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

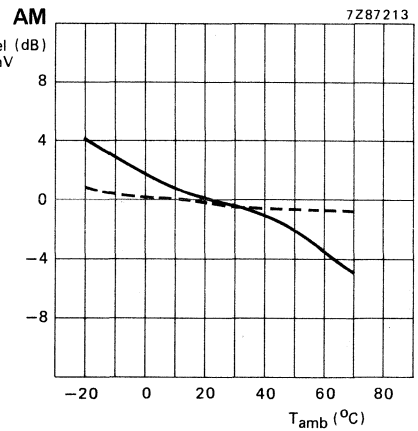
Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

Typical graphs



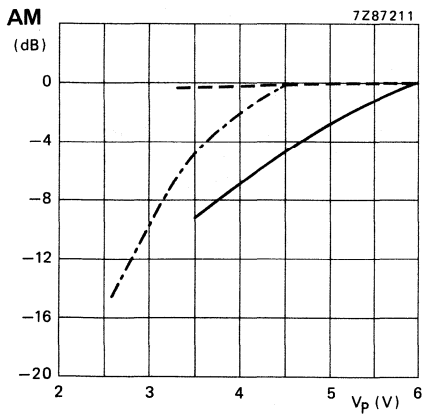
(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.
– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.
—·—·— sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

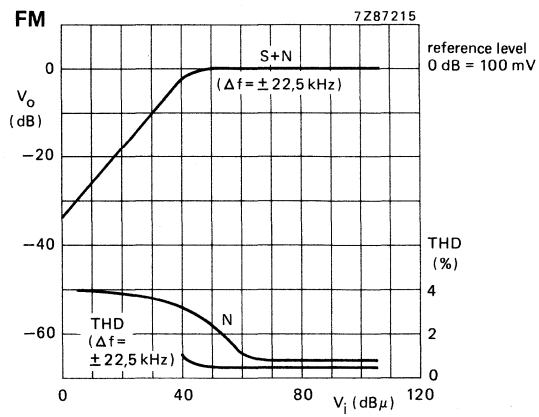
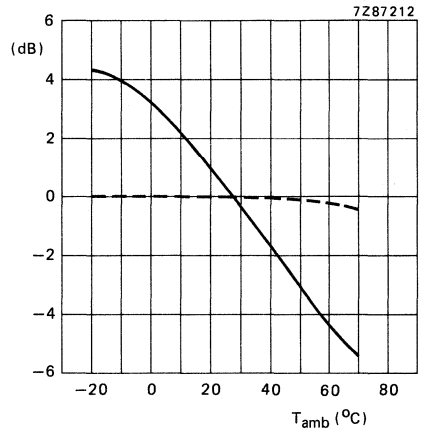


Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

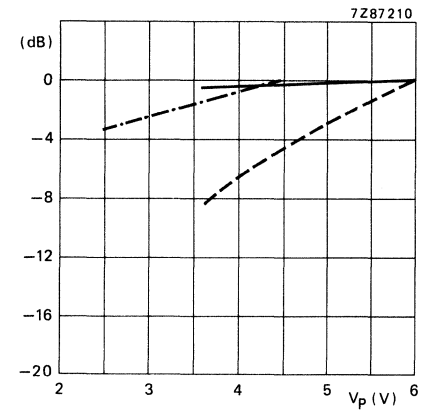
FM



——— sensitivity at −3 dB limiting.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22$ kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

FM



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.
–·–·– sensitivity at −3 dB limiting: V_P = 4,5 V application.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22{,}5$ kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

AM/FM

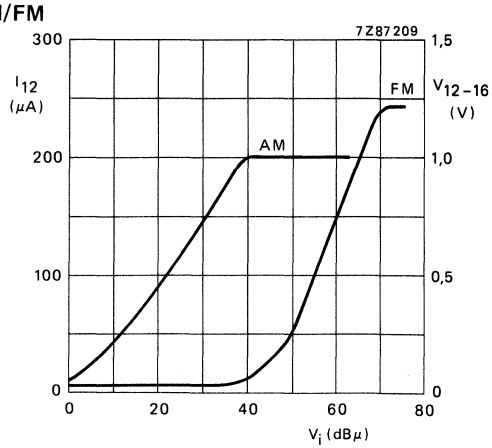


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

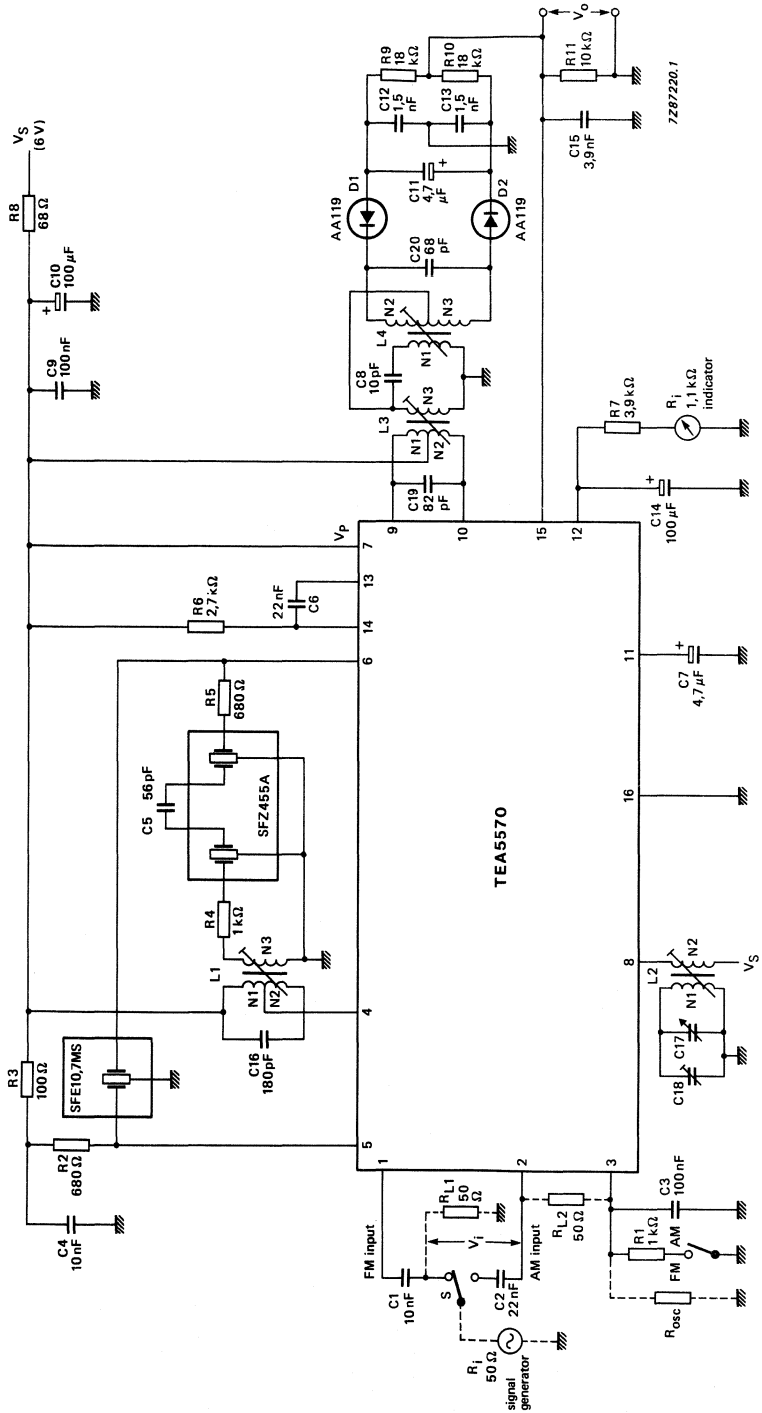


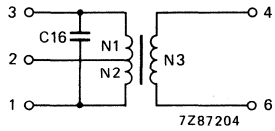
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 = 2{,}7\ k\Omega$ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275\ \Omega$ (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

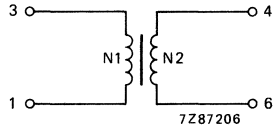
COIL DATA

AM i.f. coils (Fig. 10)



N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

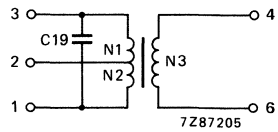
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.



N1 = 90
N2 = 7
Wire = 0,07 mm dia.

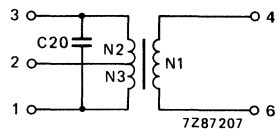
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)



N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

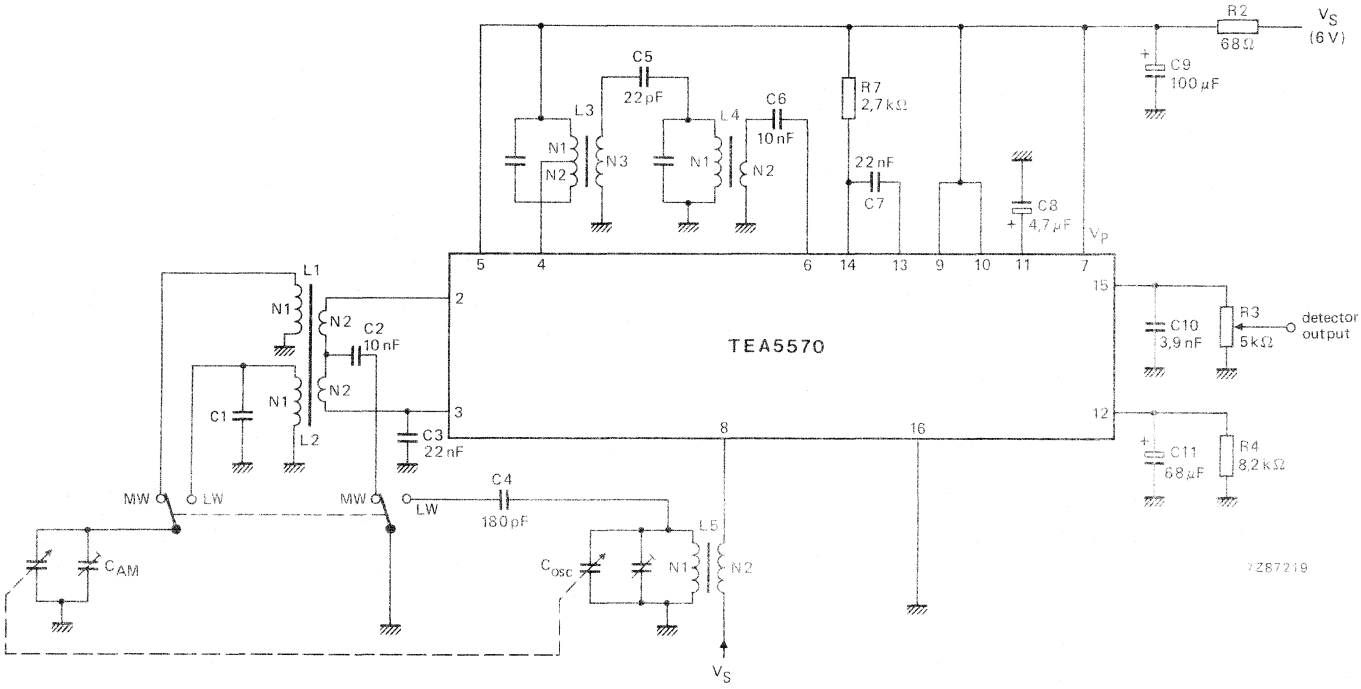


N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



Coil data

L3	N1 = 73	L4 N1 = 146	L5 N1 = 90
	N2 = 73	N2 = 9	N2 = 6
	N3 = 9	C = 180 pF	
	C = 180 pF		

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

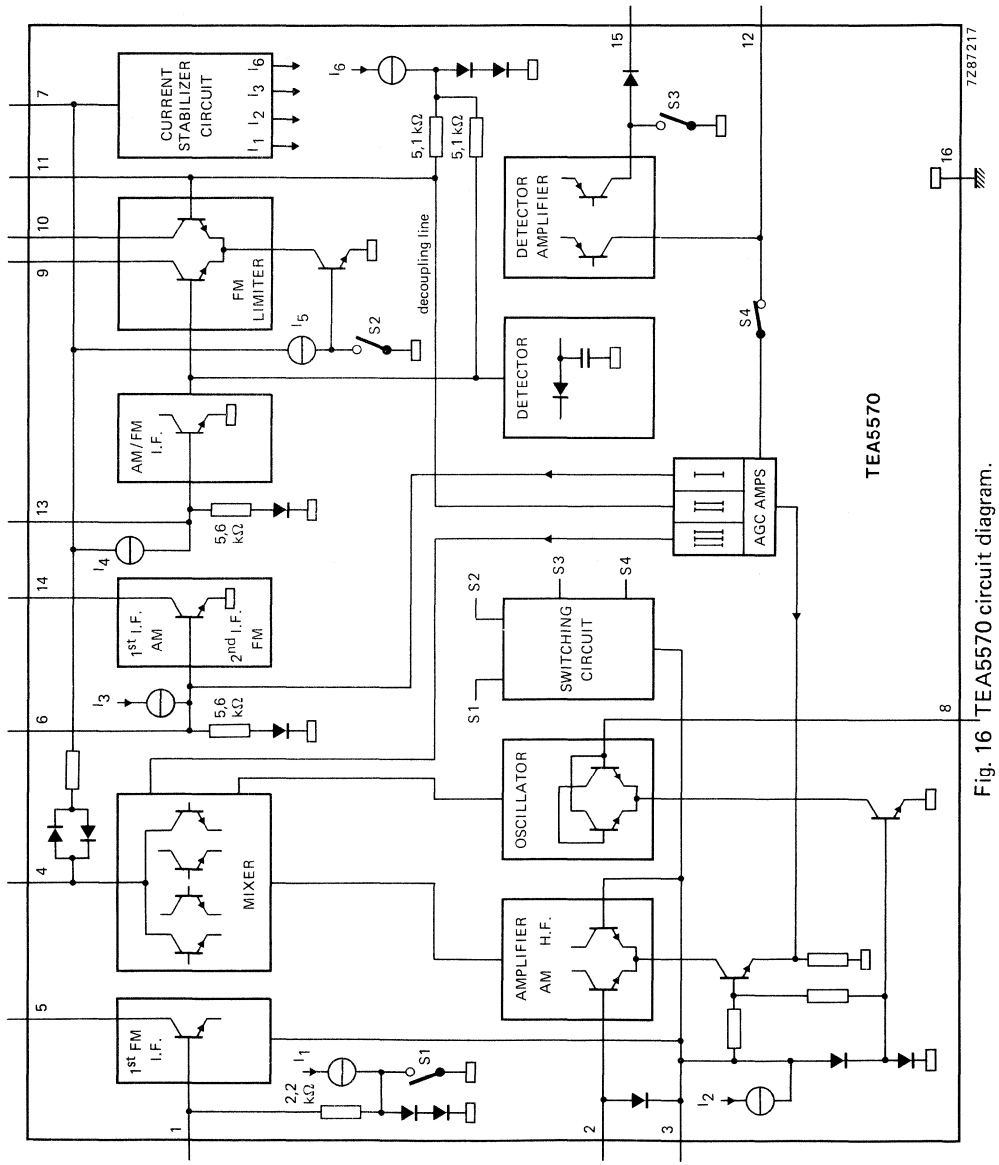


Fig. 16 TEA5570 circuit diagram.

APPLICATION INFORMATION (continued)

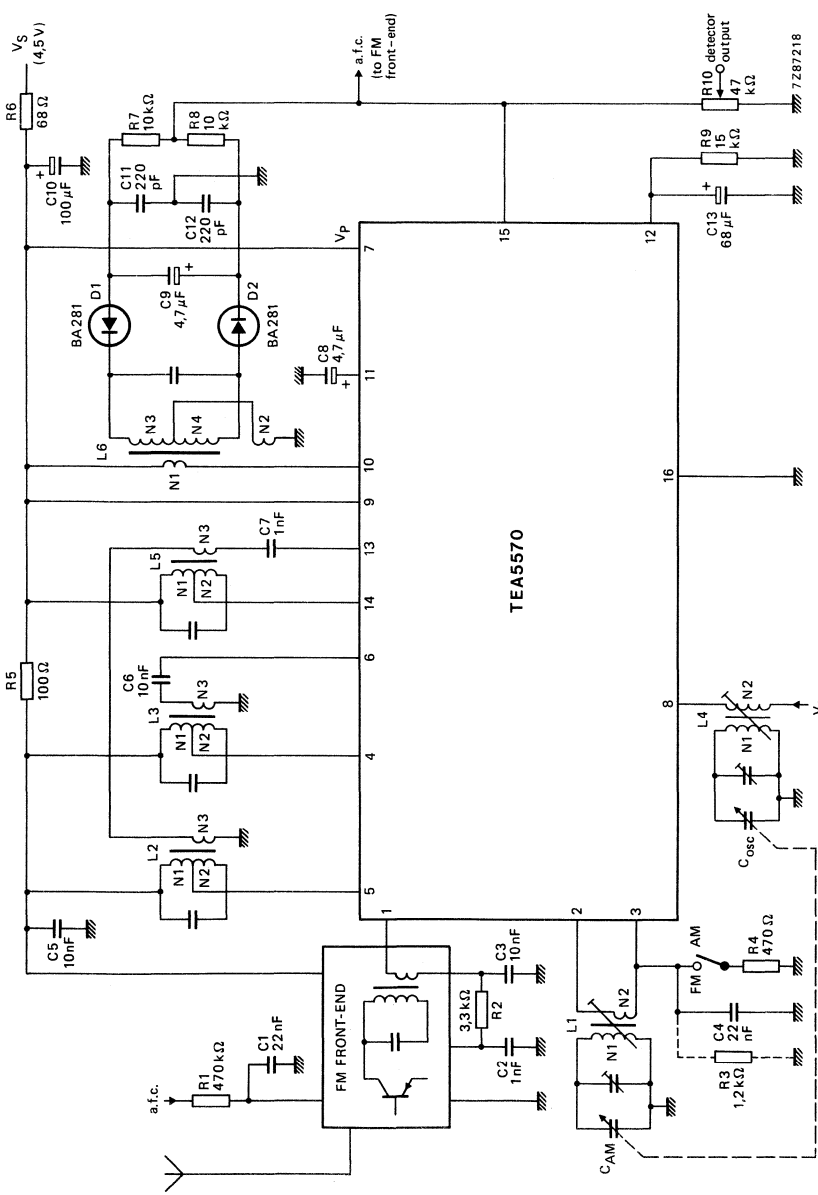


Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.

Coil data

L2	N1 = 3	L3	N1 = 33	L4	N1 = 90	L5	N1 = 33
	N2 = 8		N2 = 113		N2 = 6		N2 = 113
	N3 = 1		N3 = 9				N3 = 9
	C = 82 pF		C = 180 pF				

L6	N1 = 50	
	N2 = 50	
	N3 = 4,5	
	N4 = 6,5	
	C = 82 pF	

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5580 PLL stereo decoder is for car, portable and mains-fed medium-fi radios and radio recorders. It features a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 50 dB, or up to 60 dB with adjustment of the pilot-cancelling resistor (R3, Figs 3 and 4). Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 3,6 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:
  - third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;
  - phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz pilot tone
- IF filter roll-off compensation

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

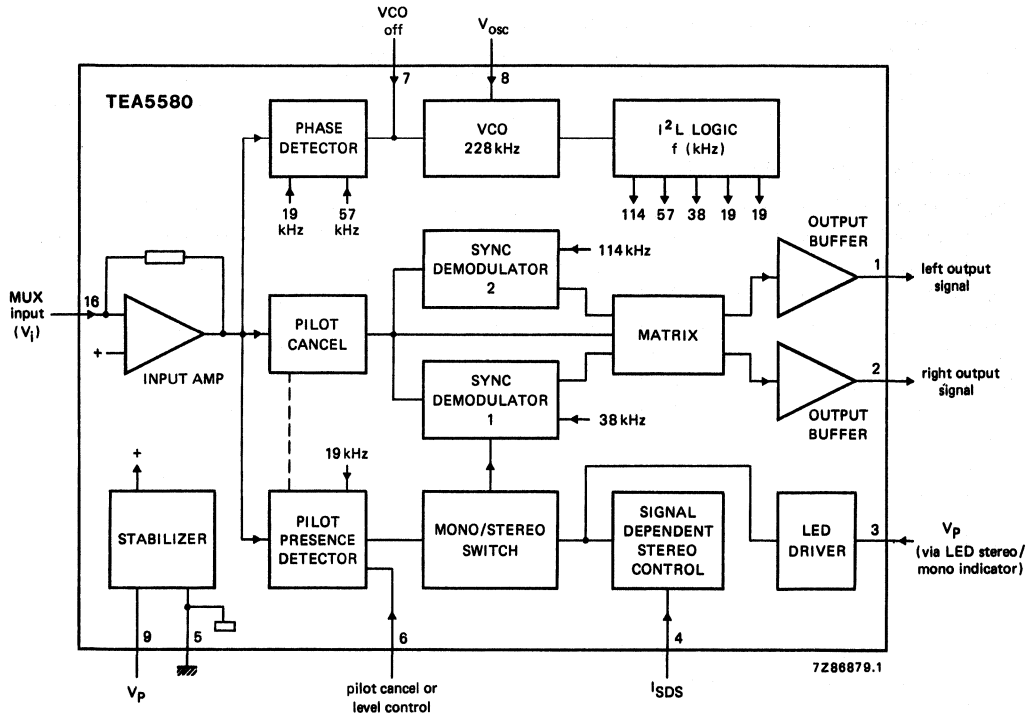


Fig. 1 Block diagram.

Note

Do **not** connect pins 10, 11, 12, 13, 14 or 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pins 3 and 9)	V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)	$-I_{3M}$	–	75	mA
Total power dissipation	P_{tot}	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 75 K/W

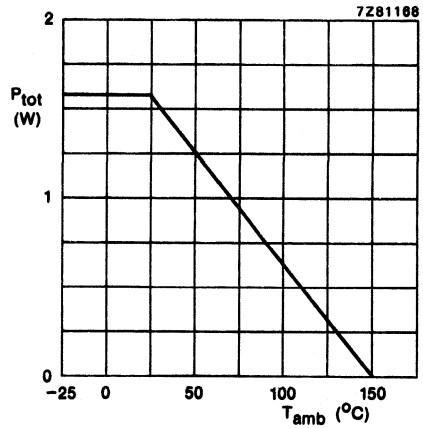


Fig. 2 Power derating curve.

CHARACTERISTICS

Measured in the circuit of Fig. 3; V_P = 7,5 V; T_{amb} = 25 °C; all d.c. voltages are with respect to pin 5; all currents are positive into the IC; a.c. measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV; f_m = 1 kHz; de-emphasizing time = 50 μs; oscillator adjusted to I_{osc} at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R1 and C1 in Fig. 3); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
D.C. Characteristics					
Supply voltage (note 1)	V_P	3,6	7,5	16	V
Total current consumption at V_P = 7,5 V (note 2)	I_P	–	10	13,5	mA
Dissipation at V_P = 7,5 V (note 2)	P_{tot}	–	75	–	mW
Bias voltage (pin 16)	V_{16-5}	–	1,4	–	V
Input current (pin 4)	I_4	–	–	400	μA
D.C. output current (pin 1)	$-I_1$	195	275	390	μA
D.C. output current (pin 2)	$-I_2$	195	275	390	μA
Output current (pin 3) (LED driver transistor)	$-I_3$	–	–	50	mA
Switch "VCO-OFF" voltage at pin 7	V_{off}	–	2,2	–	V
Switch "VCO-OFF" current into pin 7	I_7	–	–	50	μA
A.C. Characteristics					
Overall gain (mono)	Go (V_o/V_i)	7	8	9,5	dB
Gain input amplifier (adjustable) (Fig. 5)	G	0	–	20	dB
AF output voltage (mono) (r.m.s. value)	$V_{1-5} = V_{2-5}$	800	900	–	mV
Output channel unbalance	$\Delta V_o/V_o$	–	± 0,2	± 1,0	dB
Total harmonic distortion at $V_{o(rms)}$ = 0,9 V (note 3)	THD	–	0,2	0,5	%
Total harmonic distortion at $V_{o(rms)}$ = 1,0 V	THD	–	1,0	–	%
Channel separation L = 1; R = 0	α	26	40	–	dB
Signal-to-noise ratio bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
Bandwidth IEC 79 (A-curve)	S/N	–	82	–	dB
Input impedance (external)	$\lvert Z_i \rvert$	–	47	–	kΩ
Output impedance (external) R = 12 kΩ; C = 3,9 nF	$\lvert Z_o \rvert$	–	9,3	–	kΩ

parameter	symbol	min.	typ.	max.	unit
SDS control (Fig. 6)					
10 dB channel separation	I_4	–	50	–	μA
Full stereo channel separation > 26 dB	I_4	100	–	–	μA
Full mono channel separation < 1 dB	I_4	–	–	10	μA
Stereo/mono switch					
R3 = 180 kΩ; note 4; Fig. 7					
Switching to stereo	V_i	–	18	24	mV
Switching to mono	V_i	8	–	–	mV
Hysteresis	ΔV_i	–	4	–	mV
Carrier and harmonic suppression at the output (note 5)					
Pilot signal suppression f = 19 kHz; R3 = 180 kΩ; note 4; Fig. 4	α_{19}	40	50	–	dB
Subcarrier suppression					
f = 38 kHz	α_{38}	–	50	–	dB
f = 57 kHz	α_{57}	–	50	–	dB
f = 228 kHz	α_{228}	–	80	–	dB
Intermodulation suppression (note 6)					
f_m = 10 kHz; spurious signal f_s = 1 kHz	α_2	–	60	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	α_3	–	60	–	dB
VWF tone suppression f = 57 kHz (note 7)	α_{57}	–	80	–	dB
SCA tone rejection f = 67 kHz (note 8)	α_{67}	–	80	–	dB
ACI rejection (note 9)					
f = 114 kHz	α_{114}	–	90	–	dB
f = 190 kHz	α_{190}	–	60	–	dB

Notes see next page.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Ripple rejection					
f = 100 Hz; V_{ripple} = 200 mV; measured including RC network in supply line					
V_P = 7,5 V	RR_{100}	–	42	–	dB
V_P = 6,0 V	RR_{100}	–	46	–	dB
V_P = 3,6 V	RR_{100}	–	35	–	dB
VCO					
Oscillator frequency adjustable with R8	f_{osc}	–	228	–	kHz
Capture range (deviation from 228 kHz centre frequency) V_{pilot} = 9% (note 10)	$\Delta f/f$	–	8	–	%
Temperature coefficient	TC	–	+ 400 x 10^{-6}	–	K^{-1}

Notes to the characteristics

1. Minimum supply voltage only applicable in 6 V portable.
2. Without LED-driver current.
3. Guaranteed for mono, mono + pilot, stereo.
4. Also adjustable.
5. Reference output voltage at 1 kHz (measured channel R, pin 2).
6. Intermodulation suppression (BFC: Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})}\ ;\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})}\ ;\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

7. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz} \pm 23\ \text{Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

8. SCA (Subsidary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 9 kHz})}\ ;\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

9. ACI (Adjacent Channel Interference) rejection at:

$$\alpha_{114} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)}\ ;\ f_s = (3 \times 38\ kHz) - 110\ kHz$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)}\ ;\ f_s = (5 \times 38\ kHz) - 186\ kHz$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

10. The capture range of the PLL may be decreased to 4% by changing the value of C2 to 470 nF (see Fig. 4), if a small ambient temperature range is provided.

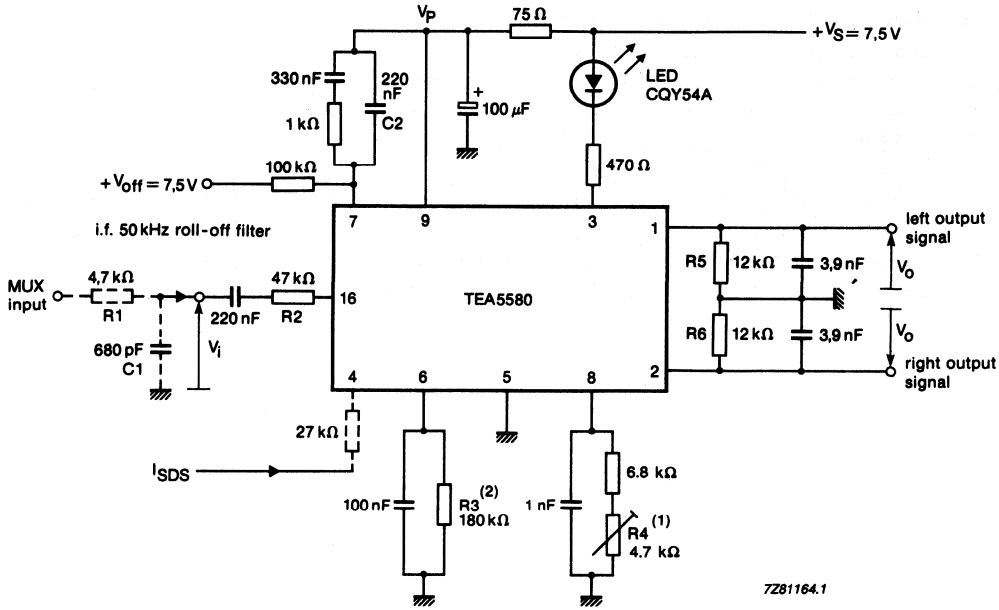


Fig. 3 Car radio application and test circuit.

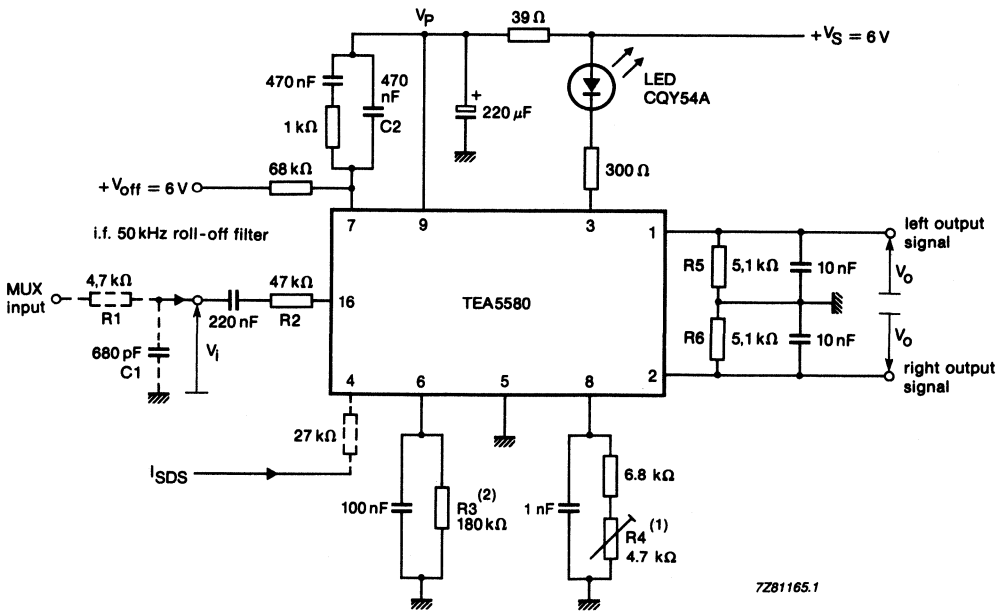
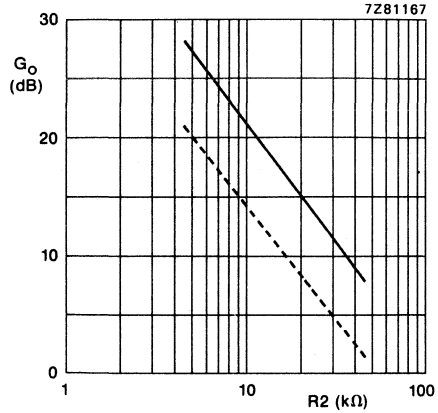


Fig. 4 Portable application circuit.

Notes to Figs 3 and 4

(1) R4: VCO frequency adjustment (228 kHz).

(2) R3: pilot cancelling or pilot level adjustment; best adjustment obtained with 470 kΩ potentiometer (see Figs 7 and 8); adjust for pilot cancellation of approx. 58 dB ± 10 dB and pilot sensitivity (mono to stereo) of approx. 23 mV ± 3 mV.



——— R5 = R6 = 12 kΩ

– – – R5 = R6 = 5,1 kΩ

Fig. 5 Overall gain as a function of input resistance (R2).

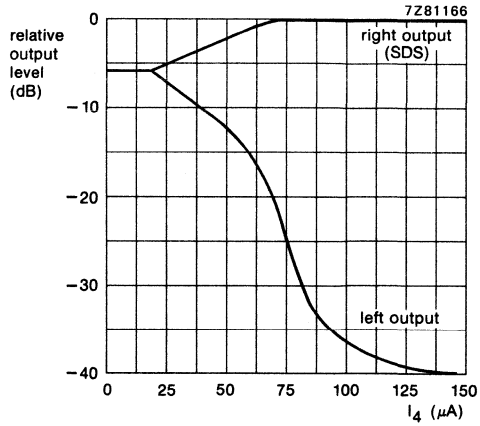
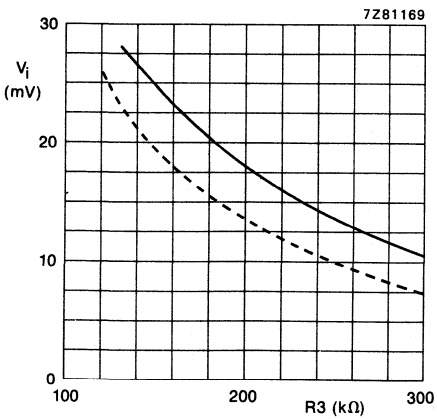


Fig. 6 Relative output level as a function of the signal dependent stereo (SDS) current (I_4); typical curves.



——— stereo "ON"

– – – stereo "OFF"

Fig. 7 Pilot sensitivity: pilot input voltage (V_i) as a function of pilot adjustment resistor R3; typical curves.

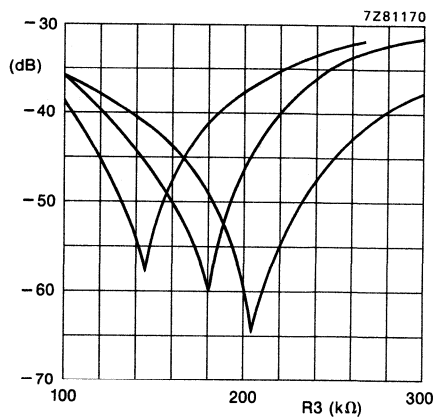


Fig. 8 Random samples of pilot cancelling: $\frac{V_o \text{ (at 19 kHz)}}{V_o \text{ (at 1 kHz)}}$ in dB as a function of R3; $V_{i(p\text{-}p)}$ = 1 V; V_{pilot} = 32 mV (9%).

PLL STEREO DECODER

GENERAL DESCRIPTION

The TEA5581 PLL stereo decoder is for car and medium-fi radios. It incorporates all the features provided by the TEA5580 together with a source selector, muting circuit and output amplifiers with adjustable gain. It also features a switch for radio or cassette function and a 228 kHz voltage-controlled oscillator (VCO) that is locked to the 19 kHz stereo pilot tone by a phase-locked loop (PLL) system. Subcarrier frequencies of 19, 38, 57 and 114 kHz are regenerated via I^2L logic from the VCO output.

The PLL phase detector suppresses phase distortion due to the 57 kHz pilot tone from the German 'Verkehrs Warnfunk' (VWF) traffic warning system. Typical suppression of the 19 kHz stereo pilot tone is 40 dB. Adjacent channel interference is prevented by the use of two demodulators, one driven by the 38 kHz decoding signal and the other at 114 kHz to suppress the third harmonic of the multiplexed input signal.

The gain of the input amplifier can be adjusted by an external resistor and the circuit includes compensation for an IF filter typical roll-off frequency of 50 kHz (2 dB down at 38 kHz).

The supply voltage range of the circuit is 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- Smooth stereo-to-mono change-over at weak signals (signal-dependent stereo channel separation)
- LED driver for stereo/mono indicator
- Suppresses:

  third harmonics (114 kHz) of multiplexed signal to prevent interference from strong adjacent channels;

  phase distortion due to the 57 kHz signal from VWF transmitters
- Pilot cancelling circuit to give added suppression of 19 kHz stereo pilot tone (up to 25 dB)
- IF filter roll-off compensation
- Source selector for radio or cassette input (typ. 90 dB)
- Mute circuit for 90 dB (typ.) muting of the output level
- Matrix and two output buffers with adjustable gain (max. 20 dB)

PACKAGE OUTLINES

TEA5581 : 16-lead DIL; plastic (SOT38).
TEA5581T: 16-lead mini-pack; plastic (SO16L; SOT162A).

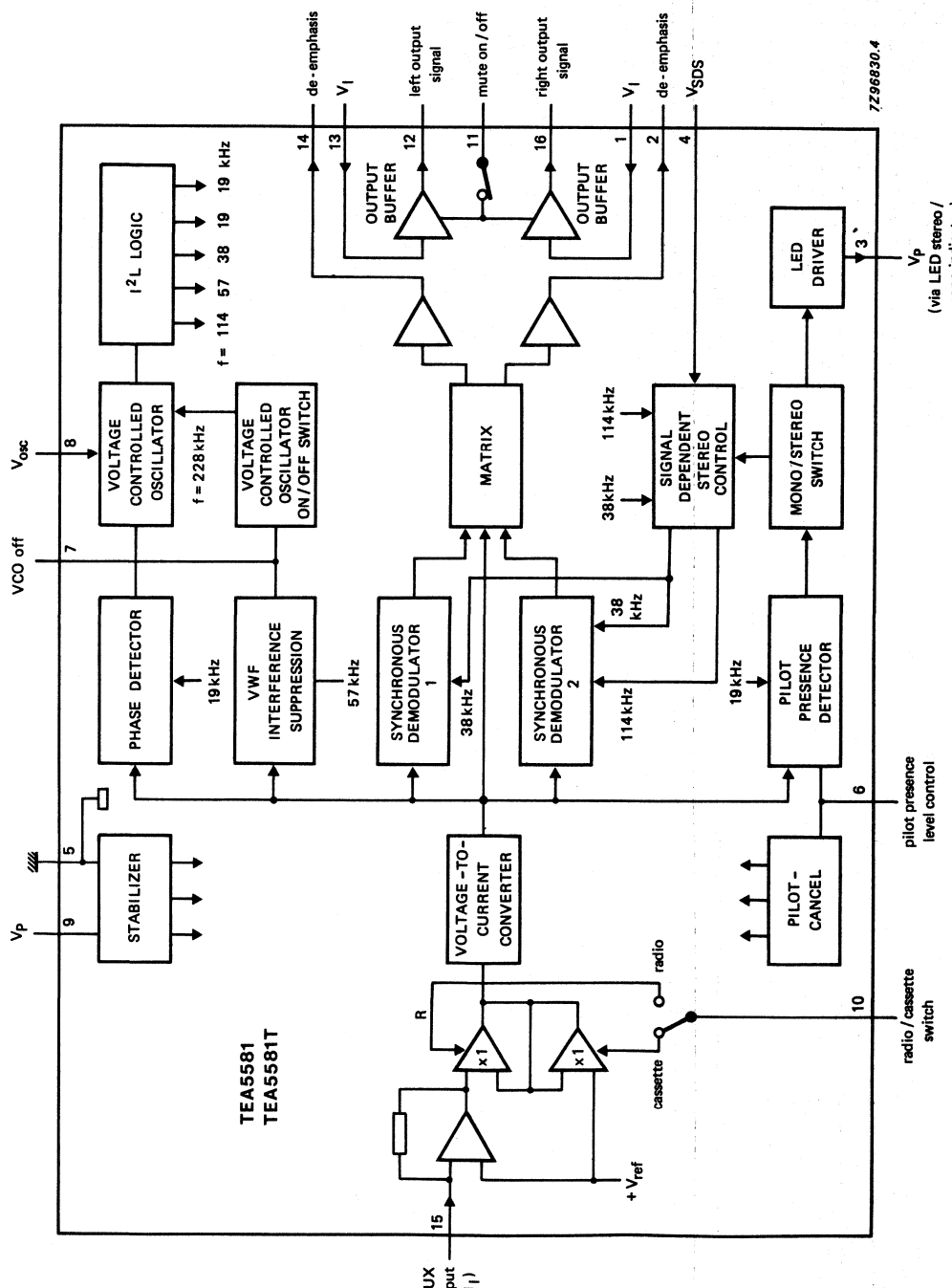


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{3-5}, V_{9-5}	–	18	V
LED-driver current (peak value)		$-I_{3M}$	–	75	mA
Total power dissipation		P_{tot}	see derating curve Fig. 2		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+80	°C
Electrostatic handling *		V_{es}	−600	+600	V

From junction to ambient in free air

SOT38	$R_{th\ j-a}$	75 K/W
SOT162	$R_{th\ j-a}$	95 K/W

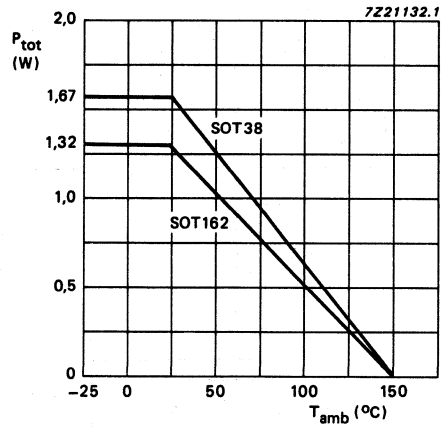


Fig. 2 Power derating curve.

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

DC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; all DC voltages are with respect to pin 5; all currents are positive into the IC.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	R1 = 75 Ω	V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	15	20	mA
Power dissipation		P_{tot}	–	125	–	mW
Voltage						
pin 15		V_{15}	–	2.1	–	V
pins 12 and 16		V_{12}, V_{16}	3.2	3.6	4.0	V
DC output current						
pins 2 and 14		$-I_{14}$, $-I_2$	225	320	450	μA
Output current						
pin 3		$-I_3$	–	–	20	mA
Switch "VCO-OFF"						
voltage		V_7	–	2.2	–	V
Switch "VCO-OFF"						
current		I_7	–	50	75	μA

AC CHARACTERISTICS

Measured in the circuit of Fig. 7; V_S = 8.5 V; T_{amb} = 25 °C; AC measurements have an input MUX-signal of 1 V (peak-to-peak); V_{pilot} = 32 mV (9%); f_m = 1 kHz; oscillator adjusted to 228 kHz at V_i = 0 V; values are measured with an external roll-off network of 50 kHz (2 dB down at 38 kHz) at the input (dashed components R_S and C_S in Fig. 7); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Transimpedance		V_O/I_I	0.13	0.15	0.17	V/μA
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R3 = 47 kΩ	G_o (V_o/V_i)	9.0	10.0	11.0	dB
AF output voltage (RMS value)		$V_{12} = V_{16}$	0.95	1.14	1.33	V
AF output voltage (RMS value)		$V_2 = V_{14}$	–	–	500	mV
Total harmonic distortion	note 1; $V_{O(rms)}$ = 1 V	THD	–	0.1	0.5	%
Output voltage	THD = 1%	$V_{12} = V_{16}$	–	1.5	–	V
Output channel unbalanced		V_{12}/V_{16}	–	0.2	1.0	dB
Channel separation	IF roll-off frequency = 50 kHz L = 1; R = 0	α	26	40	–	dB
S/N ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
SDS control	see Fig. 6					
Channel separation	V_4 = 1.0 V	α	5	10	15	dB
Full stereo	channel separation ⩾ 26 dB	V_4	–	1.2	1.25	V
Full mono	channel separation ⩽ 1 dB	V_4	0.75	0.8	–	V
Stereo/mono switch	note 2; see Fig. 5; R4 = 180 kΩ					
Switching to:						
stereo		V_{pilot}	–	14	20	mV
mono		V_{pilot}	4	–	–	mV
Hysteresis		ΔV_I	–	4.5	–	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f = 19 kHz; R4 = 180 kΩ; note 2; see Figs 3 and 4	α_{19}	32	40	–	dB
Subcarrier suppression						
f = 38 kHz		α_{38}	–	50	–	dB
f = 57 kHz		α_{57}	–	50	–	dB
f = 228 kHz		α_{228}	–	75	–	dB
Intermodulation suppression	note 4					
f_m = 10 kHz	spurious signal f_s = 1 kHz	α_2	–	50	–	dB
f_m = 13 kHz	spurious signal f_s = 1 kHz	α_3	–	50	–	dB
VWF tone suppression						
f = 57 kHz	note 5	α_{57}	–	80	–	dB
SCA tone rejection						
f = 67 kHz	note 6	α_{67}	–	70	–	dB
ACI rejection	note 7					
f = 114 kHz		α_{114}	–	90	–	dB
f = 190 kHz		α_{190}	–	60	–	dB
Ripple rejection						
Ripple rejection	f = 100 Hz; V_{ripple} = 100 mV; mono	RR_{100}	–	50	–	dB
VCO						
Oscillator frequency adjustable with R5		f_{osc}	–	228	–	kHz
Capture range	deviation from 228 kHz centre frequency; V_{pilot} = 32 mV	$\Delta f/f$	–	6	–	%
Temperature coefficient	uncompensated	TC	–	-200×10^{-6}	–	K^{-1}

parameter	conditions	symbol	min.	typ.	max.	unit
Source selector						
Suppression of MPX signal	$V_{10} \geqslant 2$ V	α	80	90	–	dB
Switching level	cassette to radio					
voltage		V_{IL}	–	–	0.8	V
current		I_{IL}	–	10	25	μA
Switching level	radio to cassette					
voltage		V_{IH}	2.0	–	V_S	V
current		I_{IH}	–	–	1	μA
Output amplifiers						
Gain	note 8; R_6/R_7	G_v	–	–	20	dB
Output impedance		Z_o	–	200	500	Ω
External load impedance		$\|Z_I\|$	5	–	–	kΩ
Suppression (mute)	$V_{11} = \leqslant 0{,}8$ V	α	84	90	–	dB
DC offset voltage at outputs during mute switching	mute OFF-to-ON	ΔV_{12}, ΔV_{16}	–	1.0	–	mV
	mute ON-to-OFF	ΔV_{12}, ΔV_{16}	–	2.0	–	mV
Muting circuit						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2.0	–	V_S	V
Input current	mute ON	I_{IL}	–	10	25	μA
	mute OFF	I_{IH}	–	–	1	μA

Notes to the characteristics

1. Guaranteed for mono, mono + pilot and stereo.
2. Also adjustable.
3. Reference output voltage at 1 kHz (measured channel R, pin 16).
4. Intermodulation suppression (Beat-Frequency Components):

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 10\text{ kHz}) - 19\text{ kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 13\text{ kHz}) - 38\text{ kHz}$$

measured with 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

5. Traffic radio (VWF) tone suppression:

$$\alpha_{57} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 1\text{ kHz} \pm 23\text{ Hz})}$$

measured with 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 kHz; 60% AM modulated with f_{mod} = 23 Hz).

6. SCA (Subsidiary Communication Authorization) tone rejection:

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 9\text{ kHz})};\ f_s = (2 \times 38\text{ kHz}) - 67\text{ kHz}$$

measured with 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

7. ACI (Adjacent Channel Interference) rejection at:

$$\alpha 114 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (3 \times 38\text{ kHz}) - 110\text{ kHz}$$

$$\alpha 190 = \frac{V_{o(signal)}\ (\text{at } 1\text{ kHz})}{V_{o(spurious)}\ (\text{at } 4\text{ kHz})};\ f_s = (5 \times 38\text{ kHz}) - 186\text{ kHz}$$

measured with 90% mono signal; f_s = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

8. Maximum permitted value of feedback resistor = 220 kΩ.

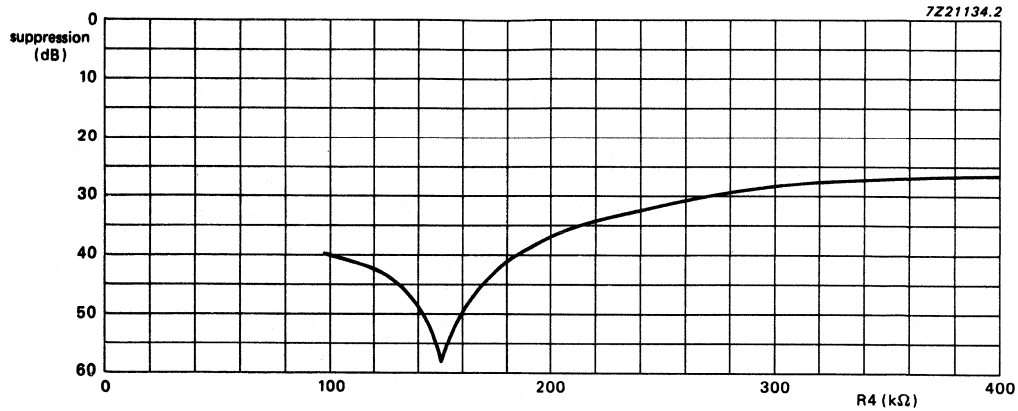
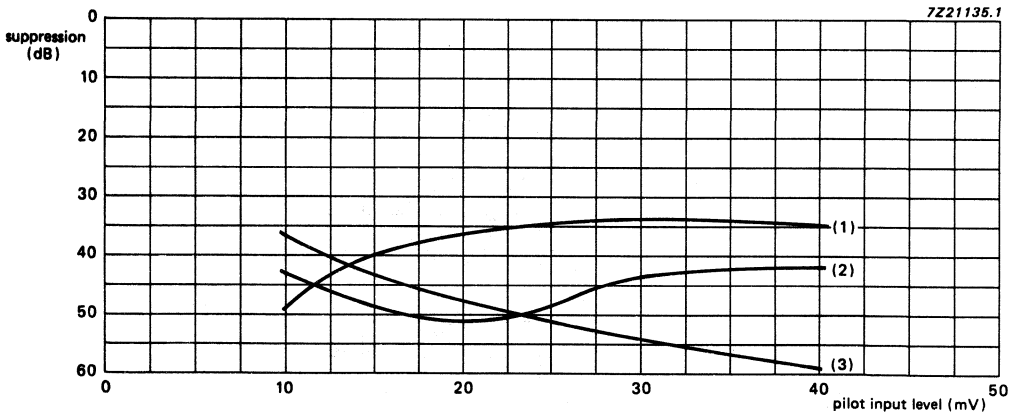
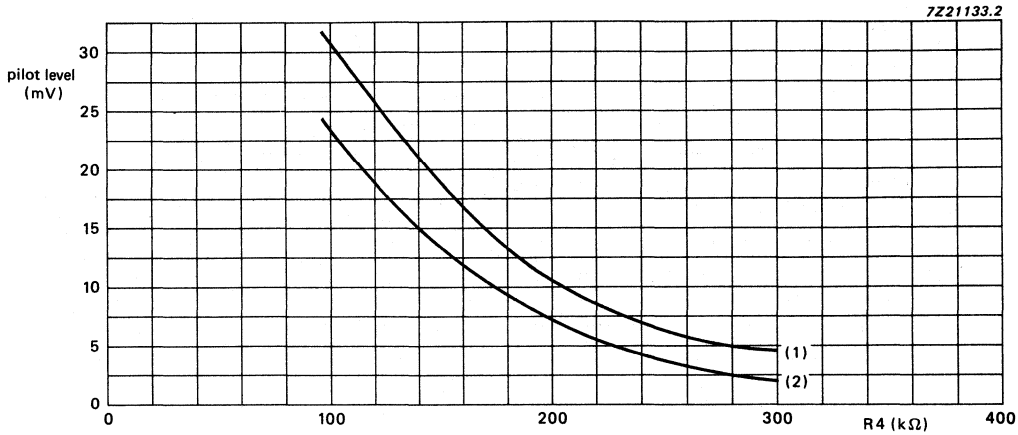


Fig. 3 Pilot suppression plotted against resistance (R4).



(1) 220 kΩ
(2) 180 kΩ
(3) 150 kΩ

Fig. 4 Pilot suppression plotted against pilot input voltage level.



(1) Switching from mono to stereo.
(2) Switching from stereo to mono.

Fig. 5 Pilot sensitivity against resistance (R4).

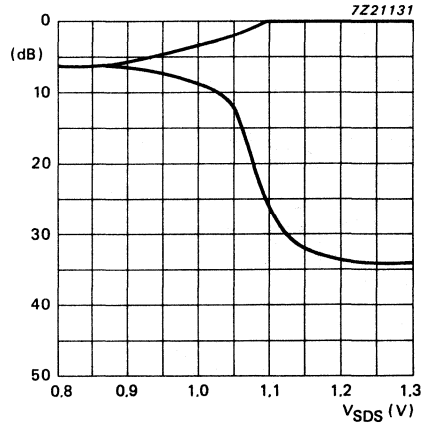
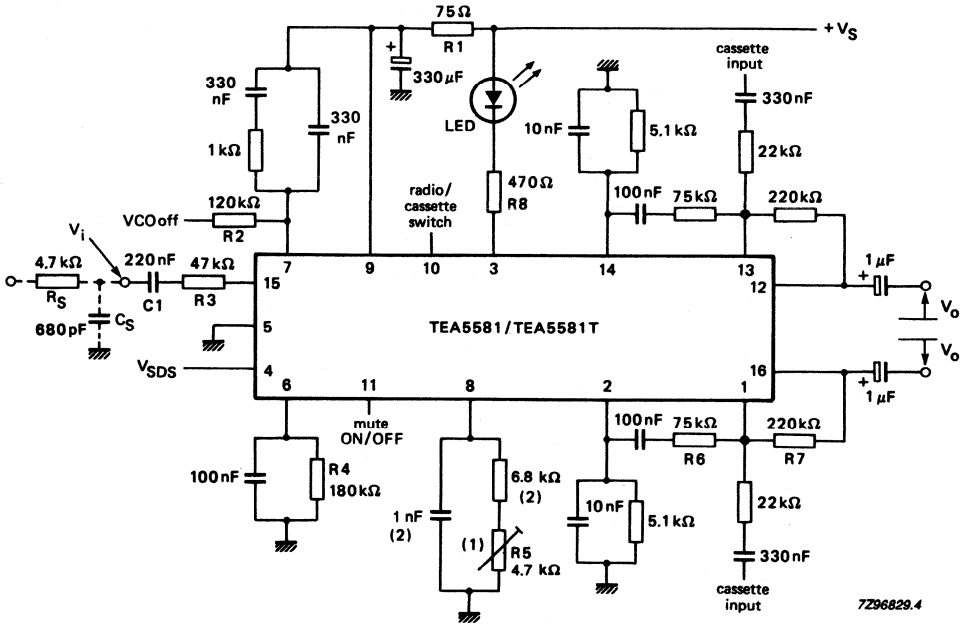


Fig. 6 Channel separation against V_{SDS}.

APPLICATION INFORMATION



(1) 25% tolerance (all other resistors have a 5% tolerance).
(2) 1% tolerance (NP0).

Fig. 7 Application diagram.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591 is an integrated radio circuit which is designed for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. The main advantage of this IC is its ability to operate over a wide range of supply voltages without loss of performance. The AM circuit incorporates a balanced mixer and a 'one-pin' oscillator, which operates in the 0.6 MHz to 30 MHz frequency range, with amplitude control. The circuit also includes an IF amplifier, a detector and an AGC circuit which controls the IF amplifier and the mixer. The FM circuit incorporates an RF amplifier, a balanced mixer and a 'one-pin' oscillator together with two AC coupled IF amplifiers (with distributed selectivity), a quadrature demodulator for the ceramic filter and internal AFC.

Features

- DC AM/FM switch facility
- Three internal separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 9) are ESD protected

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	3.0	15	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 13)	m = 0.3					
RF sensitivity						
RF input voltage	V_o = 10 mV	V_i	–	3.5	–	μV
RF input voltage	(S+N)/N = 26 dB	V_i	–	17	–	μV
Signal plus noise-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.7	–	%
FM performance (pin 1)	Δf = 22.5 kHz					
RF sensitivity,						
RF input voltage						
−3 dB before limiting		V_i	–	2.3	4.0	μV
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)	V_i = 3.0 μV	(S+N)/N	23	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

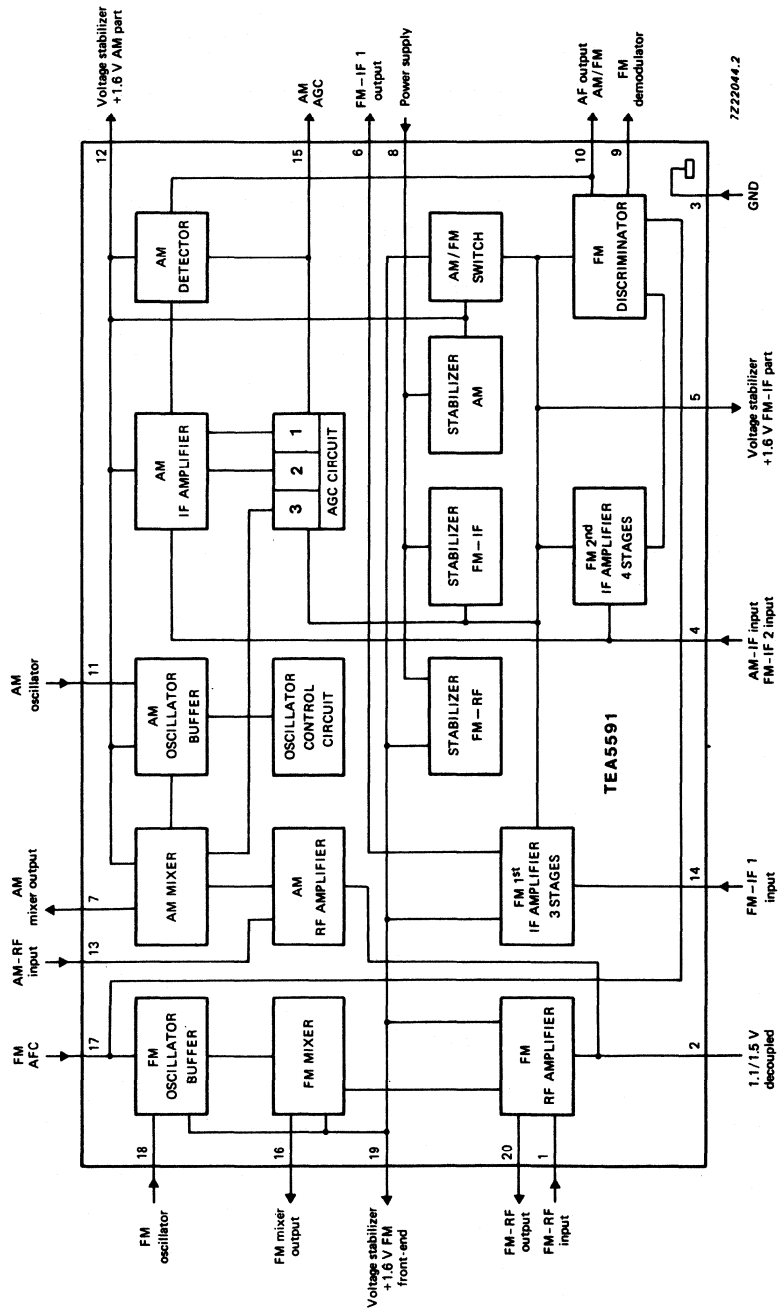


Fig.1 Block diagram.

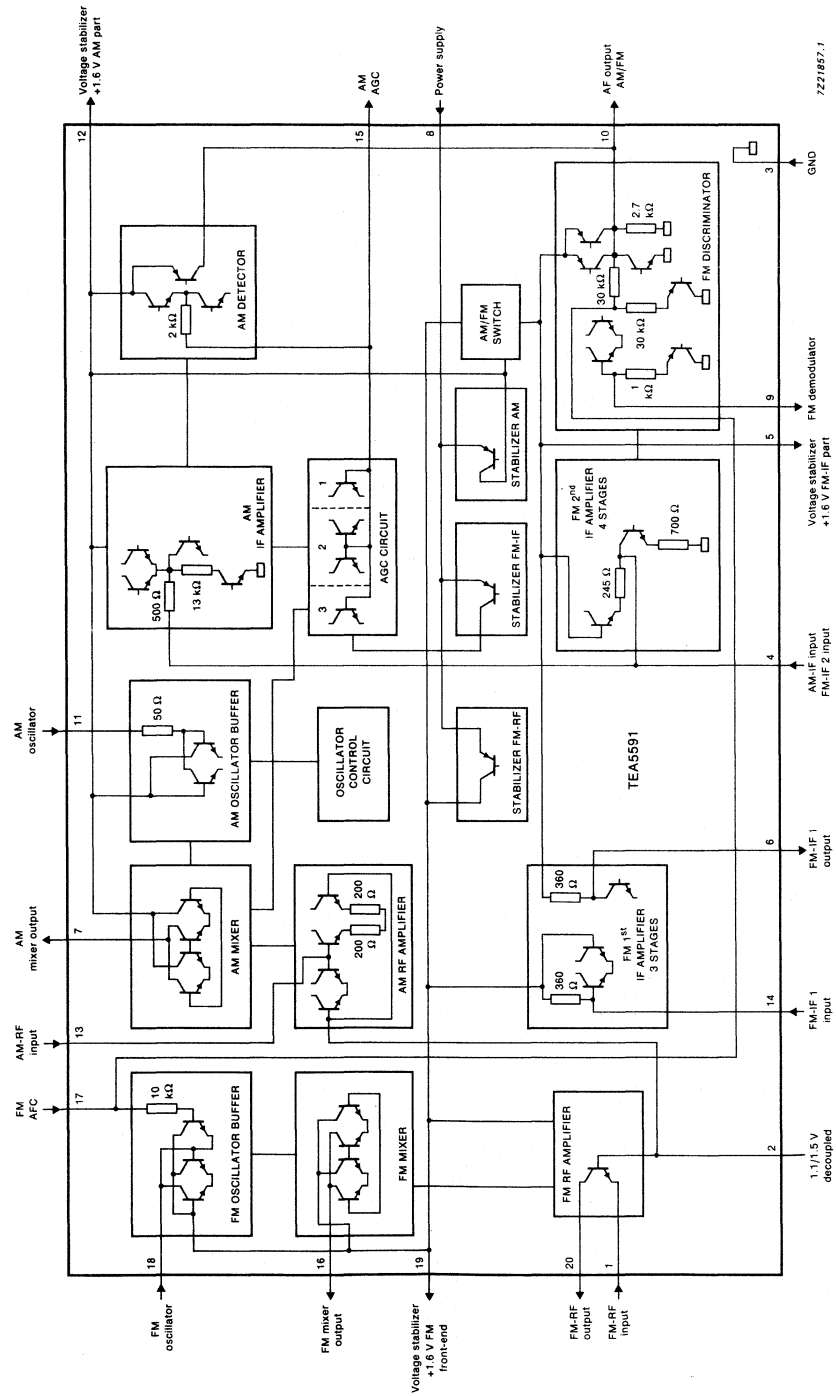


Fig.2 Equivalent circuit diagram.

PINNING

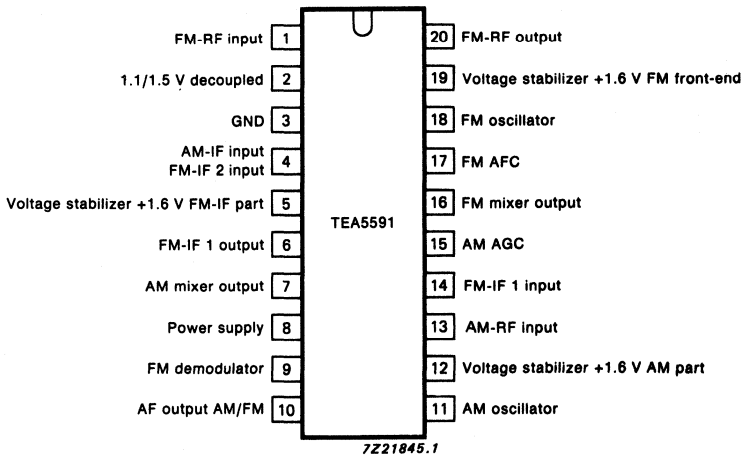


Fig.3 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−15	+ 60	°C
Total power dissipation		P_{tot}	see Fig.4		

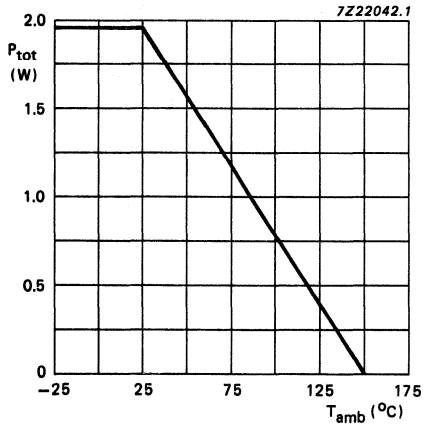


Fig.4 Power derating curve.

DC CHARACTERISTICS

All voltages are referenced to pin 3; all input currents are positive; all parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 1		V_1	–	0.90	–	V
pin 2		V_2	–	1.60	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	1.5	1.60	1.75	V
pin 6		V_6	–	1.48	–	V
pin 9		V_9	–	1.05	–	V
pin 14		V_{14}	–	1.63	–	V
pin 17		V_{17}	–	0.60	–	V
pin 19		V_{19}	–	1.60	–	V
Voltages (AM)						
pin 2		V_2	–	1.10	–	V
pin 12		V_{12}	–	1.60	–	V
pin 15		V_{15}	–	1.54	–	V
Supply current						
AM part		$I_{P(AM)}$	–	14	19	mA
FM part		$I_{P(FM)}$	–	17	23	mA

AC CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PART						
Input conductance pin 4	f = 0.5 MHz	g_{ie}	–	1.7	–	ms
Input capacitance pin 4	f = 0.5 MHz	C_{ie}	–	5	–	pF
Input conductance pin 13	f = 1.0 MHz	g_{ie}	–	230	–	µs
Input capacitance pin 13	f = 1.0 MHz	C_{ie}	–	13	–	pF
Output conductance pin 7	f = 0.5 MHz	g_{oe}	–	4	–	µs
Output capacitance pin 7	f = 0.5 MHz	C_{oe}	–	4.7	–	pF
Conductance pin 11	f = 1.5 MHz	g_e	–	–6.8	–	ms
Capacitance pin 11	f = 1.5 MHz	C_e	–	25	–	pF
FM PART						
Input conductance pin 4	f = 10.7 MHz	g_{ie}	–	2.7	–	ms
Input capacitance pin 4	f = 10.7 MHz	C_{ie}	–	6	–	pF
Input conductance pin 14	f = 10.7 MHz	g_{ie}	–	2.8	–	ms
Input capacitance pin 14	f = 10.7 MHz	C_{ie}	–	2.5	–	pF
Output conductance pin 6	f = 10.7 MHz	g_{oe}	–	2.8	–	ms
Output capacitance pin 6	f = 10.7 MHz	C_{oe}	–	3.0	–	pF
Output conductance pin 16	f = 10.7 MHz	g_{oe}	–	1.6	–	µs
Output capacitance pin 16	f = 10.7 MHz	C_{oe}	–	4.5	–	pF
Conductance pin 9	f = 10.7 MHz	g_e	–	880	–	µs
Capacitance pin 9	f = 10.7 MHz	C_e	–	3.6	–	pF
Conductance pin 18	f = 100 MHz	g_e	–	–4	–	ms
Capacitance pin 18	f = 100 MHz	C_e	–	10	–	pF

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified.
RF conditions: Input frequency 1 MHz; 30% modulation where f_{mod} = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM PERFORMANCE						
RF sensitivity						
AF output voltage for: V_i = 7.5 μV	no AGC	V_o	16	30	40	mV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage of V_i = 17 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	48	–	dB
Optimum source impedance		Z_S	–	1.8	–	kΩ
Noise factor	optimum noise impedance	NF	–	4	–	dB
AGC						
Change in RF input voltage for 10 dB change in output voltage	V_{i1} = 100 mV	V_{i1}/V_{i2}	80	86	–	dB
AF output voltage	V_i = 100 μV	V_o	40	50	60	mV
Total harmonic distortion	V_i = 100 μV to 10 mV	THD	–	0.7	1.5	%
	V_i = 100 μV to 10 mV; m = 0.8	THD	–	3	5	%
	V_i = 80 mV; m = 0.8	THD	–	–	8	%

Transimpedance (Z_{tr}) = v_4/i_7 = 900Ω.

parameter	conditions	symbol	min.	typ.	max.	unit
IF suppression (note 1)	V_o = 30 mV	α	–	20	–	dB
Oscillator (pin 11)						
Input voltage	f_{osc} = 1.5 MHz	V_{osc}	–	150	190	mV
	f_{osc} = 30.5 MHz	V_{osc}	–	150	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
Temperature behaviour	–15 to + 60 °C (only the IC)					
Sensitivity		ΔV_i	–	–2	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	1	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	500	–	Hz
MW		Δf_{osc}	–	300	–	Hz
SW		Δf_{osc}	–	100	–	kHz
Supply voltage behaviour	V_P = 1.8 to 15 V					
Sensitivity		ΔV_i	–	0	–	dB
Output voltage	V_i = 1 mV	ΔV_o	–	0.5	–	dB
Oscillator frequency						
LW		Δf_{osc}	–	6	–	kHz
MW		Δf_{osc}	–	0.1	–	kHz
SW		Δf_{osc}	–	30	–	kHz

AC CHARACTERISTICS

All parameters are measured in Fig.5 at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

RF conditions: Input frequency 100 MHz; frequency deviation f = ± 22,5 kHz and f_{mod} = 1 kHz

parameter	conditions	symbol	min.	typ.	max.	unit
FM PERFORMANCE						
RF sensitivity						
RF input voltage	−3 dB before limiting	V_{iFM}	–	2.3	4.0	μV
Noise						
Signal plus noise-to-noise ratio for:						
RF input signal voltage (V_i)						
V_i = 3.0 μV		(S + N)/N	23	26	–	dB
V_i = 1 mV		(S + N)/N	–	60	–	dB
Optimum source impedance		Z_{source}	–	50	–	Ω
Noise factor	optimum source impedance	NF	–	6	–	dB
AF output voltage	V_i = 100 μV	V_o	75	90	–	mV
Total harmonic distortion	V_i = 30 μV to 50 mV	THD	–	0.8	–	%
	V_i = 1 mV; Δf = 75 kHz	THD	–	3	–	%
	V_i = 100 mV; Δf = 75 kHz	THD	–	3	–	%
AM suppression	note 2					
RF input signal	V_i = 100 μV to 10 mV	AMS	–	50	–	dB
Oscillator voltage (pin 18)	f_{osc} = 100 MHz	V_{osc}	–	220	–	mV
	V_P = 1.5 V	V_{osc}	100	–	–	mV
IF rejection ratio		IF_{rr}	–	60	–	dB
AFC	f_{osc} = 111.2 MHz					
	V_{17} = 1.4 V	Δf	–	−620	–	kHz
	V_{17} = 0.2 V	Δf	–	+420	–	kHz

parameter	conditions	symbol	min.	typ.	max.	unit
Temperature behaviour	−15 to +60 °C (only the IC)					
RF sensitivity	−3 dB limiting	ΔV_i	–	−6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	−2	–	dB
Oscillator frequency		Δf_{osc}	–	−0.3	–	%
Supply voltage behaviour	Vp = 1.8 to 15 V					
RF sensitivity	−3 dB limiting	ΔV_i	–	6	–	dB
Output voltage	V_i = 100 μV	ΔV_o	–	0.5	–	dB
Oscillator frequency		Δf_{osc}	–	100	–	kHz
Oscillator voltage		ΔV_{osc}	–	1.0	–	dB

Notes to the AC characteristics

1. $\alpha = \frac{V_i \text{ at } f_i = 455 \text{ kHz}}{V_i \text{ at } f_i = 1 \text{ MHz}}$.
2. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

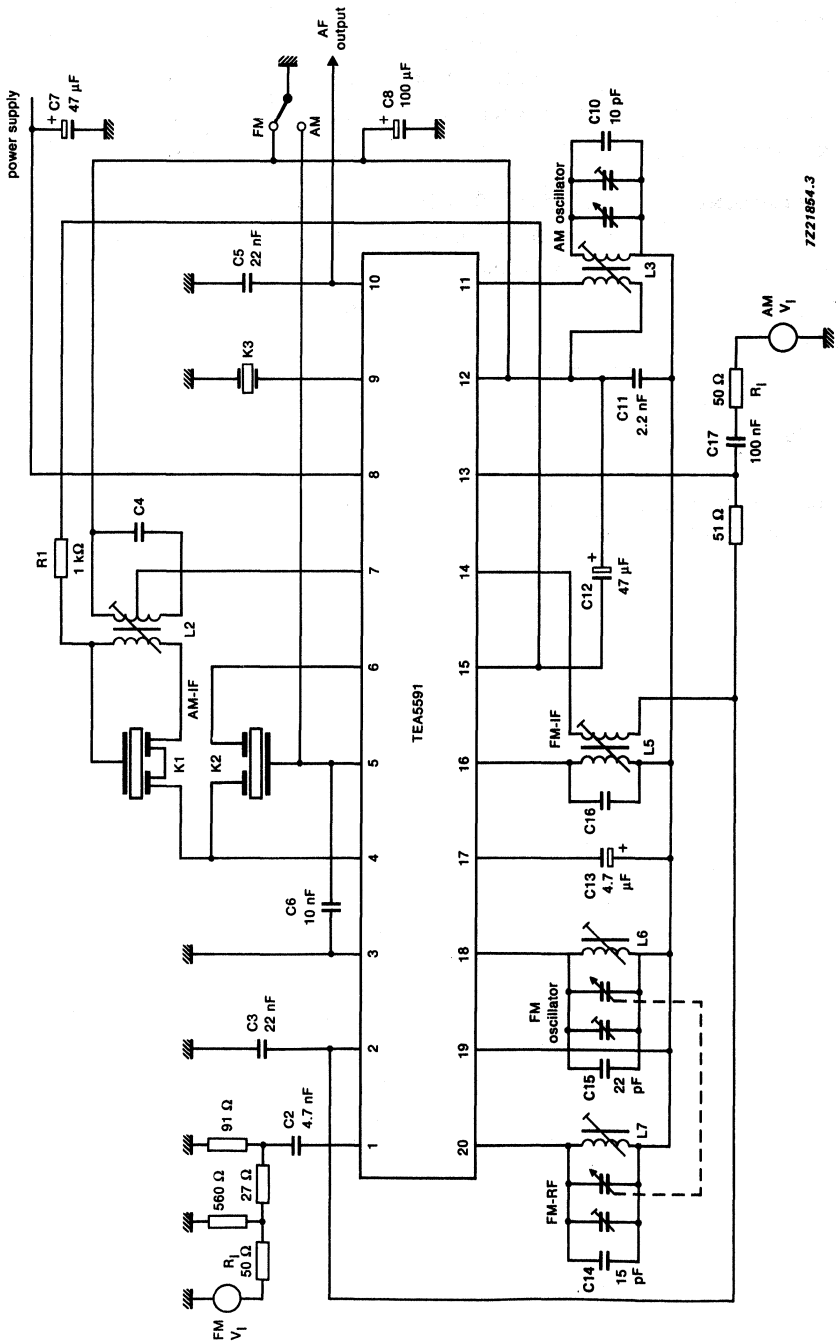


Fig.5 Test circuit.

APPLICATION INFORMATION

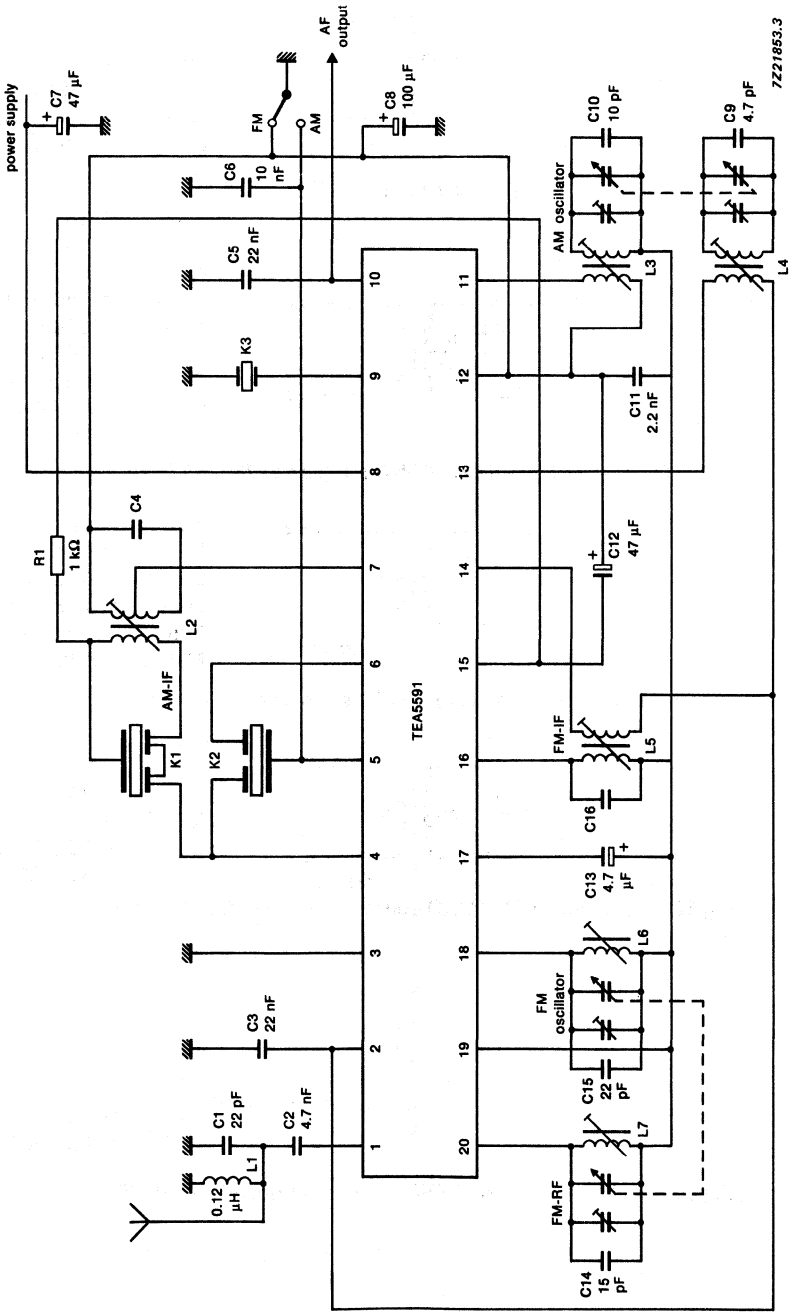
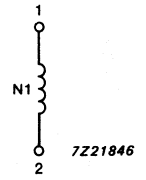


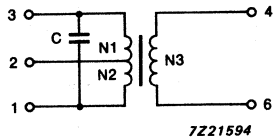
Fig.6 Application diagram.

Component data



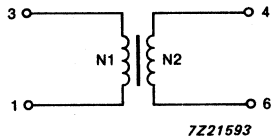
N1 = 4.5
L = 0.12 μH
Wire = 0.8 mm diameter
diameter = 4.5 mm

Fig.7 FM BFP coil (L1).



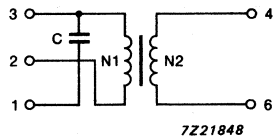
N1 = 132
N2 = 14
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
fo = 468 kHz
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7MCS

Fig.8 AM IF coil (L2). TOKO sample no. 7MCS-7P.



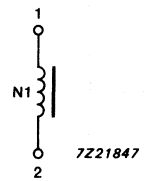
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type 7P-TOKO
Material 7BRS

Fig.9 Oscillator coil (L3). TOKO sample no. 7BRS-7P.



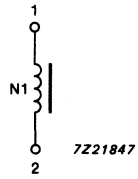
N1 = 11
N2 = 2
C = 85 pF (internal)
fo = 10.7 MHz

Fig.10 FM IF coil (L5). TOKO equivalent no. 119ACS-30120M.



N1 = 1.5
L = 0.03 μH

Fig.11 Oscillator coil (L6). TOKO equivalent no. 301SN-0100.



N1 = 2.5
L = 0.05 μH

Fig.12 FM RF coil (L7). TOKO equivalent no. 301SN-0200.

Ferroceptor coil

L4: N1 = 105; N2 = 10; L = 625 μH

Ceramic Filters

AM IF (K1). SFZ468 HL.
FM IF (K2). SFE10 . 7 MS2.
FM detector (K3). CDA10 . 7 MC1.

Tuning capacitors

AM 140/82 pF
FM 2 x 20 pF

APPLICATION INFORMATION (continued)

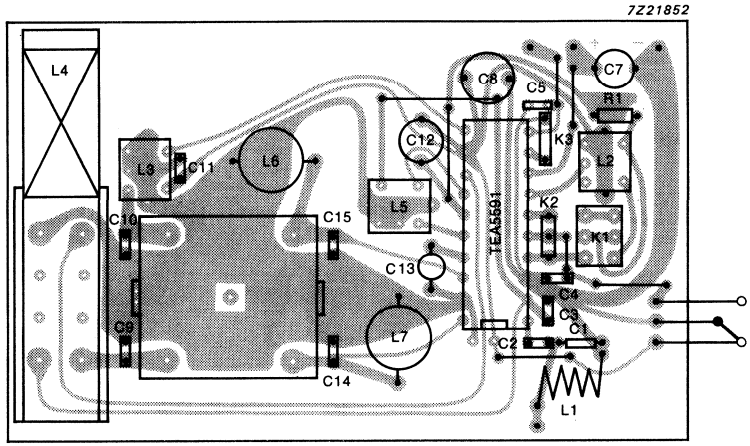


Fig.13 Printed-circuit board component side, showing component layout. For circuit diagram see Fig.6.

Physical dimensions of the printed circuit board = 5.0 x 8.1 cm.

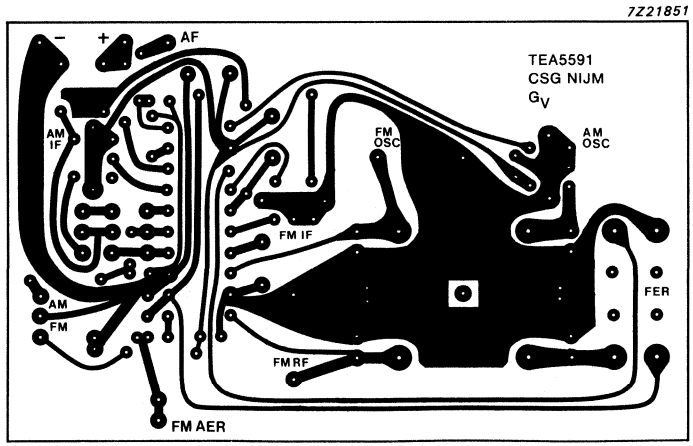


Fig.14 Printed-circuit board showing track side.

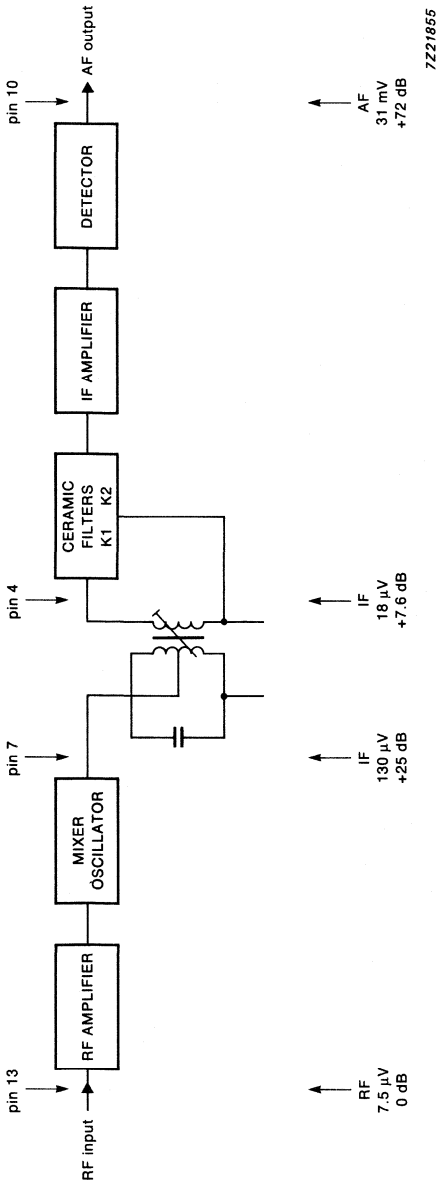


Fig.15 AM signal levels.

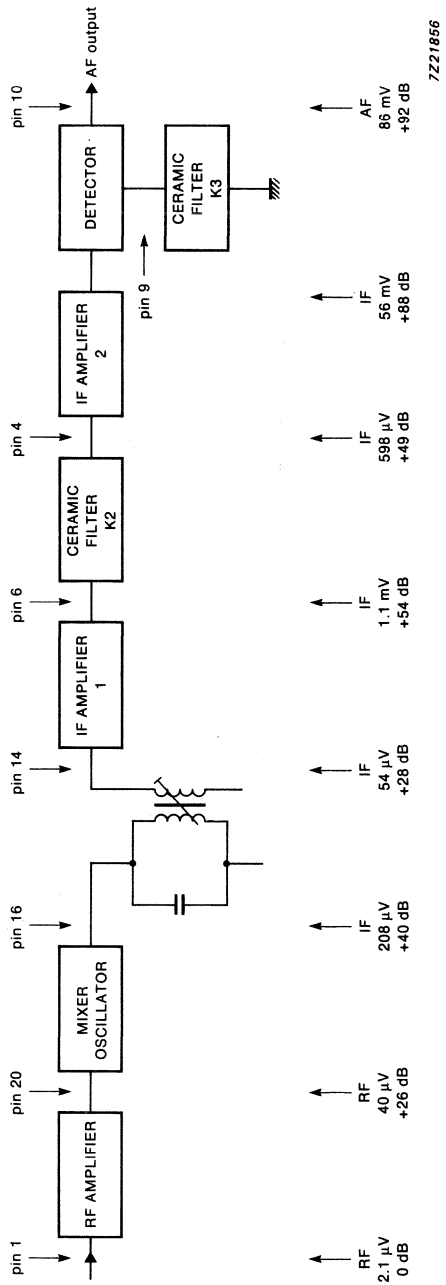


Fig.16 FM signal levels.

APPLICATION INFORMATION (continued)

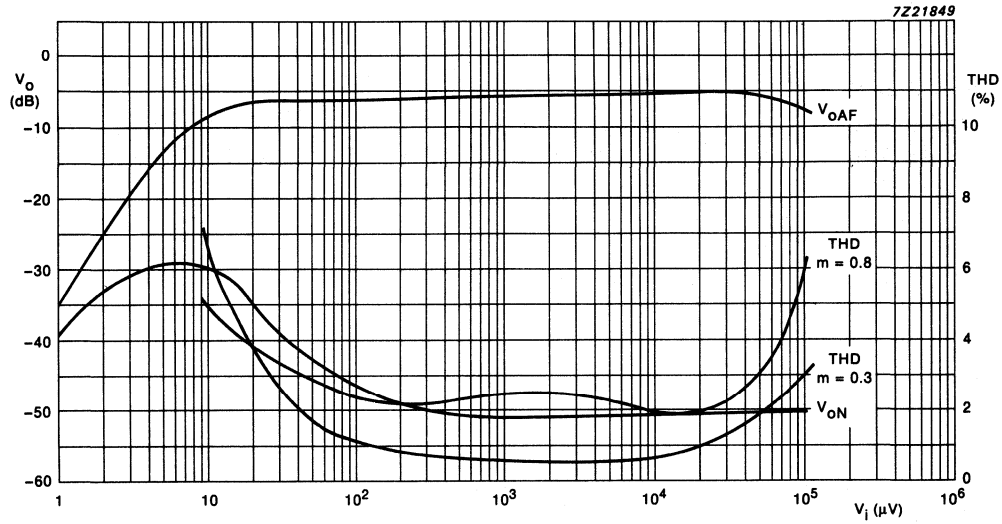


Fig.17 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV, and total harmonic distortion (THD) as a function of input voltage (V_i) at pin 13. Measured in test circuit Fig.5. AM AGC is measured at f_i = 1 MHz; f_{mod} = 1 kHz; m = 0.3. AM distortion is measured at f_i = 1 MHz; f_{mod} = 1 kHz.

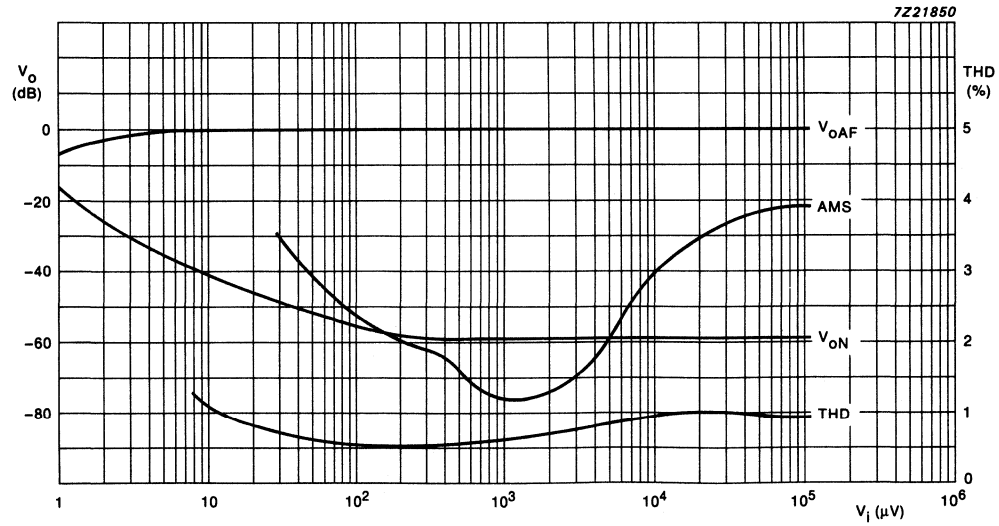


Fig.18 Signal and noise (V_{oAF}), noise (V_{oN}); reference level 0 dB = 100 mV; AM suppression (AMS) and total harmonic distortion (THD) as a function of input voltage (V) at pin 1. Measured in test circuit Fig.5 at f_i = 98 MHz; f_{mod} = 1 kHz; Δf 22.5 kHz. AM suppression is measured at f_{mod} = 400 Hz, m = 0.3 for AM; f_{mod} = 1 kHz, Δf = 75 kHz for FM.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5591A is a 24-pin integrated radio circuit, derived from the TEA5591 and is designed for use in AM/FM portable radios and clock radios. The TEA5591A differs from the TEA5591 in that it has:

- Separate IF input pins for AM and FM
- A split-up AM-IF stage (for distributed selectivity)
- An LED driver indicator

The main advantage of the TEA5591A is its ability to operate over a wide range of supply voltages (1.8 to 15 V) without any loss of performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- A split-up IF amplifier
- A detector
- An AGC circuit which controls the IF amplifier and mixer.

The FM circuit incorporates:

- An RF input amplifier
- A double balanced mixer
- A 'one pin' oscillator
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- LED AM/FM indicator
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (1.8 to 15 V)
- All pins (except pin 10) are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 8)		V_P	1.8	–	15	V
Total current consumption						
AM part		I_P	–	14	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−15	–	+60	°C
AM performance (pin 1)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S + N)/N = 26 dB	V_i	–	17	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S + N)/N	–	48	–	dB
AF output voltage		V_o	–	45	–	mV
Total harmonic distortion		THD	–	0.7	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 2)	note 2					
Limiting sensitivity	−3 dB	V_i	–	2.3	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S + N)/N	–	26	–	dB
	V_i = 1 mV	(S + N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling		V_i	–	100	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.4) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

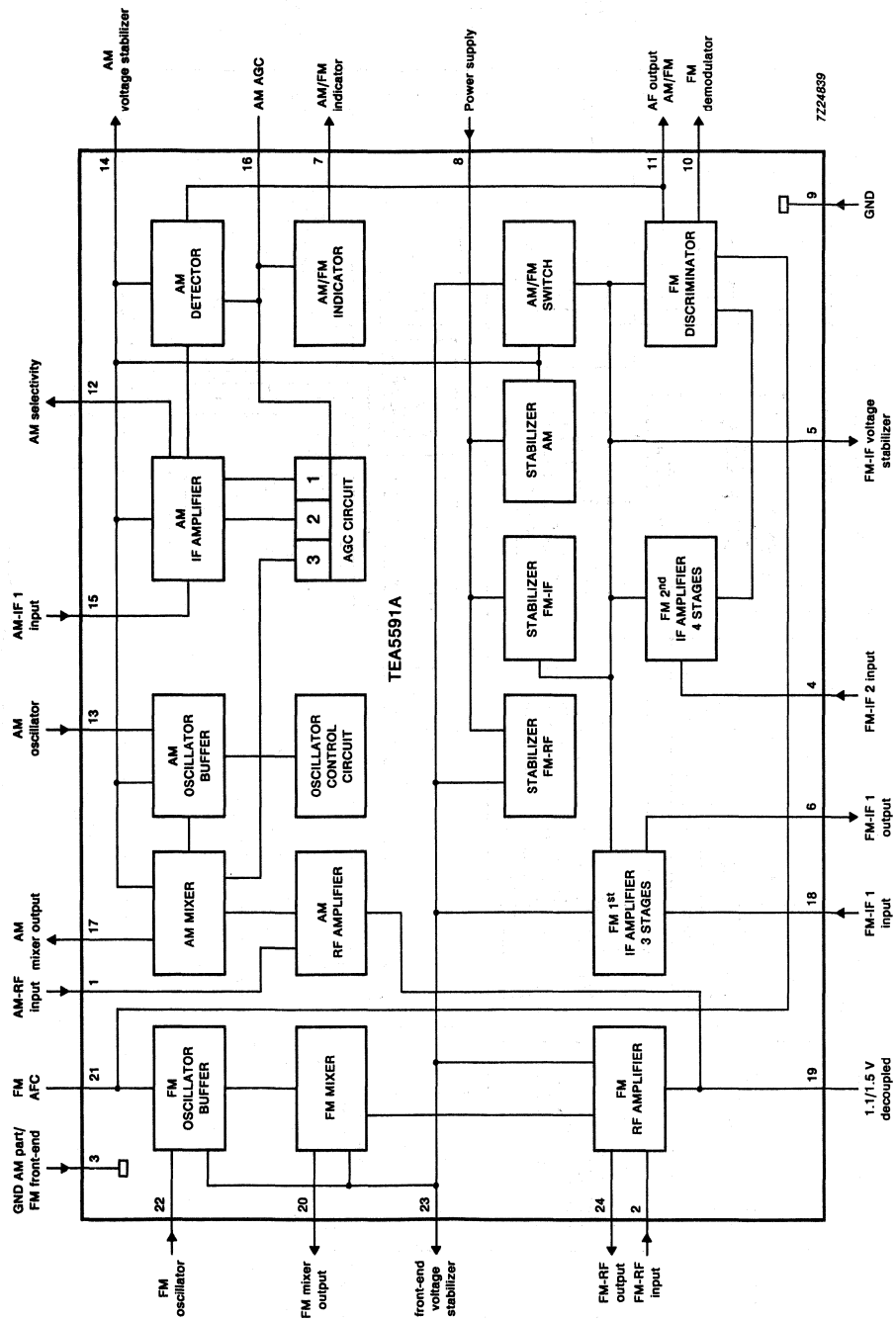


Fig.1 Block diagram.

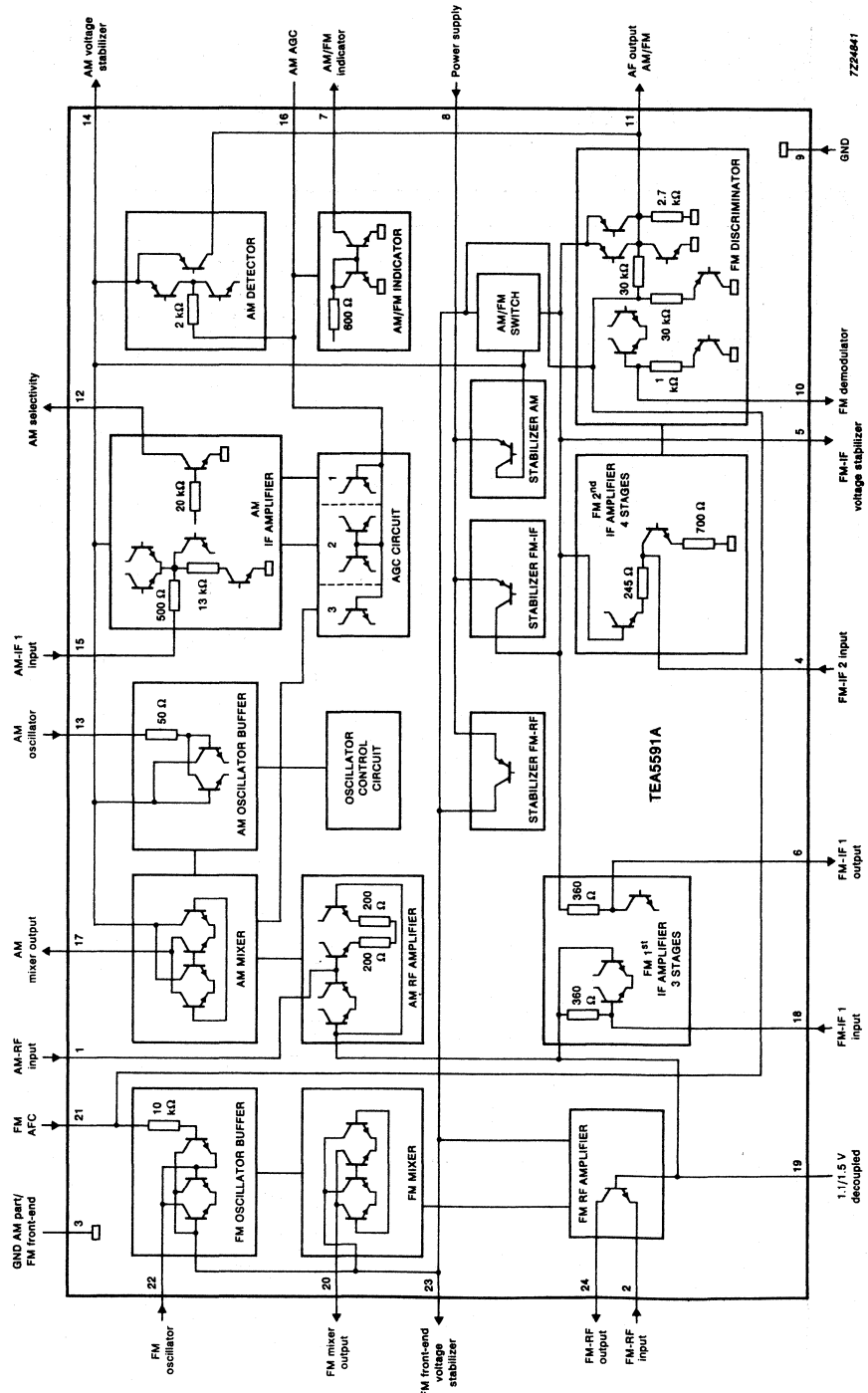


Fig.2 Equivalent circuit diagram.

PINNING

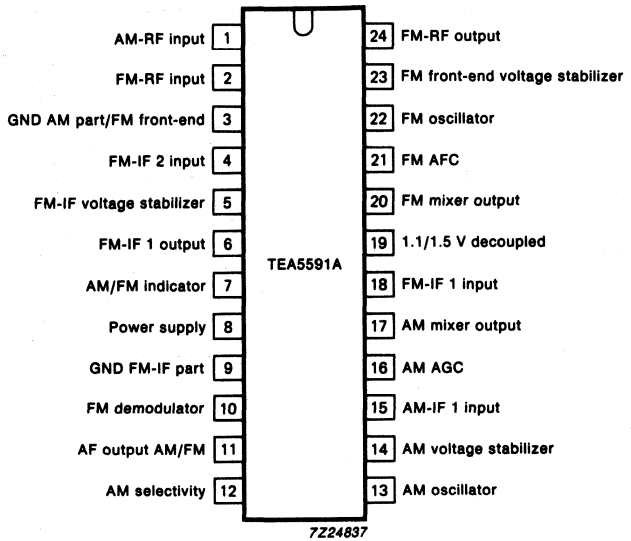


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 8)		V_P	–	18	V
LED current (pin 7)		I_7	–	*	mA
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−15	+60	°C
Electrostatic handling**		V_{es}	−1000	+1000	V

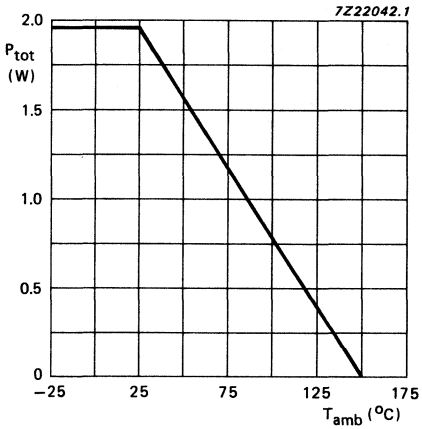


Fig.4 Power derating curve.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 3 and pin 9; all input currents are positive; all parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	1.8	3.0	15	V
Voltages (FM)						
pin 2		V_2	–	0.90	–	V
pin 4		V_4	–	0.85	–	V
pin 5		V_5	–	1.60	–	V
pin 6		V_6	–	1.48	–	V
pin 10		V_{10}	–	1.05	–	V
pin 18		V_{18}	–	1.60	–	V
pin 19		V_{19}	–	1.58	–	V
pin 21		V_{21}	–	0.69	–	V
pin 23		V_{23}	–	1.60	–	V
Voltages (AM)						
pin 14		V_{14}	–	1.60	–	V
pin 16		V_{16}	–	1.54	–	V
pin 19		V_{19}	–	1.10	–	V
Total current consumption	note 1					
AM part		I_P	–	14	19	mA
FM part		I_P	–	17	23	mA

Note to the DC characteristics

1. Without LED current.

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test set-up (see Fig.6) at nominal supply voltage V_P = 3 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM part						
AM front end (pin 1 to 17)	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 16) = V_{14} − 0.1 V	S_C	9.3	12	13.5	mA/V
	V_i = 10 mV V_{AGC} (pin 16) = V_{14} − 0.45 V	S_C	0.75	1.1	1.3	mA/V
IF suppression	note 2 V_i = 10 mV	α	20	26	–	dB
Oscillator (pin 13)						
Voltage	f = 1.5 MHz	V_{osc}	110	175	200	mV
	f = 1.5 MHz V_P = 1.5 V	V_{osc}	60	160	–	mV
IF and detector part (pin 15 to 11)	note 3					
IF sensitivity; AF output voltage	no AGC; V_i = 45 μV	V_o	12	20	55	mV
Signal + noise to noise ratio for an IF input	no AGC; V_i = 45 μV	S+N/N	23	25	–	dB
AF output voltage	V_i = 1 mV	V_o	35	45	60	mV
Total harmonic distortion	V_i = 10 mV m = 80%	THD	–	1	2.2	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	*	*	μA
	V_i = 1 mV	I_{ind}	*	*	–	mA
Overall performance (pin 1 to 11)	note 4					
Total harmonic distortion	V_i = * mV	THD	–	4.5	8	%

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
FM part						
FM front end (pin 2 to 20)	note 5					
Conversion transconductance	V_i = 1 mV	S_C	7.5	11	13.5	mA/V
Oscillator (pin 22)						
Voltage	V_{AFC} (pin 21) = 0.8 V	V_{osc}	155	200	245	mV
	V_{AFC} = 0.8 V V_P = 1.5 V	V_{osc}	60	120	–	mV
AFC control; change in oscillator frequency	V_{AFC} = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = –0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	–620	–	kHz
IF and demodulator part (pin 18 to 11)	note 6					
IF sensitivity; AF output voltage	note 7 V_i = 100 μV	V_o	–3	–1	0	dB
Signal + noise to noise ratio for an IF input	V_i = 100 μV; out of limiting	S+N/N	26	30	–	dB
AF output voltage	V_i = 1 mV	V_o	75	90	120	mV
Total harmonic distortion	Δf = 75 kHz V_i = 50 mV	THD	–	3	–	%
LED-indicator circuit (pin 7)						
Output current	V_i = 0 V	I_{ind}	–	–	20	μA
	V_i = 1 mV	I_{ind}	0.6	1	1.9	mA

Notes to the AC characteristics

1. Input frequency = 1 MHz; output frequency = 468 kHz.
2. $$\alpha = \frac{(V_o \text{ at } f_i = 1 \text{ MHz})}{(V_o \text{ at } f_i = 468 \text{ kHz})}$$
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

APPLICATION AND TEST INFORMATION

DEVELOPMENT DATA

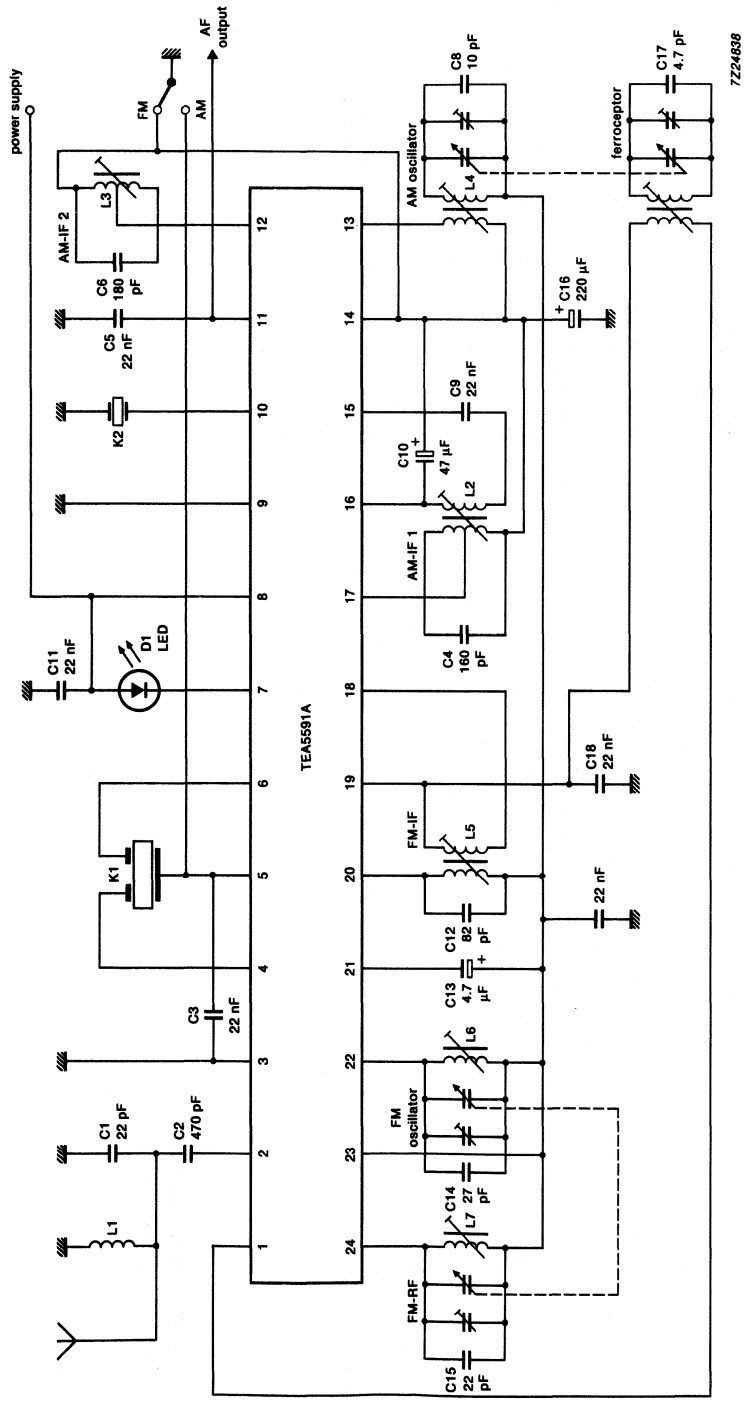


Fig.5 Application circuit.

APPLICATION AND TEST INFORMATION (continued)

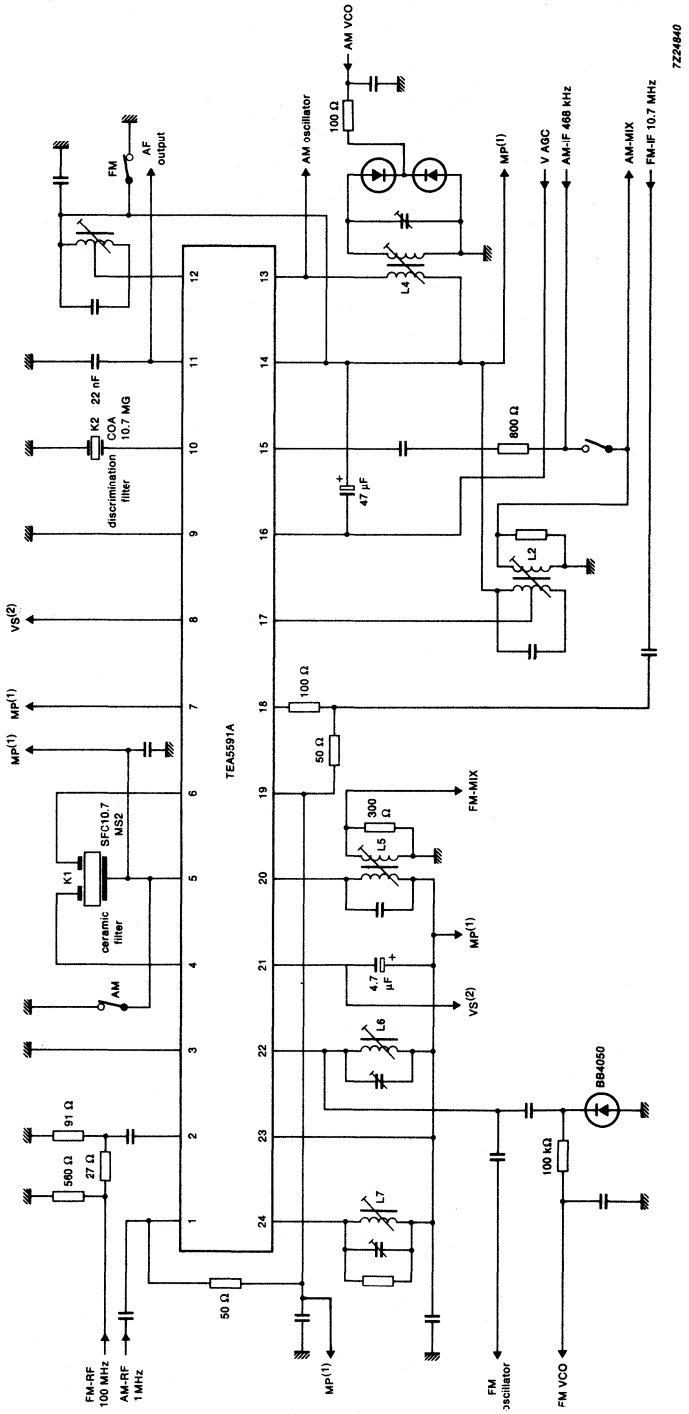


Fig.6 Test circuit.

(1) MP = measurement pin.
(2) VS = voltage source.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5592 is a 24-pin integrated radio circuit designed for use in all personal audio and car radio sets especially those sets with in- and out-door aerials that have to fulfill the FTZ (Amtsblatt) requirements.

The AM-IF and FM-IF stages are designed for the application of lumped selectivity. The main advantage of the TEA5592 is its ability to operate over a wide range of supply voltages (2.7 to 15 V) without any loss in performance.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the 0.6 to 30 MHz frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (designed for FTZ (Amtsblatt) radio sets)
- A 5-stage IF amplifier
- A quadrature demodulator for a ceramic filter
- Internal AFC

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Three separate stabilizers to enable operation over a wide range of supply voltages (2.7 to 15 V)
- All pins are ESD protected

PACKAGE OUTLINE

24-lead shrink DIL; plastic (SOT234).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	17	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+85	°C
AM performance (pin 13)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	1.5	–	μV
	(S+N)/N = 26 dB	V_i	–	15	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S+N)/N	–	48	–	dB
AF output voltage		V_o	–	55	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 22)	note 2					
Limiting sensitivity	−3 dB	V_i	–	1.8	–	μV
Signal-to-noise ratio	V_i = 2.5 μV	(S+N)/N	–	26	–	dB
	V_i = 1 mV	(S+N)/N	–	60	–	dB
AF output voltage		V_o	–	110	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	40	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig. 5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.

DEVELOPMENT DATA

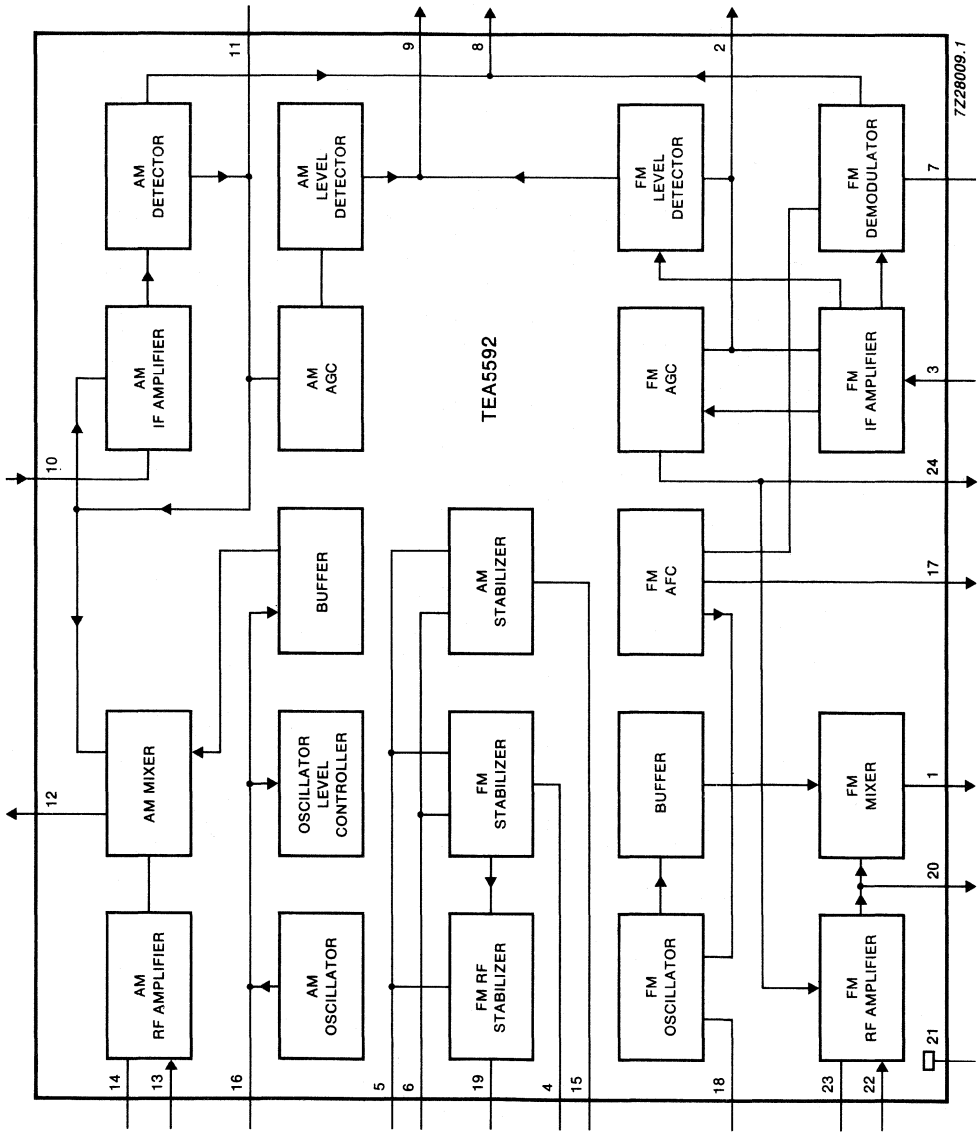


Fig.1 Block diagram.

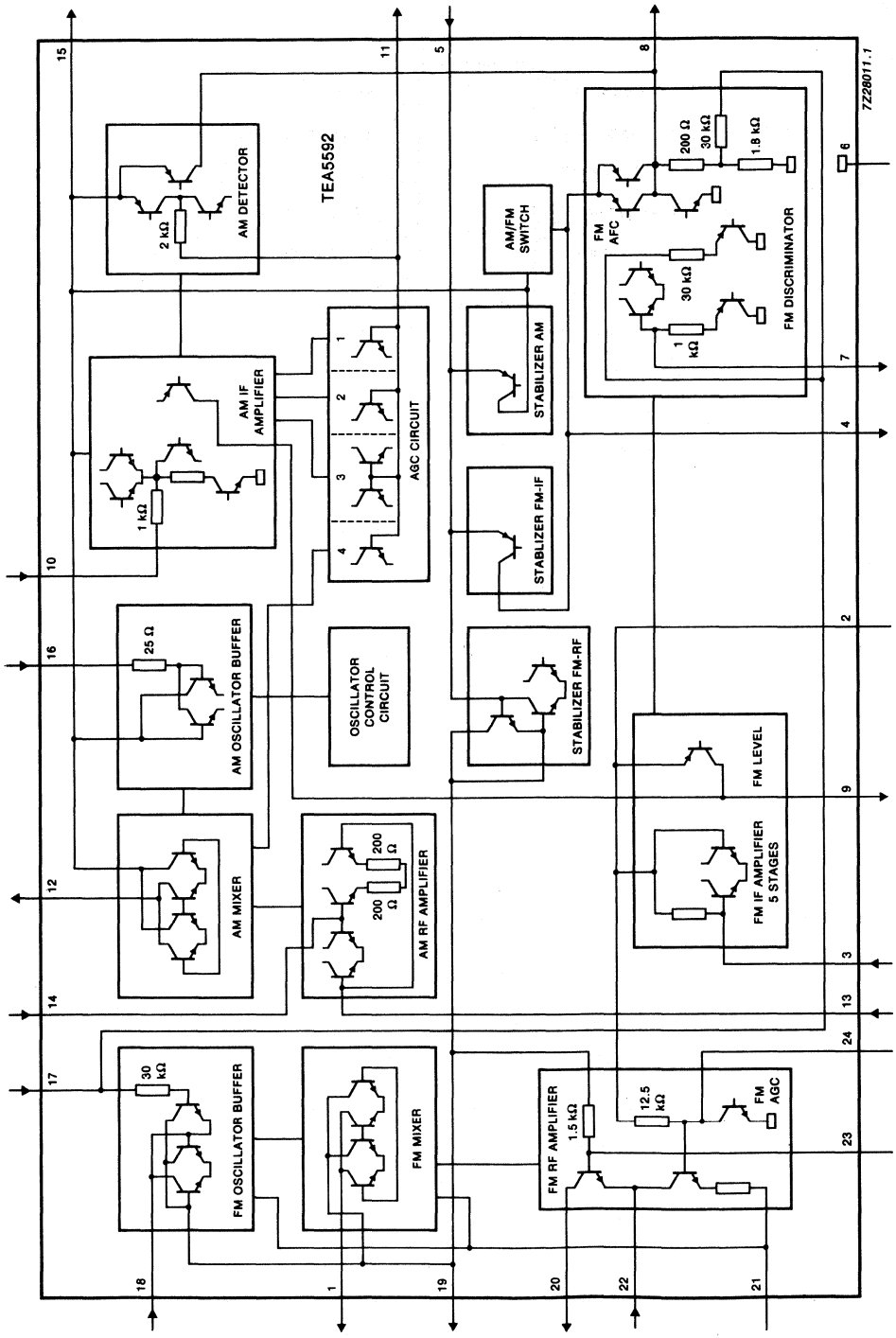


Fig.2 Equivalent circuit diagram.

PINNING

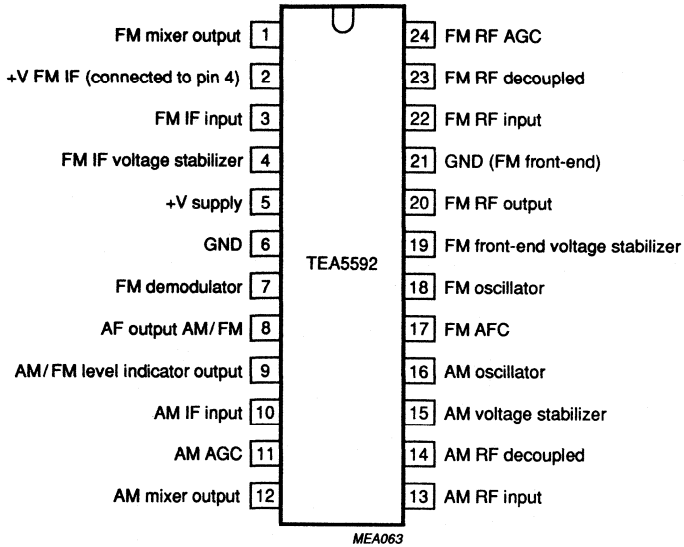


Fig.3 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 5)		V_P	–	15	V
Total power dissipation		P_{tot}	see Fig.3		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−40	+85	°C
Electrostatic handling *		V_{es}	−2000	+2000	V

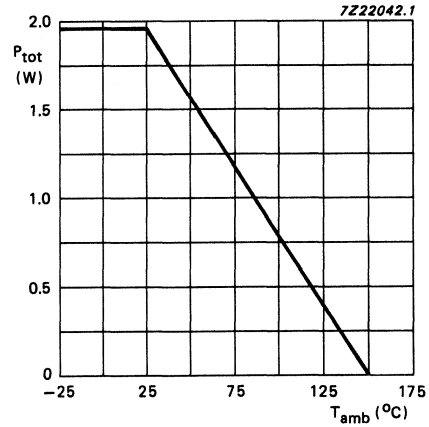


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages are referenced to pin 6 and pin 21; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 2		V_2	–	2.4	–	V
Pin 4		V_4	–	2.4	–	V
Pin 7		V_7	–	1.15	–	V
Pin 8		V_8	–	1.15	–	V
Pin 17		V_{17}	–	0.8	–	V
Pin 19		V_{19}	–	1.6	–	V
Pin 22		V_{22}	–	0.9	–	V
Pin 23		V_{23}	–	1.6	–	V
Pin 24		V_{24}	–	1.0	–	V
Voltages (AM)						
Pin 8		V_8	–	0.2	–	V
Pin 10		V_{10}	–	0.8	–	V
Pins 13 and 14		V_{13}, V_{14}	–	1.1	–	V
Pin 15		V_{15}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	19	mA
FM part		I_P	–	17	23	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.11) at nominal supply voltage Vp = 6 V; T_{amb} = 25 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
AM section						
AM front end (pin 13 to 12)	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 11) = V_{15} - 0.1 V	S_C	9.1	11.5	14	mA/V
	$V_{AGC} = V_{15}$ - 0.45 V	S_C	0.78	1.1	1.39	mA/V
IF suppression	note 2; V_o = 10 mV	α	20	30	–	dB
Oscillator (pin 16)						
Voltage	f = 1.5 MHz	V_{osc}	110	160	200	mV
	f = 1.5 MHz; V_P = 2.25 V	V_{osc}	60	–	–	mV
IF and detector section (pin 10 to 8)	note 3					
IF sensitivity;						
AF output voltage	no AGC; $V_{i(IF)}$ = 70 μV	V_o	27	40	55	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 70 μV	S+N/N	20	26	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	40	55	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	–	1	3	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	95	mV
	$V_{i(IF)}$ = 200 μV	V_9	–	200	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	450	600	mV
Overall performance (pin 13 to 8)	note 4					
Total harmonic distortion	V_i = 50 mV	THD	–	1.5	4	%

parameter	conditions	symbol	min.	typ.	max.	unit
FM section						
FM front end (pin 22 to 1)	note 5					
Conversion transconductance	V_i = 1 mV; V_{AGC} (pin 24) = 1.1 V	S_c	9	14	19	mA/V
	V_i = 1 mV; V_{AGC} (pin 24) = 0.8 V	S_c	4	8	10	mA/V
Oscillator (pin 18)						
Voltage	V_{AFC} = 0.8 V	V_{osc}	–	–	310	mV
	V_{AFC} = 0.8 V; V_P = 2.25 V	V_{osc}	95	200	–	mV
AFC control; change in oscillator frequency	V_{AFC} (pin 17) = 0.8 V	f	–	111.2	–	MHz
	ΔV_{AFC} = –0.6 V	Δf	–	+420	–	kHz
	ΔV_{AFC} = +0.6 V	Δf	–	–620	–	kHz
IF and demodulator section (pin 3 to 8)	note 6					
IF sensitivity;	note 7					
AF output voltage	$V_{i(IF)}$ = 70 μV	V_o	–3	–1	0	dB
Signal + noise-to-noise ratio for an IF input	$V_{i(IF)}$ = 70 μV no limiting	S+N/N	20	30	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	80	110	130	mV
Total harmonic distortion	Δf = 75 kHz; $V_{i(IF)}$ = 50 mV	THD	–	1	–	%
Indicator/level detector (pin 9)						
Output voltage	$V_{i(IF)}$ = 0 V	V_9	–	–	20	mV
	$V_{i(IF)}$ = 500 μV	V_9	–	260	–	mV
	$V_{i(IF)}$ = 10 mV	V_9	–	550	670	mV

DEVELOPMENT DATA

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz.
2. α = 20 log (V_i at f_i = 468 kHz) / (V_i at f_i = 1 MHz).
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
4. Front-end connected to IF plus detector part. Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz.
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at V_i = 1 mV.

DEVELOPMENT DATA

APPLICATION AND TEST INFORMATION

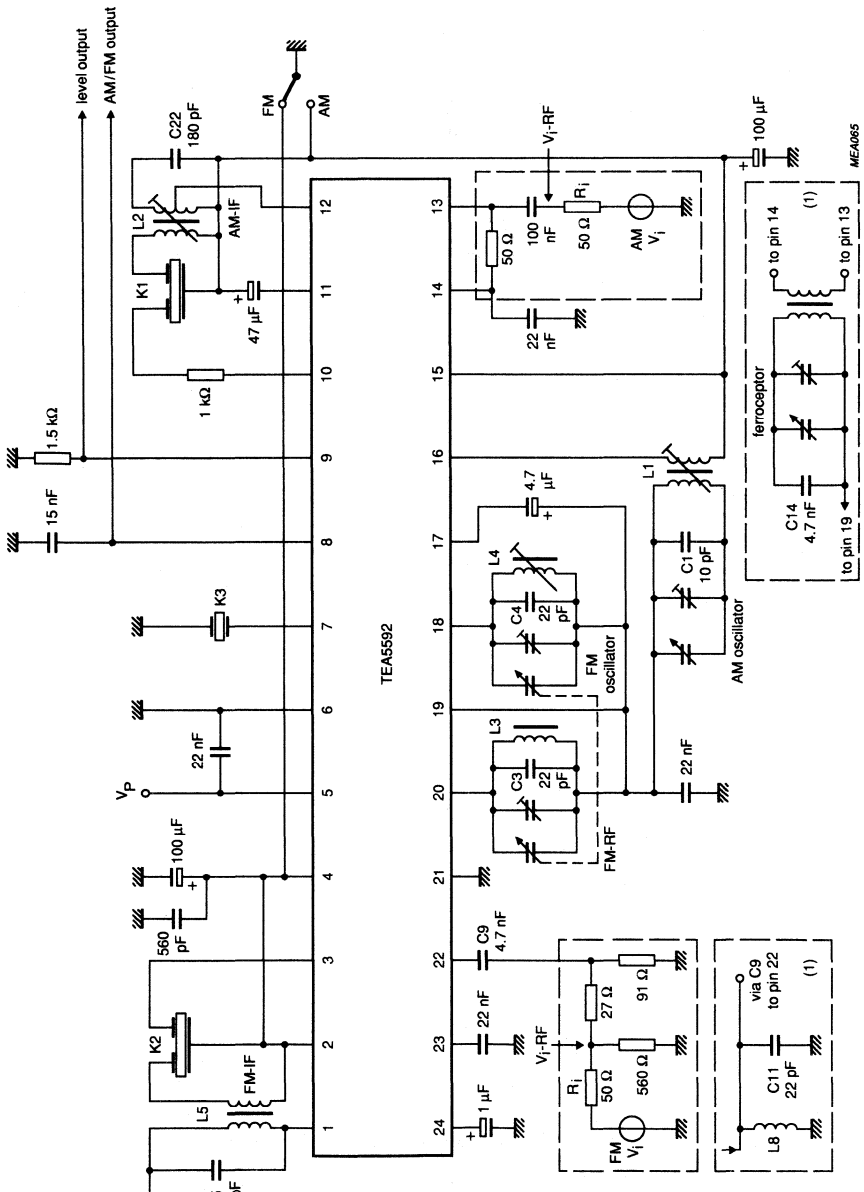


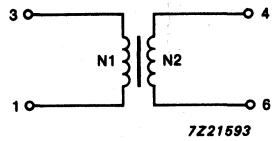
Fig. 5 Application circuit.

(1) In application the input circuits can be replaced by ferroceptor and aerial input circuit.

APPLICATION AND TEST INFORMATION (continued)

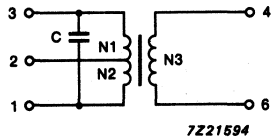
Component data

COILS



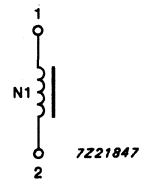
N1 = 86
N2 = 11
Lprim = 270 μH
Wire = 0.07 mm diameter
Coil type TOKO 7BRS

Fig.6 AM oscillator coil (L1).



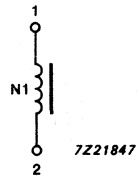
N1 = 135
N2 = 13
N3 = 5
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MCS

Fig.7 AM-IF coil (L2).



N1 = 2.5
L = 0.066 μH

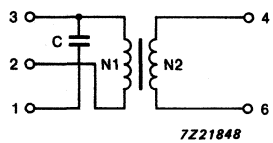
Fig.8 FM-RF coil (L3). TOKO equivalent no. 301SN-0200.



N1 = 1.5
L = 0.04 μH

Fig.9 FM oscillator coil (L4). TOKO equivalent no 301SN-0100.

DEVELOPMENT DATA



N1 = 11
N2 = 2
C = 82 pF (internal)
f_o = 10.7 MHz

Fig.10 FM-IF coil (L5). TOKO equivalent no. 301-20N

CERAMIC FILTERS

AM-IF (K1). SFU468B.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1.

TUNING CAPACITORS

AM section – 140/82 pF
FM section – 2 x 20 pF

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

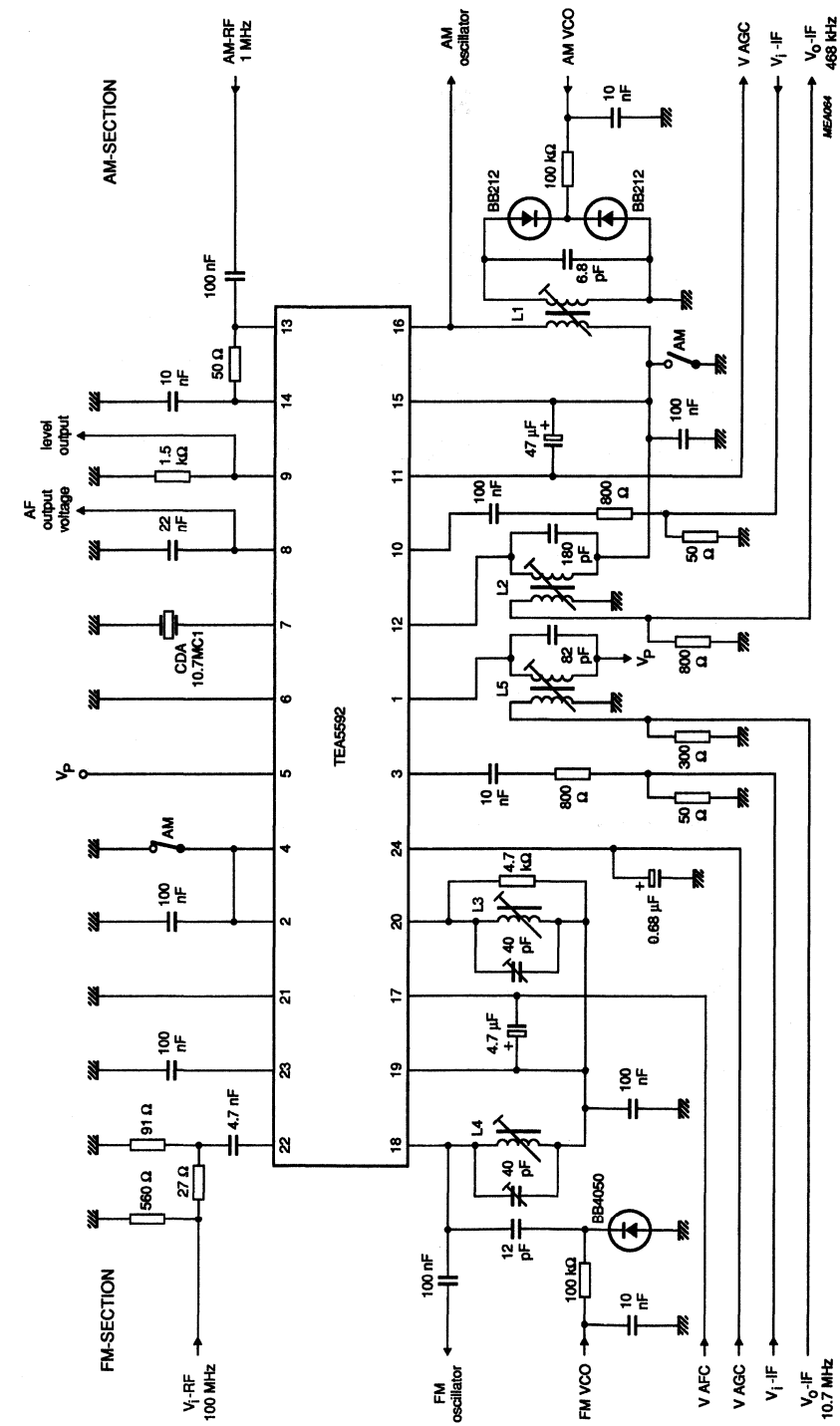


Fig.11 Factory test circuit.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5594 is a 32-pin integrated radio circuit designed for use in all Electronic Tuned Radio (ETR) sets especially those sets which have to fulfil the immunity requirements of CENELEC.

The AM circuit incorporates:

- A double balanced mixer
- A 'one-pin' oscillator with amplitude control operating in the LW/MW frequency range
- An IF amplifier and AM detector
- An AGC circuit which controls the IF amplifier and mixer

The FM circuit incorporates:

- A front-end (fulfilling the "out of band" CENELEC requirements)
- Two IF amplifiers (for distributed selectivity)
- A quadrature demodulator with a ceramic filter

The TEA5594 also contains:

- Oscillator output buffers for AM and FM
- A combined AM/FM IF counter output buffer with counter "enable" function
- A field strength level detector for AM and FM
- A soft mute circuit at FM, adjustable
- An extra IF amplifier to split up IF filtering

Features

- Low distortion on FM
- AM/FM level/indicator circuit
- A DC AM/FM switch facility
- Supply voltages 2.7 to 15 V
- A local distance switch facility (LOCAL-DX) at FM
- All pins are ESD protected

PACKAGE OUTLINE

32-lead shrink DIL; plastic (SOT232).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 9)		V_P	2.7	–	15	V
Total current consumption						
AM part		I_P	–	13	–	mA
FM part		I_P	–	24	–	mA
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C
AM performance (pin 22)	note 1					
Sensitivity	V_o = 10 mV	V_i	–	3.5	–	μV
	(S + N)/N = 26 dB	V_i	–	16	–	μV
Signal-to-noise ratio	V_i = 1 mV	(S + N)/N	–	48	–	dB
AF output voltage		V_o	–	50	–	mV
Total harmonic distortion		THD	–	0.8	–	%
Signal handling	m = 80%; THD = 8%	V_i	–	100	–	mV
FM performance (pin 30)	note 2					
Limiting sensitivity	−3 dB; note 3	V_i	–	2.5	–	μV
Signal-to-noise ratio	V_i = 3 μV	(S + N)/N	–	26	–	dB
	V_i = 1 mV	(S + N)/N	–	60	–	dB
AF output voltage		V_o	–	90	–	mV
Total harmonic distortion		THD	–	0.1	–	%
Maximum signal handling		V_i	–	200	–	mV
AM suppression	100 μV < V_i < 100 mV	AMS	–	50	–	dB

Notes to the quick reference data

1. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 1 MHz; 30% modulated with f_{mod} = 1 kHz; unless otherwise specified.
2. All parameters are measured in the application circuit (see Fig.5) at nominal supply voltage V_p = 8.5 V; T_{amb} = 25 °C; unless otherwise specified. RF conditions: Input frequency 100 MHz; frequency deviation Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
3. Soft mute switched off.

DEVELOPMENT DATA

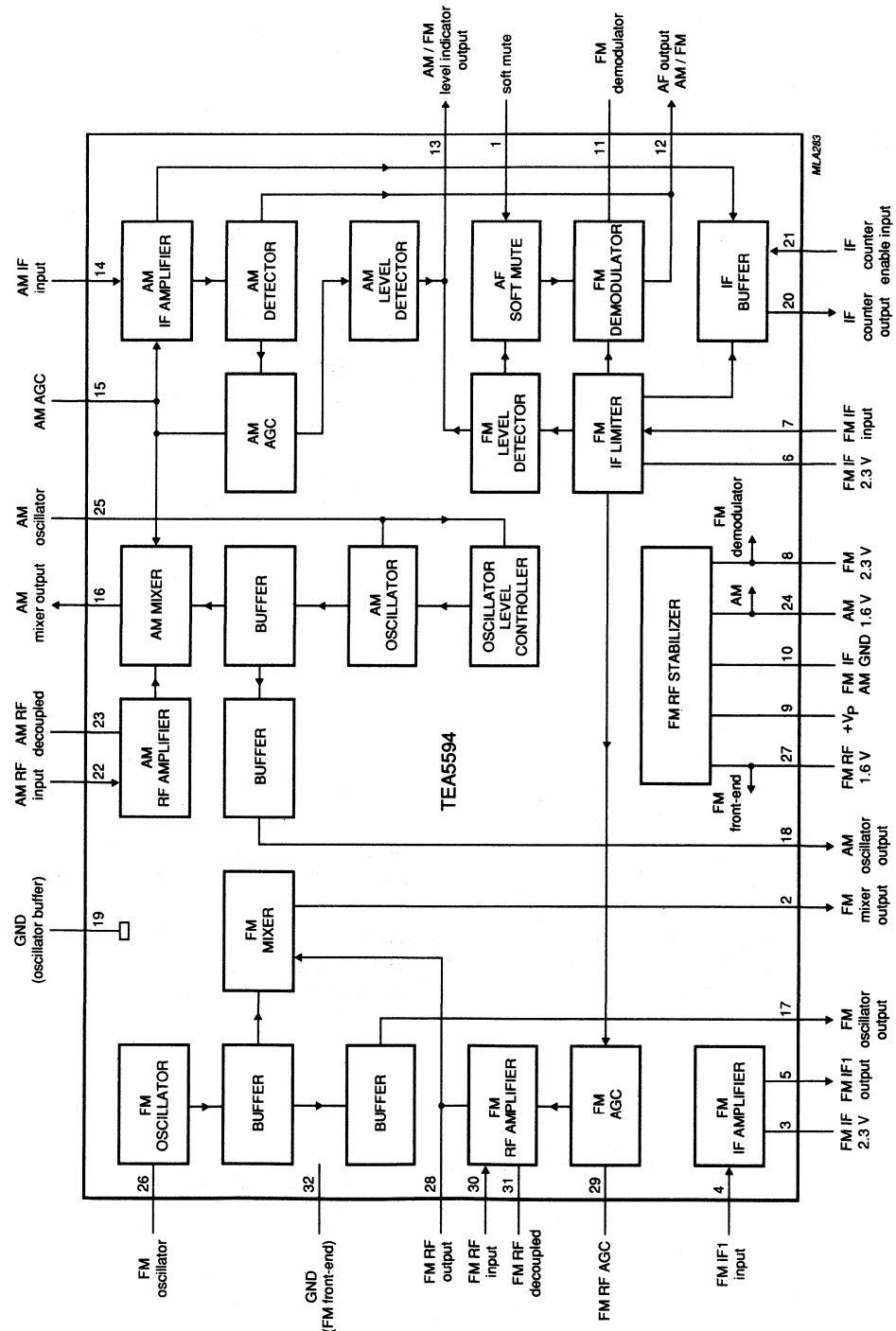


Fig.1 Block diagram.

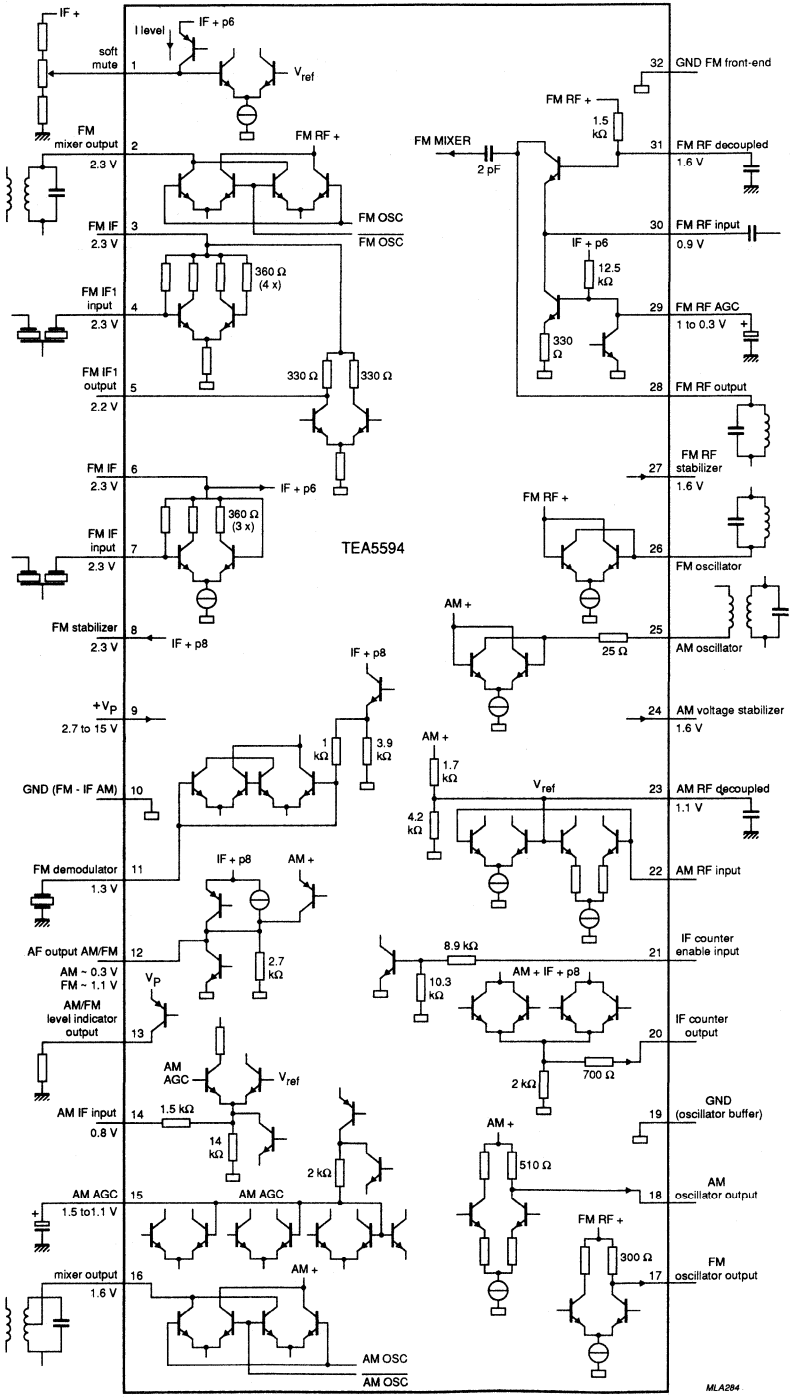


Fig.2 Equivalent circuit diagram.

DEVELOPMENT DATA

PINNING

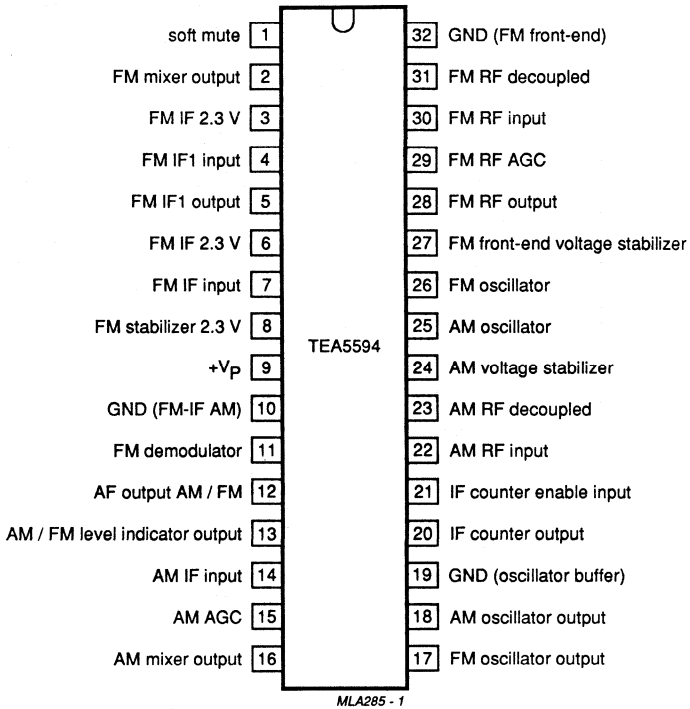


Fig.3 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 9)		V_P	–	18	V
Total power dissipation		P_{tot}	see Fig.4		
Storage temperature range		T_{stg}	−65	+ 150	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Electrostatic handling*		V_{es}	−2000	+ 2000	V

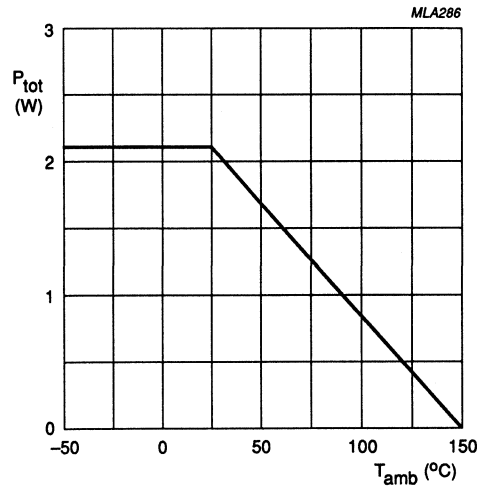


Fig.4 Power derating curve.

* Equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor.

DEVELOPMENT DATA

DC CHARACTERISTICS

All voltages are referenced to pin 10, pin 19 and pin 32; all input currents are positive; all parameters are measured in application circuit (see Fig.5) at nominal supply voltage V_P = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	2.7	8.5	15	V
Voltages (FM)						
Pin 4		V_4	–	2.3	–	V
Pin 5		V_5	–	2.2	–	V
Pin 7		V_7	–	2.3	–	V
Pin 8		V_8	–	2.3	–	V
Pin 12		V_{12}	–	1.15	–	V
Pin 27		V_{27}	–	1.6	–	V
Pin 29		V_{29}	–	1.0	–	V
Pin 30		V_{30}	–	0.9	–	V
Pin 31		V_{31}	–	1.6	–	V
Voltages (AM)						
Pin 12		V_{12}	–	0.2	–	V
Pin 14		V_{14}	–	0.8	–	V
Pin 15		V_{15}	–	1.54	–	V
Pins 22 and 23		V_{22}, V_{23}	–	1.1	–	V
Pin 24		V_{24}	–	1.6	–	V
Total current consumption						
AM part		I_P	–	13	*	mA
FM part		I_P	–	24	*	mA

* Value to be fixed.

AC CHARACTERISTICS

All parameters are measured in test circuit (see Fig.6) at nominal supply voltage V_P = 6 V; T_{amb} = 25 °C unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
AM SECTION						
AM front end	note 1					
Conversion transconductance	V_i = 10 mV V_{AGC} (pin 15) = V_{24} - 0.1 V	S_C	*	13.5	*	mA/V
	V_{AGC} = V_{24} - 0.45 V	S_C	*	1.2	*	mA/V
IF suppression	note 2	α	20	30	–	dB
Oscillator (pin 25)						
Voltage	f = 1.5 MHz	V_{osc}	–	160	*	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{18}	*	140	–	mV
IF and detector part	note 3					
IF sensitivity; AF output voltage	no AGC; $V_{i(IF)}$ = 90 μV	V_o	30	40	60	mV
Signal + noise to noise ratio for an IF input	no AGC; $V_{i(IF)}$ = 90 μV	S+N/N	22	24	30	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	35	50	70	mV
Total harmonic distortion	$V_{i(IF)}$ = 10 mV; m = 80%	THD	0.75	2	5	%
	$V_{i(IF)}$ = * to * mV; m = 30%	THD	–	*	–	%
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	560	*	mV
	$V_{i(IF)}$ = 200 μV	V_{13}	*	3200	*	mV
	$V_{i(IF)}$ = 10 mV	V_{13}	*	6600	*	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
AM IF counter output buffer						
Counter "enable"						
Output voltage (peak-to-peak value)		V_{20}	100	125	–	mV
Counter "disable"						
Suppression of 468 kHz		V_{20}	–40	–	–	dB
Overall performance	note 4					
Total harmonic distortion	$V_{i(RF)}$ = 50 mV	THD	–	–	8	%
Signal handling	THD = * %; m = 0.8%		–	*	–	
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
FM SECTION						
FM front end	note 5					
Conversion transconductance	$V_{i(RF)}$ = 1 mV; V_{AGC} = 1.1 V	S_c	16	24	32	mA/V
	$V_{i(RF)}$ = 1 mV; V_{AGC} = 0.8 V	S_c	5	10	15	mA/V
Oscillator (pin 26)						
Voltage		V_{osc}	–	250	–	mV
Oscillator buffer						
Output voltage (peak-to-peak value)		V_{17}	*	270	–	mV
IF and demodulator part	note 6					
IF sensitivity	note 7					
AF output voltage	$V_{i(IF)}$ = 40 μV no mute	V_o	–3	–1	0	dB
	with mute	V_o	–20	–30	–40	dB
AM suppression	note 8	α	–	*	–	dB
Signal + noise-to-noise ratio for an IF input	no mute; $V_{i(IF)}$ = 40 μV	S+N/N	28	46	50	dB
	$V_{i(IF)}$ = 1 mV	S+N/N	–	*	–	dB
AF output voltage	$V_{i(IF)}$ = 1 mV	V_o	*	85	*	mV
Total harmonic distortion	$V_{i(IF)}$ = 50 mV; Δf = 75 kHz	THD	–	1	–	%
	Δf = 22.5 kHz	THD	–	*	–	%

* Value to be fixed.

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator/level detector						
Output voltage	$V_{i(IF)}$ = 0 V	V_{13}	*	2600	*	mV
	$V_{i(IF)}$ = 50 μV	V_{13}	*	5750	*	mV
	$V_{i(IF)}$ = 1 mV	V_{13}	*	6250	*	mV
AM/FM IF counter output buffer						
Counter "enable"	note 5					
Output voltage (peak-to-peak value)		V_{20}	–	130	–	mV
Counter "disable"						
Suppression of 10.7 MHz		V_{20}	–40	–	–	dB
Counter enable circuit						
IF counter output OFF		V_{21}	–	–	0.8	V
IF counter output ON		V_{21}	2	–	V_P	V
AM/FM switch						
FM OFF/AM ON		$V_{8\text{-}10}$	–	0	0	V
FM ON/AM OFF		$V_{24\text{-}10}$	–	0	0	V

Notes to the AC characteristics

1. Input frequency = 1 MHz, output frequency = 468 kHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N2/N3}{R}$ (see TR2 Component data)
   Where R = 1.2 kΩ (total impedance at pin 16).
2. α = 20 log (V_i at f_i = 468 kHz)/(V_i at f_i = 1 MHz); V_o = 10 mV; no AGC.
3. Input frequency = 468 kHz; m = 30% modulated with f_{mod} = 1 kHz; R_{source} = 800 Ω unless otherwise specified.
4. Front-end connected to IF plus detector part (see Fig.5). Input frequency = 1 MHz; m = 80% modulated with f_{mod} = 1 kHz.
5. Input frequency = 100 MHz; output frequency = 10.7 MHz;
   $S_c = \frac{V_{o(IF)}}{V_{i(RF)}} \times \frac{N1/N2}{R}$ (see TR3 Component data)
   Where R = 6.6 kΩ (total impedance at pin 2).
6. Input frequency = 10.7 MHz; frequency deviation, Δf = 22.5 kHz and f_{mod} = 1 kHz; unless otherwise specified.
7. Reference: AF output voltage = 0 dB at $V_{i(IF)}$ = 1 mV;
   No mute : $V_1 = V_8$;
   With mute : V_1 = 0 V.
8. AM suppression is measured with AM only: m = 0.8% and f_{mod} = 1 kHz referred to AF output at FM only: Δf = 75 kHz and f_{mod} = 1 kHz.

* Value to be fixed.

APPLICATION AND TEST INFORMATION

For coil information see Component data.

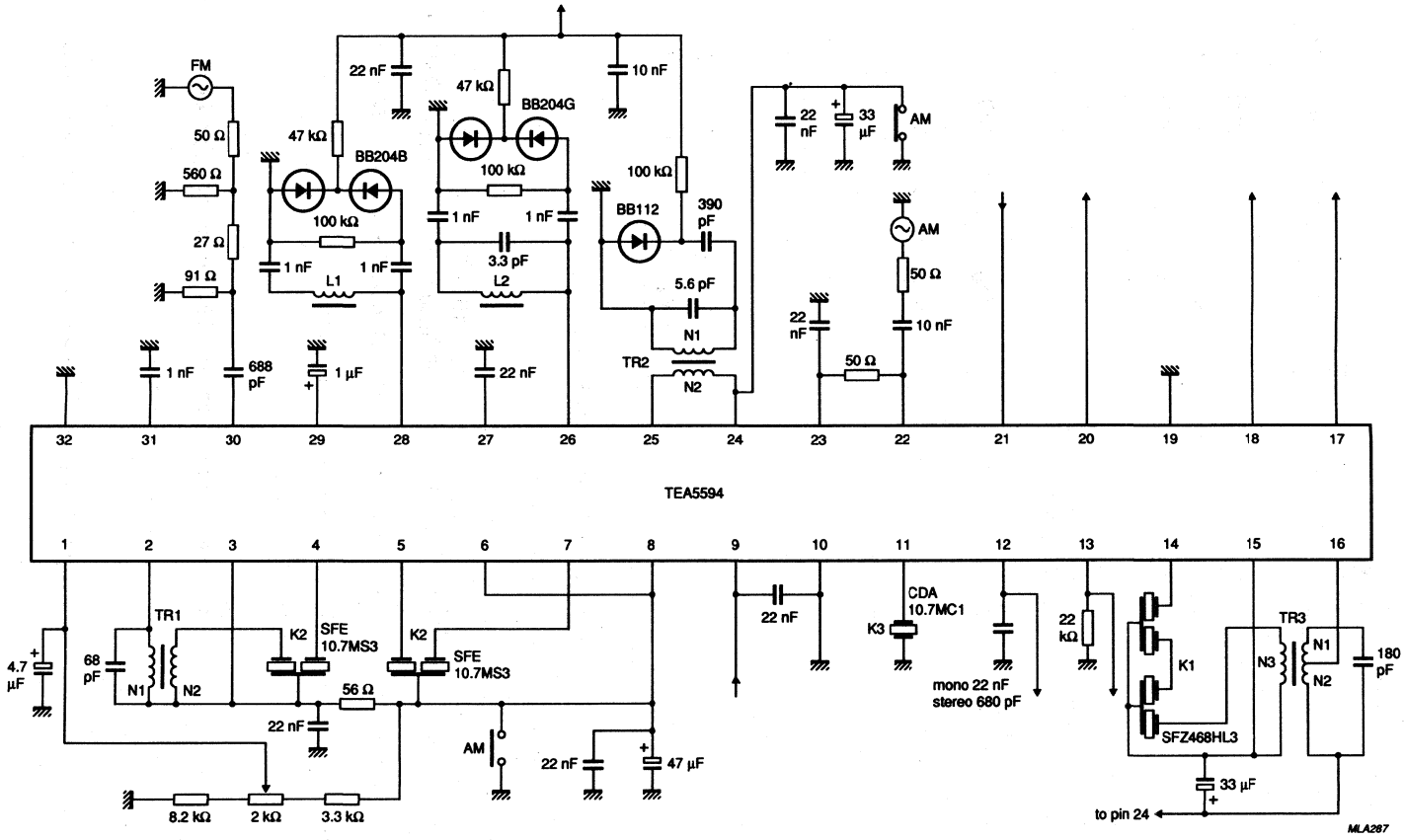


Fig.5 Application circuit for evaluation.

APPLICATION AND TEST INFORMATION (continued)

For coil information see Component data.

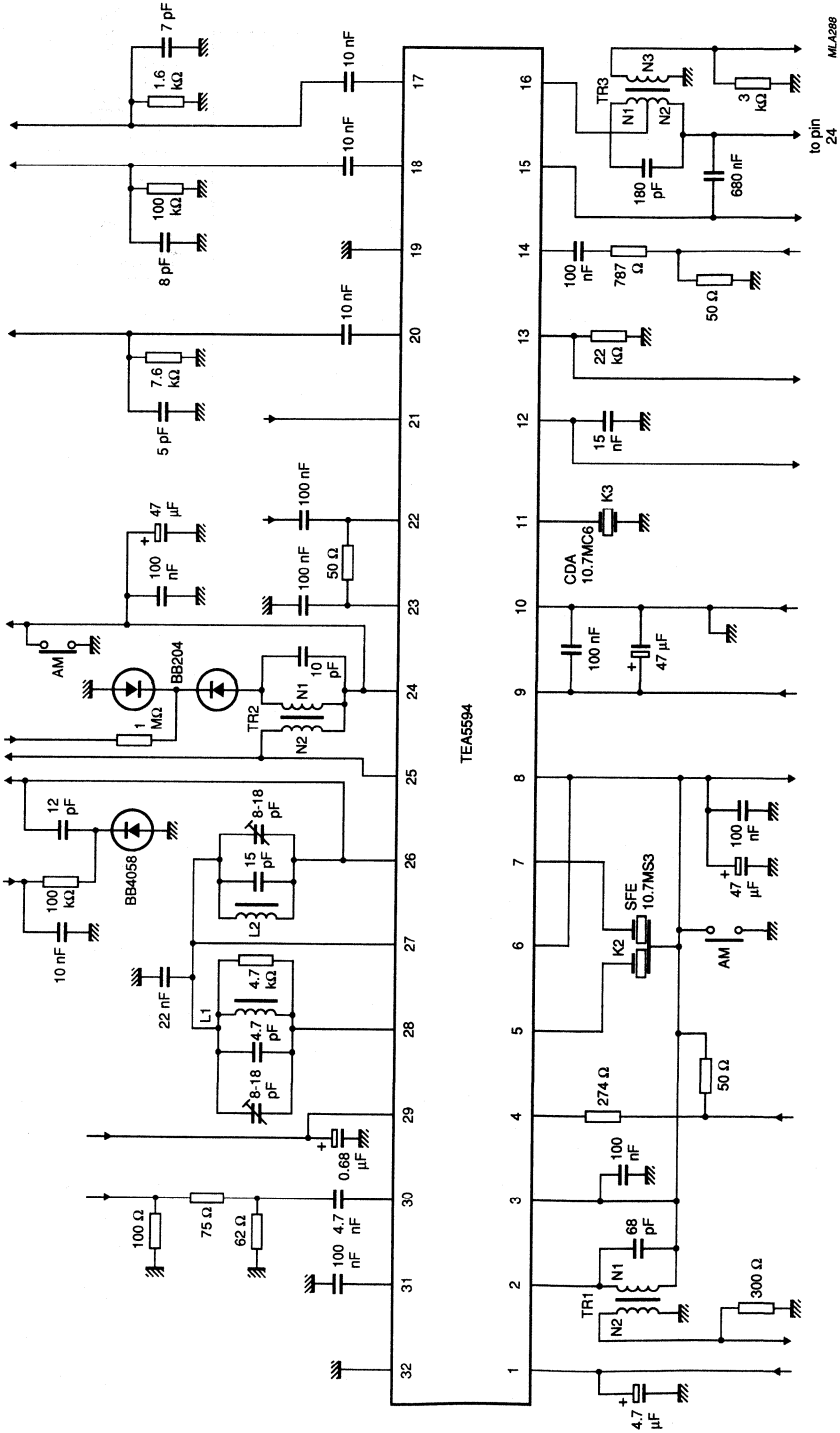
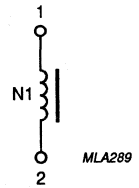


Fig.6 Factory test circuit.

Component data

COILS

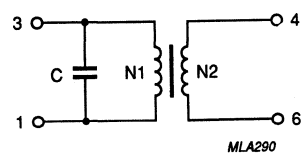


N1 = 4.5
L = 100 μH

Fig.7 FM-RF coil (L1). TOKO equivalent no. MC115.

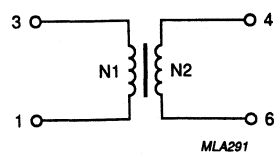
N1 = 4.5
L = 94 μH

Fig.8 FM oscillator coil (L2). TOKO equivalent no. A294SNS-1004NK.



N1 = 12
N2 = 2
C = 68 pF (internal)
f_o = 10.7 MHz
Wire = 0.07 mm diameter
Coil type TOKO 119BCS-A6515BQG

Fig.9 FM-IF coil (TR1).

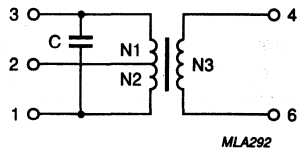


N1 = 55
N2 = 55
Lprim = 106 μH
Wire = 0.05 mm diameter
Coil type TOKO 7MCS

Fig.10 AM oscillator coil (TR2).

Component data (continued)

COILS



N1 = 139
N2 = 15
N3 = 9
C = 180 pF (internal)
Lprim = 660 μH
f_o = 468 kHz
Wire = 0.07 mm diameter
Coil type TOKO 7MC

Fig.11 AM-IF coil (TR3).

CERAMIC FILTERS

AM-IF (K1). SFZ468HL3.
FM-IF (K2). SFE10.7MS3.
FM detector (K3). CDA10.7MC1 (MC6).

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6100 is a FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes highly sensitive analogue circuitry. The digital circuitry, including an I^2C bus, controls the analogue circuitry and the AM/FM tuning and stop information for the microcomputer.

Features

- 4-stage symmetrical IF limiting amplifier
- Software selectable AM or FM input
- Symmetrical quadrature demodulator
- Single-ended LF output stage
- D.C. output level determined by the input signal
- Semi-adjustable AM and FM level voltage
- Multi-path detector/rectifier/amplifier circuitry
- 3-bit level information and 3-bit multi-path information
- Signal dependent 'soft' muting circuit; externally adjustable
- Reference voltage output (FM mode only)
- 8-bit AM/FM frequency counter with selectable counter resolution
- Possibility to measure the AM IF frequency at 460 kHz (250 Hz resolution) and 10,7 MHz (500 Hz resolution)
- Reference frequency can be directly connected to the reference frequency output of a frequency synthesizer (TSA6057, 40 kHz)

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{P1}, V_{P2}	–	8,5	–	V
Supply current		$I_{P1} + I_{P2}$	–	35	–	mA
FM/IF sensitivity	–3 dB before limiting	V_i	–	15	–	μV
Signal plus noise to noise ratio	Δf = 75 kHz; V_I = 10 mV	(S + N)/N	–	85	–	dB
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	–	200	–	mV
AM suppression	V_{IFM} = 600 μV to 600 mV; m = 0,3	AMS	–	60	–	dB
Frequency counter sensitivity						
AM	pin 19, f = 10,7 MHz	$V_{i(AM)}$	–	45	–	μV
	f = 460 kHz	$V_{i(AM)}$	–	20	–	μV
FM	pin 18, f = 10,7 MHz	$V_{i(FM)}$	–	45	–	μV
Resolution of the frequency counter	reference frequency of 40 kHz;					
AM	IF = 460 kHz	f_s (AM)	–	250	–	Hz
	IF = 10,7 MHz	f_s (AM)	–	500	–	Hz
FM		f_s (FM)	–	6,4	–	kHz

DEVELOPMENT DATA

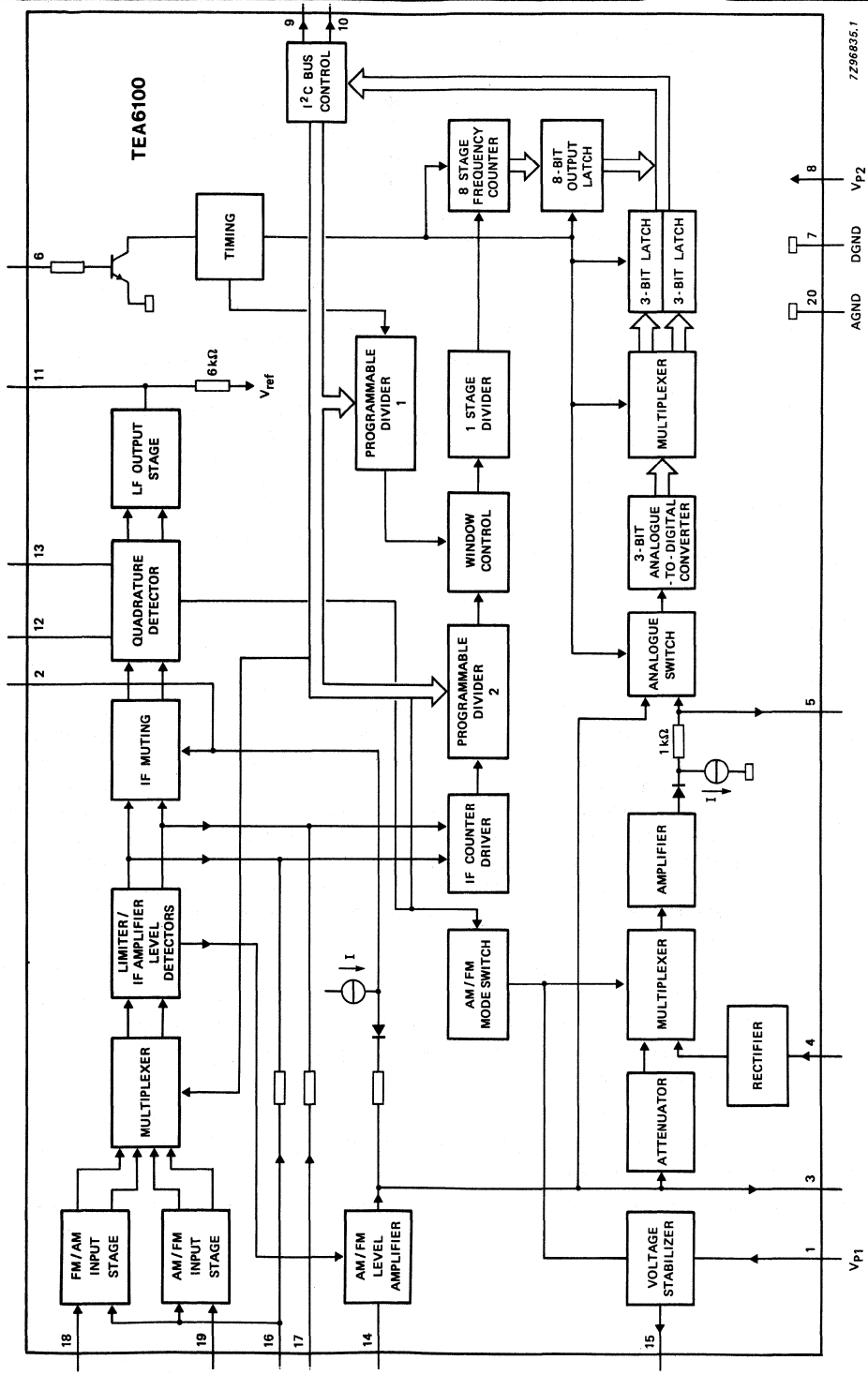


Fig. 1 Block diagram.

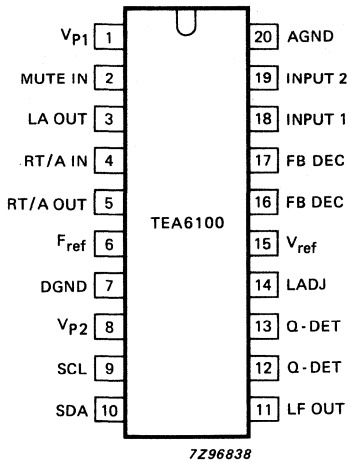


Fig. 2 Pinning diagram.

PINNING

1	V_{P1}	analogue supply voltage
2	MUTE IN	mute input
3	LA OUT	level amplifier output
4	RT/A IN	rectifier/amplifier input
5	RT/A OUT	rectifier/amplifier output
6	F_{ref}	reference frequency input
7	DGND	digital ground
8	V_{P2}	digital supply voltage
9	SCL	serial clock line) I^2C bus
10	SDA	serial data line) I^2C bus
11	LF OUT	audio output signal
12	Q-DET	phase shift for quadrature detector
13	Q-DET	phase shift for quadrature detector
14	LADJ	level amplifier adjustment
15	V_{ref}	reference voltage
16	FB DEC	decoupled feedback
17	FB DEC	decoupled feedback
18	INPUT 1	FM/AM IF input
19	INPUT 2	AM/FM IF input
20	AGND	analogue ground

FUNCTIONAL DESCRIPTION (see Figs 1 and 13)

The IF amplifier consists of four balanced limiting amplifier stages, two separate inputs (AM and FM) and one output. Software programming (see Table 2; Figs 4 and 5) allows the input signals (AM/FM) to be inserted on either input (pin 18 or 19). The output drives the frequency counter and via the mute stage, drives the quadrature detector. The output of the quadrature detector is applied to an audio stage (which has a single-ended output). The AM/FM level amplifier, which is driven by 5 IF level detectors, generates a signal dependent d.c. voltage. The level output voltage is used internally to control the mute stage and, if required, the signal can be used externally to control the stereo channel separation and frequency response of a stereo decoder. The signal is also feed to the analogue-to-digital converter (ADC). Due to the front-end spread in the amplification, the level voltage is made adjustable (LADJ, pin 14). The level voltage amplifier controls the mute stage and this insures the −3 dB limiting point remains constant, independent of the front-end spread. AM and FM mode have different front-end circuitry, therefore LADJ must be adjustable for both inputs.

The output voltage of the level amplifier is dependent upon the field strength of the input signal. The multi-path of the FM signal exists in the AM modulation of the input signal. The following method is used to determine the level information and the amount of multi-path (as a DC voltage):

- the IF level detector detects the multi-path and feds the signal, via the level amplifiers, to the external bandpass filter (pin 3) and ADC1
- the signal is then fed to an internal rectifier
- the rectified signal is then fed to an amplifier, so at pin 5 the DC level information is externally available and internally used by ADC2

In the FM mode, the DC information concerning the multi-path is available at pin 5 and the level information is available at pin 3.

In the AM mode, the level information at pin 3 cannot be directly used owing to AM modulation on the output signal of the level amplifier. This signal requires filtering, which is achieved by the following method:

- the multiplexer is switched to a position which causes the signal to be applied to the attenuator
- after attenuation the signal is fed to an amplifier (the resultant gain of attenuator and amplifier is unity), after amplification the signal is filtered by an internal resistor and external capacitor
- after filtering the signal is applied to ADC2 and is externally available

In AM mode pin 5 contains the level information.

The voltages on pin 3 and 5 are converted into two 3-bit digital words by the ADC, which can then be read out by the I^2C bus. The meaning of the 3-bit words is shown in Table 1.

Table 1 3-bit words

	position	
word	FM	AM
1	multipath	level without modulation
2	level	level with modulation

The FM modulated signal is converted into an audio signal by the symmetrical quadrature detector. The main advantage of such a detector is that it requires few external components.

An FM signal requires good AM suppression, and as a result, the IF amplifiers must act as limiters. To achieve good suppression on small input signals the IF amplifiers must have a high gain and thus a high sensitivity. High sensitivity is an undesirable property when used in car radio applications, this problem is solved by having an externally adjustable mute stage to control the overall sensitivity of the device.

The IF mute stage is controlled by the level amplifier (soft muting) and is only active in FM mode. If the input falls below a predetermined level, the mute stage becomes active. To avoid the 'ON/OFF' effect of the audio signal due to fluctuations of the input signal, the mute stage is activated rapidly but de-activated slowly. The mute stage is de-activated slowly, via a current source and an external capacitor at pin 2, to avoid aggressive behaviour of the audio signal. It is possible to adjust the '−3 dB limiting point' of the audio output via the level voltage due to the level signal being externally adjustable. If hard muting is required then pin 2 must be switched to ground.

The 8-bit counter allows accurate stop information to be obtained, because exact tuning is achieved when the measured frequency is equal to the centre frequency of the IF filter.

To measure the input frequency, the number of pulses which occur in a defined time must be counted. This defined time is refered to as 'window'. A wide window indicates a long measuring time and therefore a high accuracy. The counter resolution is defined as Hertz per count. Due to the TEA6100 having to measure the IF frequencies of AM and FM, the counter resolution must be adjustable (different channel spacing). The counter resolution depends on the setting of dividers 1 (N1), divider 2 (N2) and the reference frequency (F_{ref}). The divider ratios of N1 and N2 are controlled by software (see section PROGRAMMING INFORMATION). In Table 3 the window and counter resolution has been calculated for a reference frequency of 40 kHz. The accuracy is controlled by bit 7 of the input word. Although the resolution is the same for bit 7 = logic 0 and bit 7 = logic 1, the width of the window doubles when bit 7 = logic 1.

- bit 7 = 0, accuracy = ± counter resolution
- bit 7 = 1, accuracy = $\pm \frac{1}{2}$ counter resolution

Communication between TEA6100 and the microcomputer is via a two wire bidirectional I^2C bus. The power supply lines are fully isolated to avoid cross talk between the digital and analogue parts of the circuit.

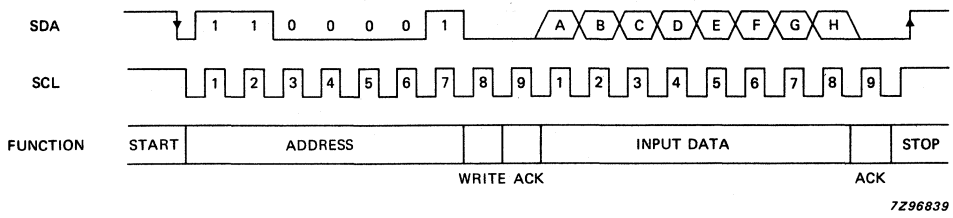


Fig. 3 Input data format waveforms.

Table 2 Input bits

bit	function	logic 0	logic 1	see Figs. 5 and 6
1	reference frequency	32 kHz	40 kHz	A
2	IF mode	AM	FM	B
3	IF input	pin 19	pin 18	C
4	counter input	460 kHz	10,7 MHz	D
5	counter mode	AM	FM	E
6	resolution	divide by 8	divide by 1	F
7	accuracy	LOW	HIGH	G
8	test mode	OFF	ON	H

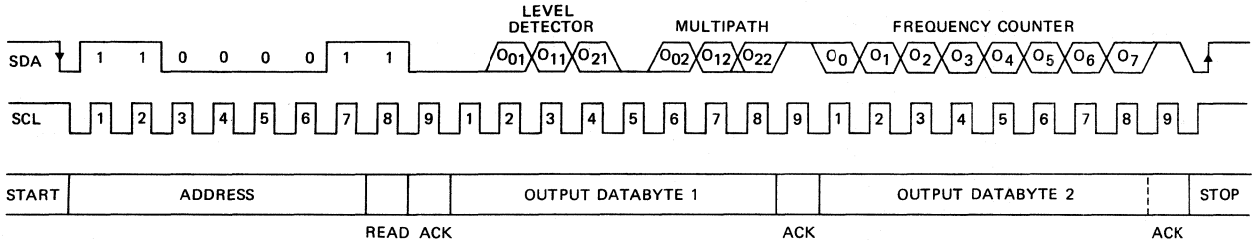


Fig. 4 Output data format waveforms.

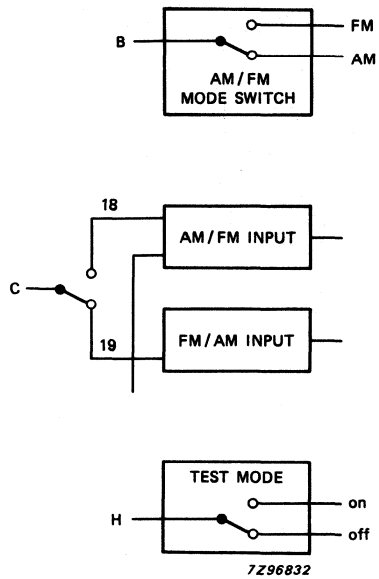


Fig. 5 Switch positions, analogue part (switches drawn in logic 0 state).

DEVELOPMENT DATA

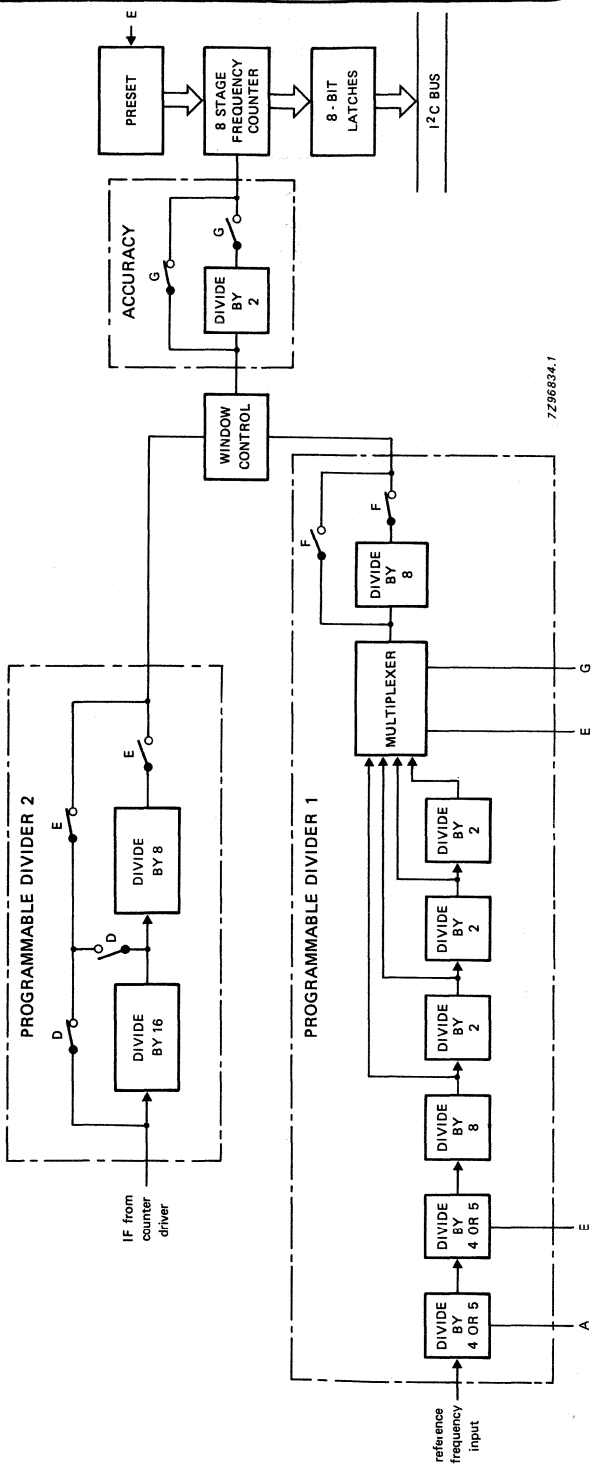


Fig. 6 Switch positions, digital part (switches drawn in logic 0 state, see Tables 2 and 3).

Table 3 Possible window settings and counter resolutions with a 40 kHz reference frequency (see Figs. 5 and 6)

position of switch ADEFG	window (ms)	counter resolution Hz/count	IF frequency (kHz)	read out by IF frequency (hex)	range (kHz)	
					min.	max.
00000	25,6	39,1	460,0	4F	456,914	466,875
10000	32,0	31,3	460,0	CF	453,531	461,500
00001	51,2	39,1	460,0	4F	456,914	466,875
10001	64,0	31,3	460,0	CF	453,531	461,500
00100	128,0	1000,0	460,0	C3	265,000	520,000
10100	160,0	800,0	460,0	36	416,800	620,800
00101	256,0	1000,0	460,0	C3	256,000	520,000
10101	320,0	800,0	460,0	36	416,800	620,800
00010	3,2	312,5	460,0	0F	455,312	535,000
10010	4,0	250,0	460,0	7F	428,250	492,000
00011	6,1	312,5	460,0	0F	455,312	535,000
10011	8,0	250,0	460,0	7F	428,250	492,000
00110	16,0	8000,0	460,0	30	76,000	2116,000
10110	20,0	6400,0	460,0	3F	56,800	1688,800
00111	32,0	8000,0	460,0	30	76,800	2116,000
10111	40,0	6400,0	460,0	3F	56,800	1688,800
01000	25,6	625,0	10700,0	2F	10670,625	10830,000
11000	32,0	500,0	10700,0	E7	10584,500	10712,000
01001	51,2	625,0	10700,0	2F	10670,625	10830,000
11001	64,0	500,0	10700,0	E7	10584,000	10712,000
01100	128,0	1000,0	10700,0	C3	10505,000	10760,000
11100	160,0	800,0	10700,0	36	10656,800	10860,800
01101	256,0	1000,0	10700,0	C3	10505,000	10760,000
11101	320,0	800,0	10700,0	36	10656,800	10860,000
01010	3,2	5000,0	10700,0	AB	9845,000	11120,000
11010	4,0	4000,0	10700,0	C2	9924,000	10944,000
01011	6,4	5000,0	10700,0	AB	9845,000	11120,000
11011	8,0	4000,0	10700,0	C2	9924,000	10944,000
01110	16,0	8000,0	10700,0	30	10316,000	12356,000
11110	20,0	6400,0	10700,0	7F	9887,200	11519,200
01111	32,0	8000,0	10700,0	30	10316,000	12356,000
11111	40,0	6400,0	10700,0	7F	9887,200	11519,200

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	0	13,2	V
Total power dissipation		P_{tot}	see Fig. 7		
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	−30	+85	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 70 K/W

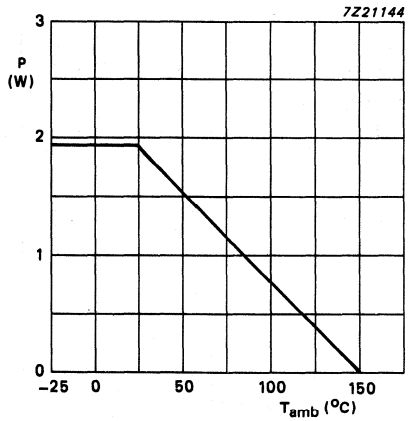


Fig. 7 Power derating curve.

DC CHARACTERISTICS (note)

$V_{P1} = V_{P2} = 8{,}5$ V; $T_{amb} = 25$ °C; all currents positive into the IC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pins 1 and 8	V_{P1}, V_{P2}	7,5	8,5	12	V
Supply current						
FM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	19	25	mA
AM mode	$V_{ADJ} > 2{,}4$ V	I_{P1}	–	15	25	mA
digital part		I_{P2}	–	16	23	mA
Power dissipation		P_d	–	280	–	mW

DEVELOPMENT DATA

AC CHARACTERISTICS (note 1)

V_P = 8,5 V; $V_{i(FM)}$ = 1 mV; f = 10,7 MHz; Δf = 22,5 kHz; f_m = 1 kHz; FM mode; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
IF amplifier, quadrature detector and LF amplifier output	pin 11					
Sensitivity	−3 dB before limiting; inactive mute	$V_{i(FM)}$	–	15	30	μV
Sensitivity	S/N = 26 dB; inactive mute	$V_{i(FM)}$	–	12	–	μV
Signal plus noise to noise ratio	$V_{i(FM)}$ = 10 mV; bandwith = 0,3 to 15 kHz; Δf = 75 kHz	(S + N)/N	–	85	–	dB
IF input range	AM suppression > 40 dB	$V_{i(FM)}$	–	0,09 to 1000	–	mV
Audio output voltage after limiting	Δf = 22,5 kHz	V_o	160	200	240	mV
Total harmonic distortion for single tuned circuit	Δf = 75 kHz	THD	–	0,65	–	%
AM suppression	note 2; see Fig. 8;					
	$V_{i(AM)}$ range = 200 μV to 600 mV	AMS	–	60	–	dB
	$V_{i(AM)}$ range = 200 μV to 600 μV	AMS	–	55	–	dB
Supply voltage ripple rejection	200 Hz; 20 log (V_i/V_o)	SVRR	38	40	–	dB
IF counter inputs						
Frequency counter sensitivity	minimum input voltage for a readout ± 1 bit;					
FM mode	10,7 MHz	$V_{i(FM)}$	–	–	60	μV
AM mode	10,7 MHz	$V_{i(AM)}$	–	–	60	μV
AM mode	460 kHz	$V_{i(AM)}$	–	–	45	μV
Maximum input voltage		V_i	–	–	1	V

parameter	conditions	symbol	min.	typ.	max.	unit
FM level performance	see Fig. 9					
Output voltage adjustment range	$V_{i(FM)}$ = 0 V; pins 3 and 14	V_{LFM}	–	0,1 to 4,6	–	V
Maximum output voltage	pins 3 and 14	V_{LFM}	V_P–1,5	–	–	V
Adjustable gain	$V_{i(FM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(FM)}$	1,4	1,6	1,8	V/dec *
Output impedance of level amplifier	$V_{LFM} > 1$ V	$\|Z_o\|$	–	100	–	Ω
AM level performance	see Fig. 10					
Output voltage adjustment range	$V_{i(AM)}$ = 0 V; pins 5 and 14	V_{LFM}	–	0,1 to 4,6	–	V
	$V_{i(AM)}$ = 10 mV; pins 5 and 14	V_{LAM}	6	–	–	V
Adjustable gain	$V_{i(AM)}/V_{ADJ}$	G_{ADJ}	–	–2	–	dB
Level voltage slope	V_{ADJ} = 2,4 V; $V_{i(FM)}$ = 100 to 10 mV	$S_{i(AM)}$	1,3	1,5	1,7	V/dec *
IF soft muting	V_{LFM}; pin 3; see Fig. 11					
Mute operating range		V_{LFM}	–	0,1 to 2,5	–	V
Mute voltage	–3 dB output attenuation	V_{LFM}	1,20	1,45	1,75	V
Maximum muting	V_{LFM} = 0,1 V	V_{MUTE}	–	19	–	dB
IF hard muting	V_{MUTE}; pin 2					
Mute voltage	–60 dB output attenuation	V_{MUTE}	–	460	–	mV
Mute discharge current	V_{MUTE} = 1 V; V_{LEVEL} = 0 V; mute ON; pin 2	$+I_2$	–	270	–	μA
Mute charging current	V_{MUTE} = 0 V; mute OFF	$-I_2$	–	1,5	–	μA

* V/dec = voltage per decade.

DEVELOPMENT DATA

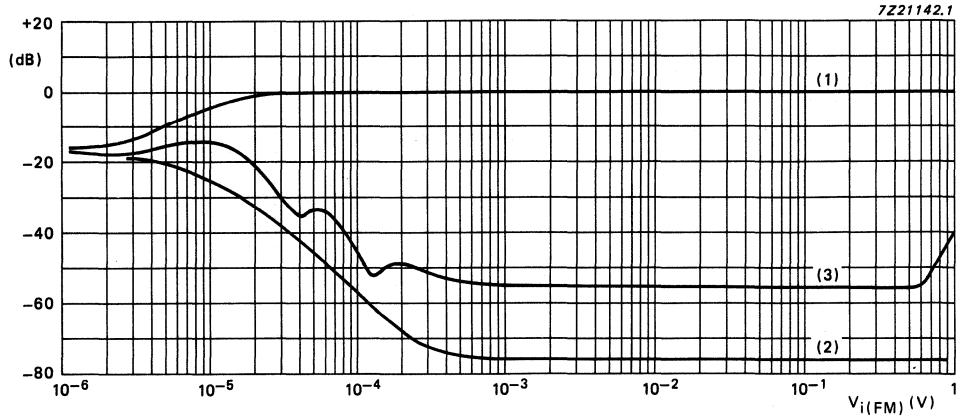
AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Rectifier/amplifier						
Input impedance	pin 4	$\|Z_i\|$	7	10	13	kΩ
Conversion gain AC to DC	pins 4 and 5; bandwith = 100 Hz to 120 kHz; 20 log $V_{O(MP)}$ (d.c.)/ $V_{i(MP)}$ (a.c.)	G_A	–	30	–	dB
DC output voltage range		$V_{O(MP)}$	–	0,2 to 6	–	V
Output characteristics	see Fig. 13; note 3					
Discharge current		I_o	–	200	–	μA
Output ripple in AM mode (peak-to-peak value)	f_m = 200 Hz; m = 0,8; $V_{i(AM)}$ range = 100 μV to 30 mV	V_{ripple}	–	300	400	mV
Multi-path output	see Fig. 12; note 4					
Reference voltage output	pin 15, FM only					
Output voltage		V_{ref}	–	4,4	–	V
Output sink current		$+I_{15}$	–	–	1,5	mA
Output impedance		$\|Z_O\|$	–	–	10	Ω
Output charge current		$-I_{15}$	5	–	–	mA
Output voltage	AM mode	V_{ref}	–	0	–	V
Output impedance	AM mode	$\|Z_O\|$	–	14	–	kΩ
I²C bus data format	see Figs 3 and 4; Table 2					
3-bit ADC	multi-path and level information, note 5					
Trip level LOW		V_{TL}	1,20	1,45	1,75	V
Trip level HIGH		V_{TH}	4,25	4,50	4,75	V
Reference frequency input	pin 6					
Reference range		F_{ref}	–	–	40	kHz
Input voltage LOW		V_{IL}	–	–	0,4	V
Input current HIGH		I_{IH}	5	–	–	μA

Notes to the characteristics

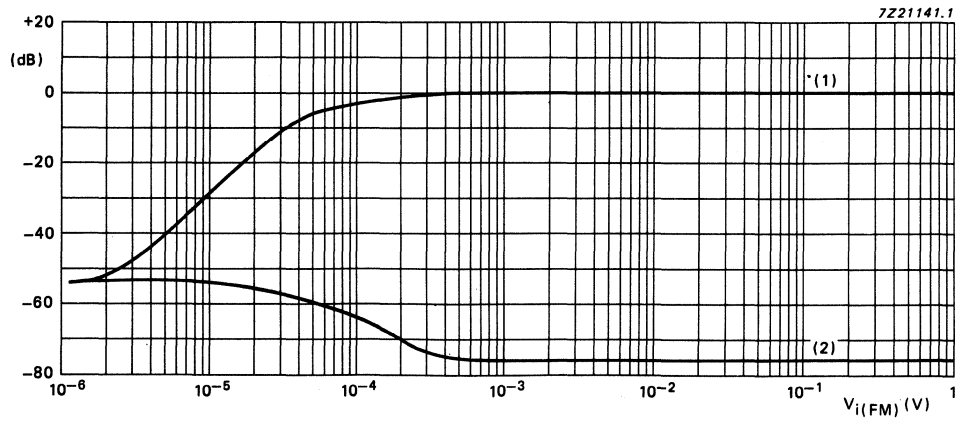
1. All characteristics are measured from the circuit shown in Fig. 13.
2. Conditions for this parameter are:
   20 log $V_{o(FM)}$; m = 0,3 or 20 log $V_{o(AM)}$; m = 0,3.
3. Voltage source followed by diode and resistor.
4. A DC shift can be achieved by connecting a 1,8 MΩ resistor between pin 4 and pin 15.
5. Step size between trip levels:
   $(V_{TH} - V_{TL})/6 \pm 0{,}07$ V.

DEVELOPMENT DATA



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.
(2) Noise (with dBA filter) for V_{ADJ} = 0 V.
(3) AM suppression (m = 0,3 and f_{mod} = 1 kHz) for V_{ADJ} = 0 V.

Fig. 8(a) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.



(1) Audio (Δf = 22,5 kHz and f_{mod} = 1 kHz) for V_{ADJ} = 2,4 V.
(2) Noise (with dBA filter) for V_{ADJ} = 2,4 V.

Fig. 8(b) Audio output voltage performance plotted against input signal, $V_{i(FM)}$.

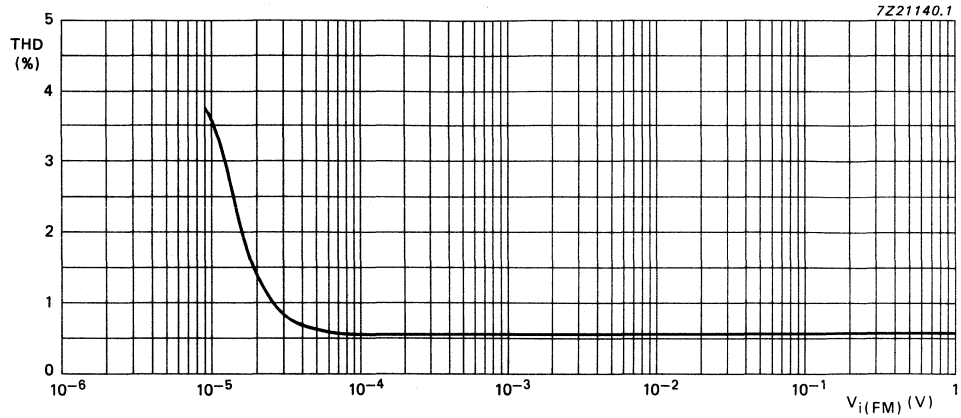
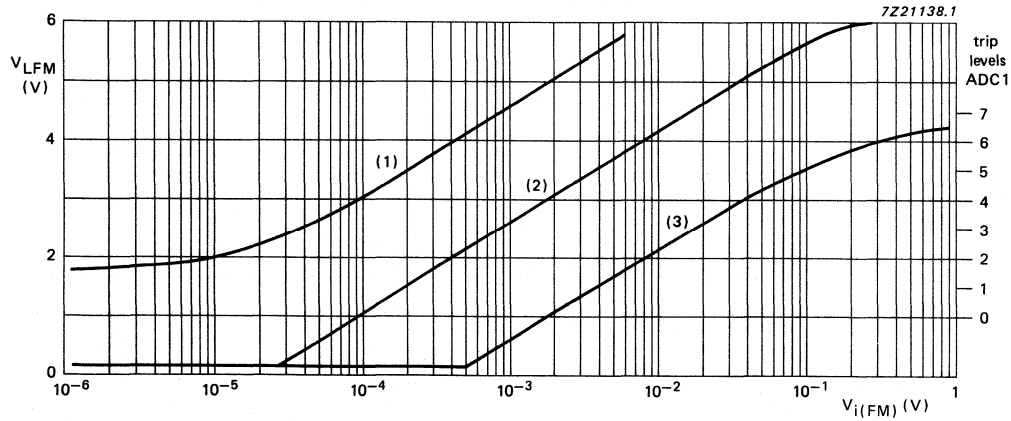


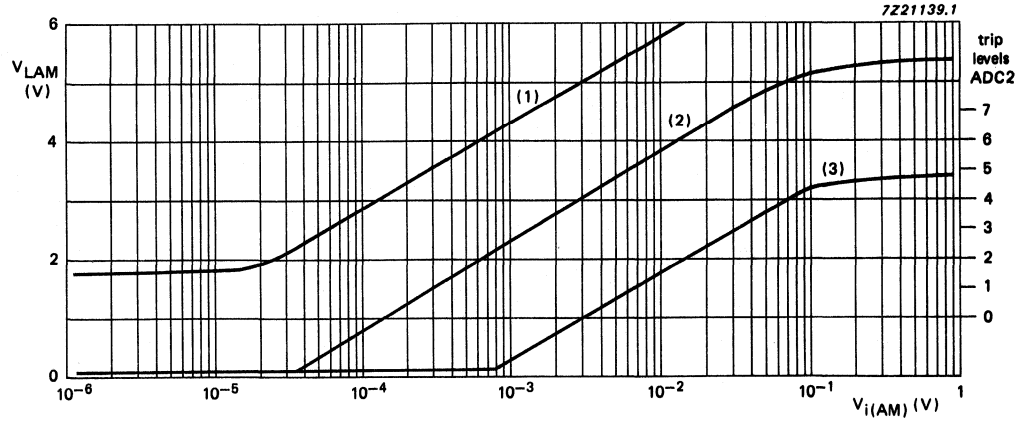
Fig. 8(c) Total harmonic distortion; Δf = 75 kHz, f_{mod} = 1 kHz and V_{ADJ} = 0 V.

DEVELOPMENT DATA



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 9 Level voltage output (V_{LFM}) plotted against IF input signal, $V_{i(FM)}$; IF = 10,7 MHz.



(1) V_{ADJ} = 1,4 V.
(2) V_{ADJ} = 2,4 V.
(3) V_{ADJ} = 3,4 V.

Fig. 10 Level voltage output (V_{LAM}) plotted against IF input signal, $V_{i(AM)}$; IF = 10,7 MHz or 460 kHz.

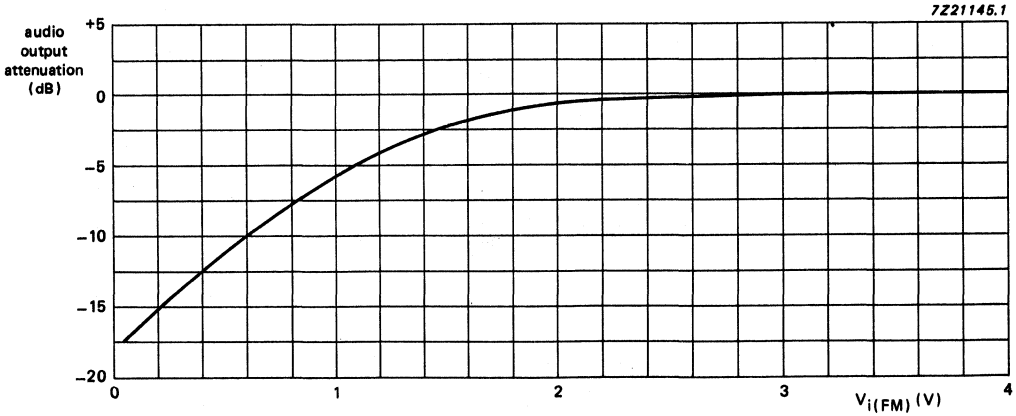
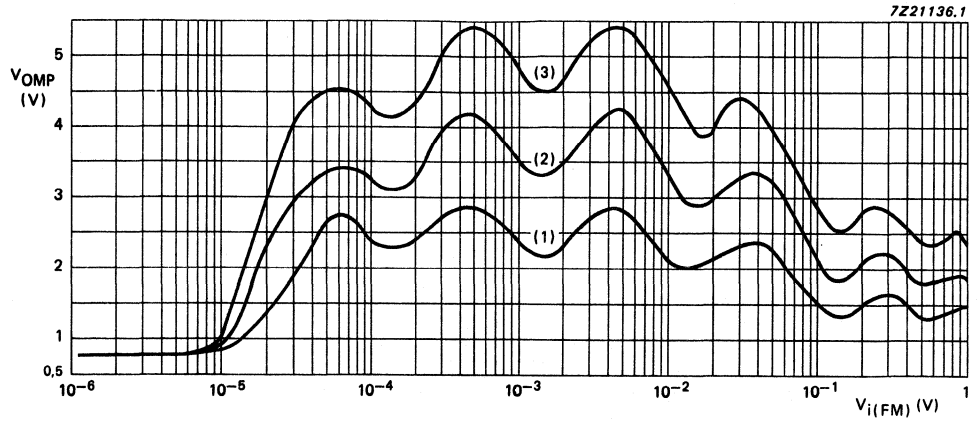


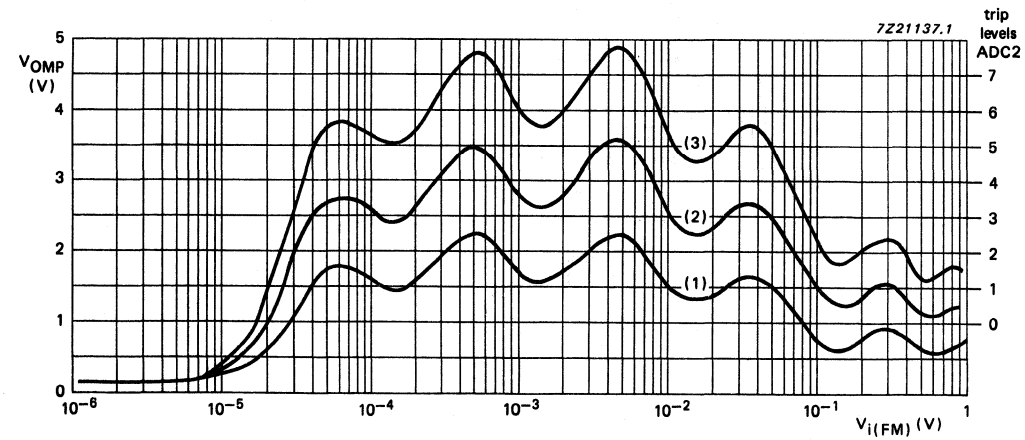
Fig. 11 Soft muting plotted against level output voltage; $V_{i(FM)}$ = 1 mV and Δf = 22,5 kHz.



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(a) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V and 1,8 MΩ resistor connected between pin 4 and pin 15.

DEVELOPMENT DATA



(1) mod = 0,2
(2) mod = 0,3
(3) mod = 0,4

Fig. 12(b) Multi-path output plotted against IF input signal, $V_{i(FM)}$; f_{mod} = 3 kHz (AM, no FM modulation), V_{ADJ} = 2,4 V.

APPLICATION INFORMATION

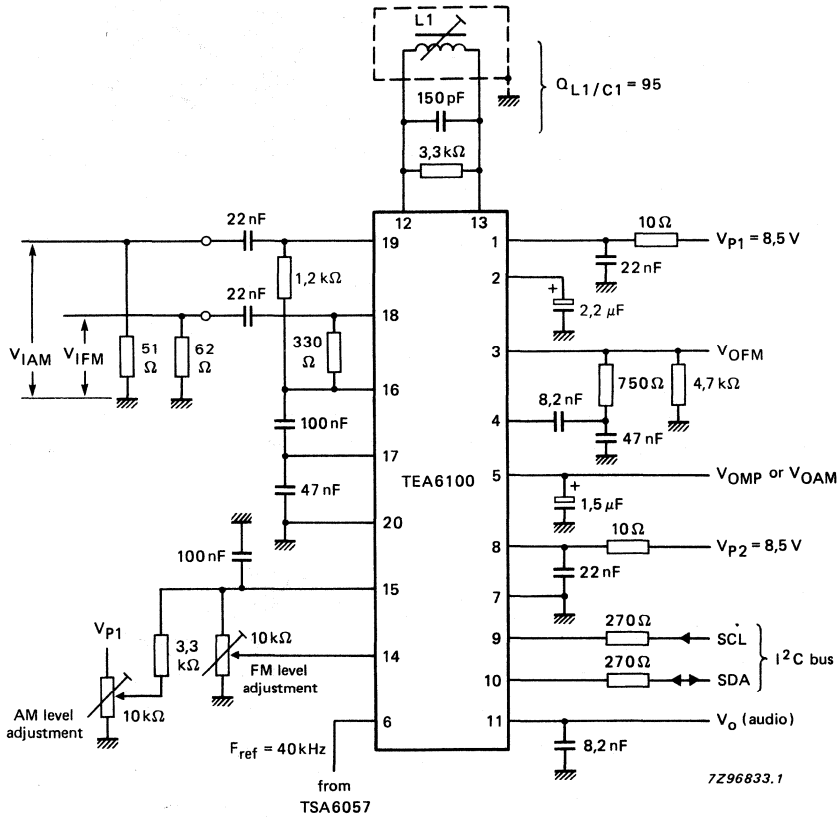


Fig. 13 Application diagram.

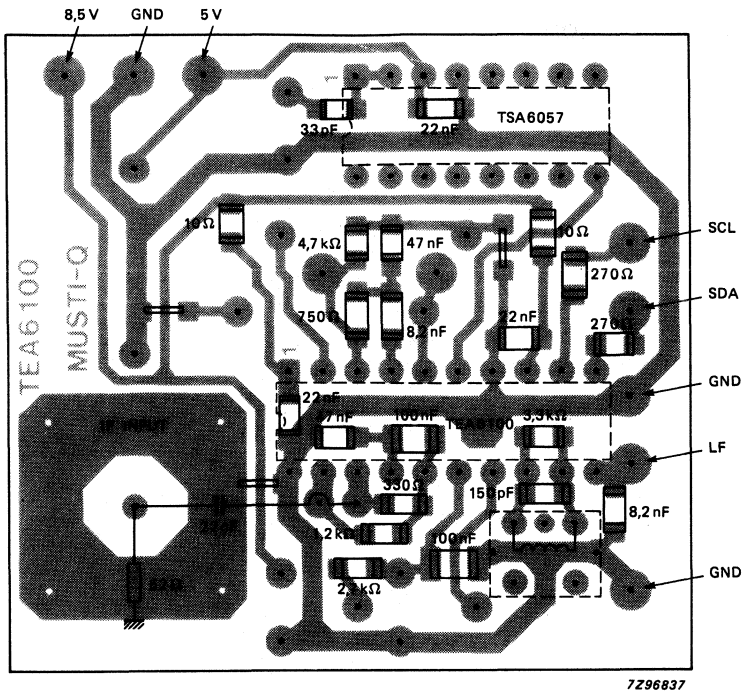


Fig. 14 Track side of printed circuit board.

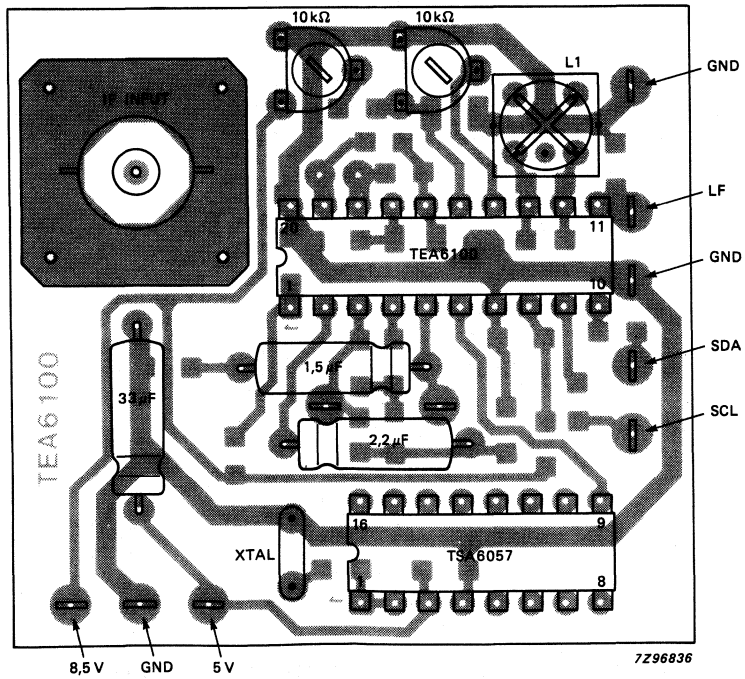
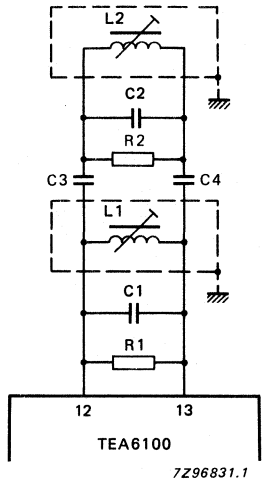


Fig. 15 Component side of printed circuit board.

Double tuned circuit



R1 = 5,1 kΩ, R2 = 1,5 kΩ
C1 = C2 = 150 pF (n = 220)
C3 = C4 = 10 pF
L1 = L2 = 1,6 μH

Fig. 16 Double tuned demodulator circuit.

Alignment of the circuit is obtained with an IF input signal > 200 μV. Tuning the circuit is performed by, detuning L2, adjusting L1 to obtain a minimum distortion level and then adjusting L2 to obtain a minimum distortion level.

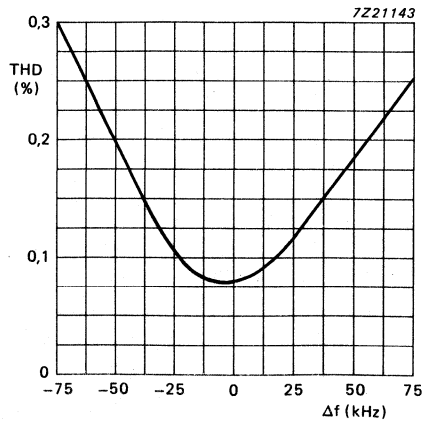


Fig. 17 Total harmonic distortion plotted against IF detuning; for $\Delta f = \pm 75$ kHz, $f_{mod} = 1$ kHz and $V_O = 500$ mV.

PROGRAMMING INFORMATION

Converting the read out of the counters into frequency

The counter resolution at the input is defined as:

- resolution = divider ratio of N2/window

For every increment of the counter the counted frequency increases relative to the resolution in Hertz, as shown in example:

- window = 20 ms; N2 = 128; IF frequency = 10,7 MHz; resolution = 128/0,02 = 6,4 kHz per count

The counter consists of 8 bits. Therefore, the maximum frequency range that can be counted is 256 x resolution = 1,6384 MHz. In the example the frequency to be counted is 10,7 MHz, therefore, the counter will overflow (in the example above, 7 times). The real measured frequency is:

- f_{real} = (read out + overflow x 256) x resolution

The overflow indicates the off-set on the frequency scale which must be added to the read out. Due to the bandwidth of the IF filter, the frequencies at the input to the TEA6100 are known, for example:

- IF filter for FM has a center frequency of 10,7 MHz and −3 dB bandwidth of 300 kHz. Only the frequencies of 10,7 MHz ± 150 kHz occur at the input of the TEA6100. For this reason it is not necessary to count the overflow.

The read out of the counter has to be translated into frequency. This translation depends upon the counter resolution. The preferred way to calculate the input frequency is to:

- calculate the read out of the target IF frequency. Compare this value with that of the measured read out and multiply the difference by the resolution.

The formulae for calculating the target IF read out and the resolution are as follows (A, D, E, F and G refer to the bits of the I^2C bus input data as shown in Figs 3 and 4 and to the counter/timer block diagram shown in Fig. 6. An, Dn, En, Fn and Gn are inverted values of the variables A, D, E, F and G. Table 3 shows the following formulae calculated for a reference frequency of 40 kHz):

- N1 = (An x 4 + A x 5) x (En x 4 + E x 5) x 8 x $(2^{[E \times 2 + G \times 1]})$ x (F x 1 + Fn x 8)
- Window (T) = $N1/F_{ref}$
- N2 = (E x 16 x 8 + En x [Dn x 1 + D x 16]) x (G x 2 + Gn x 1)
- Target decimal read out (TDEC) = T x (TIFF/N2 + (E x 247 + En x 79). TIFF is the symbol for target IF frequency
- Target read out hexadecimal (THEX), convert the target decimal read out to hexadecimal and use the 2 least significant digits (Do not use overflow value). The symbol for measured hexadecimal is MHEX
- Resolution (R) = N2/T
- Measured frequency (F_I) = (TIFF) + R x (MHEX − THEX)

Note

Care should be taken if TIFF + $\frac{1}{2}$ filter bandwidth is greater than the frequency for the read out of hexadecimal value FF, or if TIFF − $\frac{1}{2}$ filter bandwith is less than the frequency at read out for hexadecimal value 00.

- Counter accuracy (AW and AN), with bit 7 (G) the accuracy can be chosen with the same resolution. If bit 7 is logic 1 the accuracy is HIGH and if bit 7 is logic 0 then the accuracy is LOW.

  bit 7 = 0, AN = ± (N2/T)
  bit 7 = 1, AW = ± ($\frac{1}{2}$ x N2/T)

DEVELOPMENT DATA

Example

The example uses the following values:

TIFF = 10,7 MHz; accuracy = LOW (G = 0); F_{ref} = 40 kHz (A = 1); IF frequency = 10, 7 MHz (D = 1); resolution = N1 (F = 1) and counter mode = FM (E = 1)

N1 = (0 x 4 + 1 x 5) x (0 x 4 + 1 x 5) x 8 x ($2^{[1 \times 2 + 0 \times 1]}$) x (1 x 1 + 0 x 8) = 800

T = 800/40 = 20 ms

N2 = (1 x 16 x 8 + 0 x [1 x 1 + 0 x 16]) x (0 x 2 + 1 x 1) = 128

TDEC = 20 x 10,7/128 + (1 x 247 + 0 x 79) = 1919

THEX; 1919 is hexadecimal 77F and the least significant 2 digits are 7F, so THEX = 7 F

R = 128/20 = 6400 Hz/count

Assume the readout is '6E', the measured frequency will be:

- F_I = 10,7 + (6E − 7F) x 6400 = 10,59 MHz

Assume the readout is '83', the measured frequency will be:

- F_I = 10,7 + (83 − 7F) x 6400 = 10,726

Antenna diversity circuit TEA6101/T

Features

- Ability to switch between up to four antennae
- Switching signal derived from two signals: the audio and the level signals
- Floating switching threshold adjusts switching rate to prevailing circumstances:
  - increasing threshold due to excessive noise
  - increasing threshold due to numerous level variations
- Memory for the most favourable antenna signal to overcome unnecessary switching
- Signal-dependent "soft" muting circuit
- Mode selection to the first antenna receiving an AM signal whilst the diversity system is reset.

APPLICATIONS

- Car radio receivers
- Mobile radio communications equipment

GENERAL DESCRIPTION

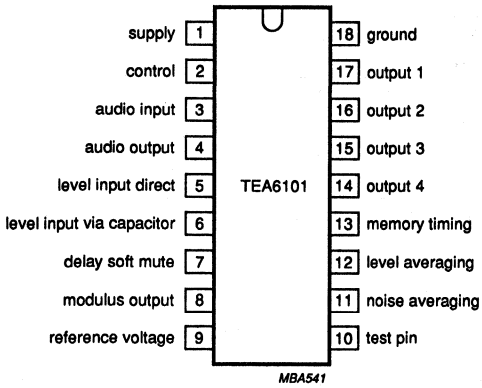
Intended for multi-antenna FM car radio reception (antenna diversity system), the TEA6101/T selects the most favourable signal from one of up to four antennae. Founded upon audible signal disturbance the criteria are derived from two signals: high frequency components (e.g. spikes due to noise and multipath reception) and variations in signal level as a result of multipath reception or fluctuations in field strength.

QUICK REFERENCE DATA

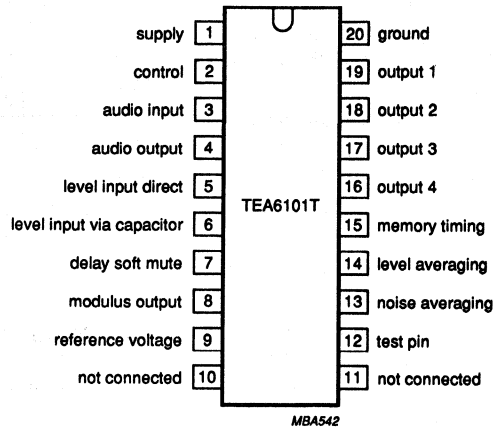
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	-	8.5	-	V
I_p	supply current	-	14	-	mA
$V_{i(p-p)}$	audio input voltage (peak-to-peak value)	-	-	3	V
I_{os}	antenna switch output current (source/sink)	-	-	7	mA
V_L	- 3 dB audio attenuation (soft mute)	-	1.45	-	V
T_{amb}	operating ambient temperature range	- 30	-	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6101	18	DIL	plastic	SOT102
TEA6101T	20	SO20	plastic	SOT163A



a) Pin configuration; TEA6101.



b) Pin configuration; TEA6101T.

Fig.1 Pin configuration.

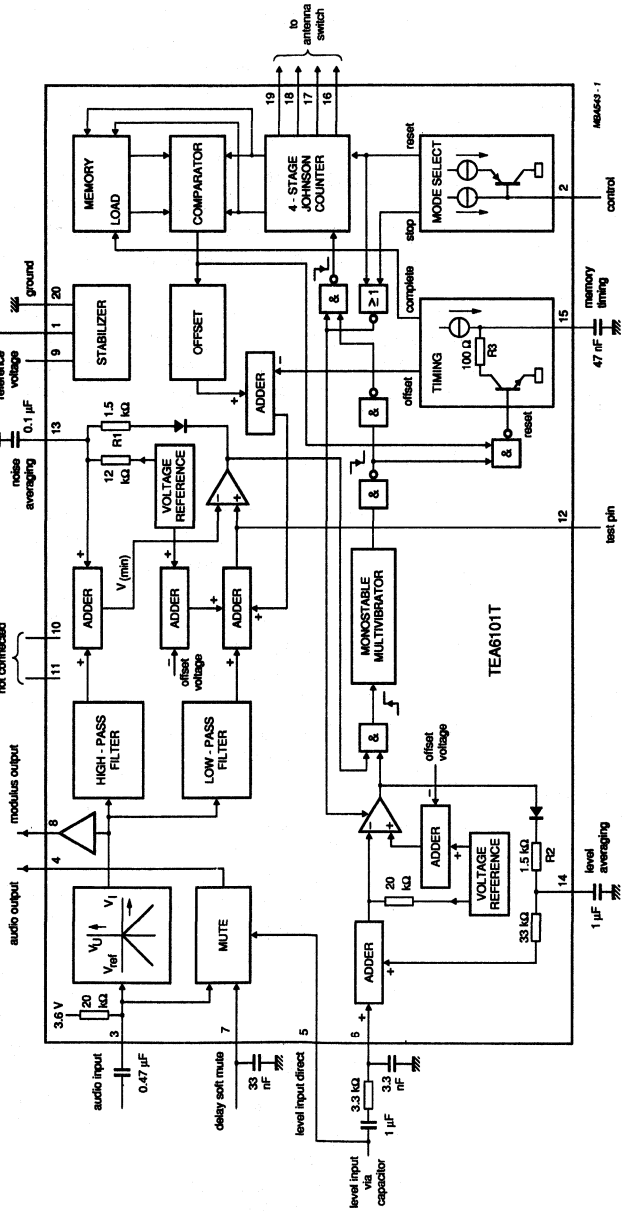


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

Various forms of disturbance can affect signal reception in car radio receivers:

- ignition interference produces spikes on the audio signal. Switching to another antenna will be ineffective. Strong ignition interference, however, will modulate the antenna field strength. In this instance another antenna possessing a directional pattern will suffer less disturbance and switching would be appropriate.
- variation of antenna field strength due to travelling through a zone of variable signal strength will result in a variation in the signal level. Greater noise will be apparent on the audio signal whilst the IF limiter is not limiting. Switching to an alternative antenna input would increase the signal strength.
- multipath reception occurs when a signal reaches the antenna from two or more directions. Often the signals will be of different phase. In certain circumstances the sum of the reflected signals results in zero and a large spike will be evident on the audio signal. It will then be necessary to switch to an alternative antenna from which the sum of the received signals will be different.

The criteria for an antenna diversity system are high frequency components (spikes and noise) on the audio signal in combination with variations in signal level.

Detection of spikes on the audio signal

A rectifier, high pass filter, low pass filter and a comparator are used to detect spikes and noise on the audio signal (see Fig.1). The negative spikes are detected by the rectifier whilst a high pass filter removes the audio signal to leave the high frequency signal components at the negative input to the comparator. The signal at the positive input to the comparator consists of an offset together with an audio signal attenuated by the low pass filter. If the amplitude of the spikes exceed that of the attenuated audio plus offset, the output of the comparator is HIGH.

When the switching rate of the comparator is HIGH, feedback increases the offset via the diode, the resistor R1, and the 100 nF capacitor. The offset is decreased by the 12 kΩ resistor and the 100 nF capacitor (pin 13). The result is an offset based upon the comparator switching rate, rapid to increase but slow to decrease, therefore permitting only the largest spikes to trigger the comparator (floating threshold).

Should high noise be apparent on the audio signal, the offset is decreased by means of the rectifier and high pass filter. This will result in more frequent switching to an alternative antenna whilst the result of the switching operation will be less audible.

Detection of voltage level variation

A 1 µF input capacitor and 20 kΩ resistor remove the absolute level voltage to leave only variations to be detected. The level comparator output is HIGH when the variations in level voltage are greater than the offset. Similarly to the audio comparator; the feedback diode, resistor R2, the 1 µF capacitor and the 33 kΩ resistor cause the threshold level to float. During periods of high activity the comparator thus switches only on the largest variations.

Switching to an alternative antenna

When both the level and the audio comparator outputs are HIGH, another output of the Johnson counter will be selected. Since switching to an alternative antenna would cause a disturbance of the audio and level signals the monostable multivibrator will prohibit the counter from selecting another antenna input for 21 µs.

Memory and timing

Approximately similar qualities of signal originating from different antennae could result in unnecessary antenna switching. This is prevented by appointing a priority antenna. The selection of an antenna without priority results in the audio offset being decreased by 1.2 V such that the audio comparator will have a HIGH output voltage. During the period of memory timing the offset increases towards the normal offset value. Should level alterations occur during this period another antenna will be selected. If, however, the memory is timed-out without the occurrence of signal variation, priority will be appointed to the selected antenna. Thus a priority antenna will be selected for the majority of the time during reception of almost all similarly weak antenna signals.

Mute

A mute function should not precede the circuit. This function is therefore assumed by the TEA6101. When used in combination with the

TEA6100 the 20 kΩ input of the IF IC together with the 6 kΩ output resistor of the TEA6101 cause an attenuation of 3 dB. The mute circuit therefore has 3 dB amplification of level voltages in excess of 2.75 V.

Mode selection

The diversity system is intended for FM reception. To avoid an audible disturbance if it is used with an AM system, the circuit can be reset. In the reset mode antenna 1 (pin 17 (19)) is selected and both comparators are switched off to prevent pulses reaching the output.

For FM search tuning the diversity system may be similarly disabled. The selected antenna will again be retained with the comparators being inhibited.

Test pin

Although intended for test purposes the test pin can be used to increase the audio offset (resistor from pin 10 (12) to ground) or to change the compensation factor (resistor between pin 8 (8) and 10 (12)). These modifications permit the behaviour of the antenna switch to be adapted to alternative IF amplifier IC's.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_p	supply voltage	0	12	V
P_{tot}	total power dissipation	-	see Fig. 3	-
T_{amb}	operating ambient temperature range	–30	+85	°C
T_{stg}	storage temperature range	–65	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$R_{th\ c\text{-}a}$	crystal to ambient SOT102		-	75	K/W
$R_{th\ c\text{-}a}$	crystal to ambient SOT163A		-	100	K/W

DC CHARACTERISTICS

Measurements using application circuit (Fig 1) at T_{amb} = 25 °C and V_p = 8.5 V. Voltages with respect to pin 18 (20); all currents positive into the IC unless otherwise specified.

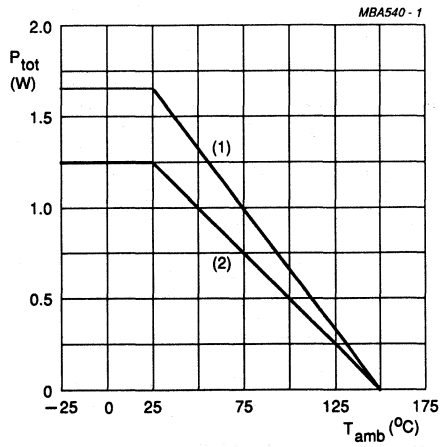
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage		7.5	8.5	12	V
I_p	supply current	I_{OS} = 0 mA	-	14	-	mA
P_{tot}	total power dissipation		-	119	-	mW
	voltage at pin:					
	1 (1)		-	8.5	-	V
	2 (2)		-	7.8	-	V
	3 (3)		-	3.6	-	V
	4 (4)		-	5.4	-	V
	5 (5)		-	0	-	V
	6 (6)		-	5.3	-	V
	7 (7)		-	0.6	-	V
	8 (8)		-	5.2	-	V
	9 (9)		-	5.4	-	V
	(10)		-	n.c.	-	
	(11)		-	n.c.	-	
	10 (12)		-	5.1	-	V
	11 (13)		-	5.4	-	V
	12 (14)		-	5.3	-	V
	13 (15)		-	0	-	V
	14 (16)		-	0	-	V
	15 (17)		-	0	-	V
	16 (18)		-	0	-	V
	17 (19)		-	7.5	-	V
	18 (20)		-	0	-	V

AC CHARACTERISTICS

V_p = 8.5 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute "Soft Mute" (V_L)						
Z_i	input impedance (pin 3 (3))		-	20	-	kΩ
	mute range	$\frac{V_{aud}\,(a\ V_L = 2.75\ V)}{V_{aud}\,(a\ V_L = 0.1\ V)}$	17	19.3	-	dB
V_{aud}/V_i	mute gain	V_L = 2.75 V	-	2.7	-	dB
V_{aud}/V_i	mute gain	V_L = 1.45 V	−1	0.6	2	dB
"Hard Mute" (V_{mute})						
V_{mute}	- 60 dB output attenuation		-	455	-	mV
$+I_m$	"ON" sink current	V_{mute} = 1 V, V_L = 0 V	-	370	-	µA
$-I_m$	"OFF" source current	V_{mute} = 0 V	3	-	-	µA
Harmonic distortion						
THD		V_i = 200 mV, V_L = 2.5 V	-	0.09	-	%
V_i	audio input voltage (peak-to-peak value)	THD > 10%	3	-	-	V
Signal to noise ratio						
(S+N)/N	measured with dB(A) curve	V_{aud} = 600 mV, 1 kHz	-	76	-	dB
Ripple rejection (see note)						
V_{aud}/V_p		300 Hz, 100 mV, V_L = 2.5 V	28	32	-	dB
Reference voltage V_{ref}						
V_{ref}	output voltage		-	5.34	-	V
Audio comparator						
V_{off1}	offset voltage	$V_{off1} = V_{min} - V_{ap}$ (with priority)	-	+ 250	-	mV
V_{off1}		no priority, V_t = 0 V	-	- 1100	-	mV
V_{off1}		V_t = 3 V	-	- 348	-	mV
Level comparator						
V_{ref}-V_{il}	voltage for high comparator output		-	56	-	mV
Monostable multivibrator						
	started with both comparator outputs HIGH					
T	period		16	21	28	µs
Timing/memory						
$-I_t$	source current		-	30	-	µA
C_t	value delay capacitor		-	-	50	nF
T_t	timing duration	C_t = 47 nF	-	6	-	ms
$+I_t$	reset current	V_t = 3 V	-	17.7	-	mA
V_t	change of priority antenna		-	3.7	-	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Antenna switch outputs						
$-I_{os}$	output source current		-	-	7	mA
$+ I_{os}$	output sink current		-	-	7	mA
V_{os}	voltage selected output	I_{os} = –10 mA	V_p - 2	-	-	V
V_{os}		I_{os} = 0 mA	V_p- 1 V	-	-	V
V_{os}	Voltage not selected output	I_{os} = + 10 mA	-	-	0.7V	V
V_{os}		I_{os} = 0 mA	-	-	0.1	V
Mode selection						
	enable					
V_r	all functions active		-	-	1	V
$-I_r$	input current	VR = 1	-	-	12	µA
	reset (active at open input)					
V_r	first antenna pin 17 (19)		4.2	-	V_p	V
	stop					
V_r	keep selected antenna		1.6	-	3.5	V
Note to the AC characteristics						
When V_p (pin 1 (1)) is filtered with R = 25 Ω and C = 100 µF the ripple rejection becomes 46 dB						



(1) SOT102

(2) SOT163A

Fig.3 Derating curves.

INTEGRATED AM UPCONVERSION RECEIVER

GENERAL DESCRIPTION

The TEA6200 is an integrated AM upconversion receiver circuit with an IF of 10.7 MHz. Because of the high dynamic range of the RF prestage there is no tuned prestage. The whole selectivity is provided by crystal filters. The circuit is intended for use in AM radios with synthesizer tuning.
The TEA6200 can handle RF signals up to 2 V RMS.

Features

- No pre-tuned selection is required
- No LW/MW switching
- RF input is protected from static discharge from the aerial
- Electronic standby switch
- Voltage controlled oscillator for synthesizer tuning
- IF output providing level information for search tuning.
- No alignment required.

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	7.6	8.5	9.4	V
Supply current range	I_P	–	50	70	mA
AF output voltage with: RF at 1 MHz and 10 mV f_m at 400 Hz and 30%	V_{af}	–	350	–	mV
AGC start	V_{rf}	30	50	80	μV
AGC range	ΔV_{rf}	–	95	–	dB

PACKAGE OUTLINE

20-lead dual in line; plastic (SOT146).

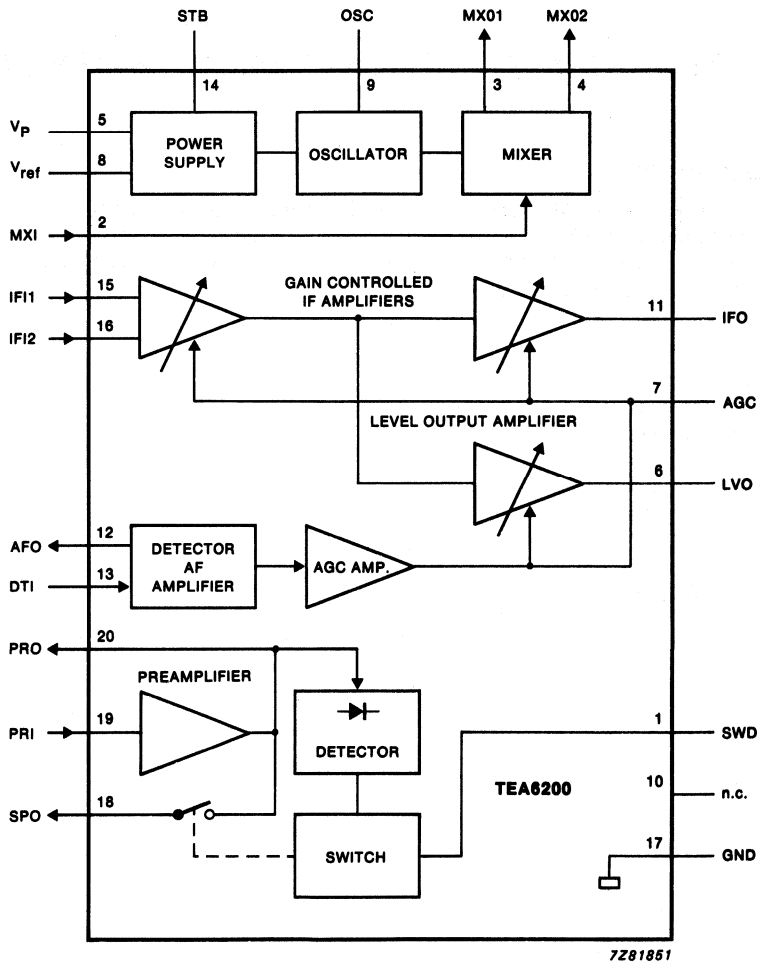


Fig. 1 Block diagram.

PINNING

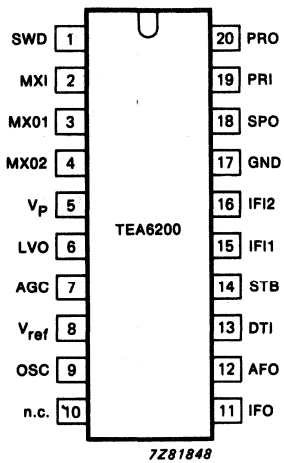


Fig. 2 Pinning diagram.

1	SWD	switching delay
2	MXI	mixer input
3	MXO1	mixer output 1
4	MXO2	mixer output 2
5	V_P	supply voltage
6	LVO	level output
7	AGC	AGC time constant
8	V_{ref}	reference voltage
9	OSC	oscillator
10	n.c.	not internally connected*
11	IFO	IF output
12	AFO	AF output
13	DTI	detector input
14	STB	standby switch
15	IFI1	IF input 1
16	IFI2	IF input 2
17	GND	ground
18	SPO	switched prestage output
19	PRI	prestage input
20	PRO	prestage output

* Pin 10 must be connected to pin 5, 8 or 17.

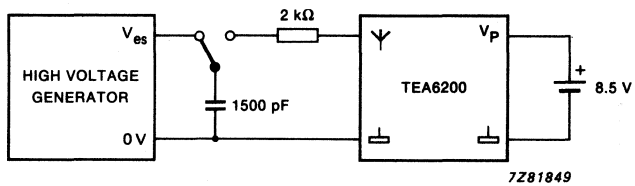
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	12	V
Supply current	I_P	–	70	mA
Total power dissipation	P_{tot}	–	850	mW
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 150	°C
Electrostatic discharge voltage	$\pm V_{es}$	–	10	kV

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 80 K/W



Will tolerate discharge between −10 kV and + 10 kV.

Fig. 3. Test circuit in accordance with IEC 315-1 clause 25.

DC CHARACTERISTICS

V_P = 8.5 V; V_{14} = V_P; Signal in OFF condition; all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Mixer input		V_I	–	4.0	–	V
Mixer output 1		V_O	–	8.5	–	V
Mixer output 2		V_O	–	8.5	–	V
Level output		V_O	–	8.5	–	V
AGC voltage		V_{AGC}	–	0.65	–	V
Reference voltage		V_{ref}	–	4.0	–	V
Oscillator DC voltage		V_{OSC}	–	4.0	–	V
Prestage input		V_I	–	1.2	–	V
Prestage output		V_O	–	3.2	–	V

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; f_{RF} = 1 MHz at 10 mV RMS; Q_{OSC} = 50; modulation = 400 Hz at 30%; insertion loss of filters: crystal filter = 1 dB; ceramic filter = 4 dB, all voltages referenced to ground unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	7.6	8.5	9.4	V
Supply current range		I_P	–	50	70	mA
Guaranteed operating voltage		V_P	7.0	–	10.0	V
Standby switch						
ON voltage		V_{14}	3.2	–	V_P	V
OFF voltage		V_{14}	0	–	1	V
ON current		$\|I_{14}\|$	–	–	10	μA
OFF current		$-I_{14}$	–	–	0.5	mA
Supply current	device OFF	I_P	–	–	10	mA
Prestage	note 1					
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis		V_{rf}	1.5	3.5	5.5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Frequency range		f_{osc}	10.8	–	17.8	MHz
Oscillator amplitude		V_{osc}	200	420	–	mV
Tuned circuit selectivity		Q_{OSC}	20	50	–	–
Mixer						
Input capacitance		$C_{2\text{-}8}$	–	5	10	pF
Input impedance		$Z_{2\text{-}8}$	10	40	–	kΩ
Conversion transconductance		$I_{3\text{-}4}/V_{2\text{-}8}$	–	3.8	–	S
IF amplifier						
Input impedance		$R_{16\text{-}15}$	10	–	–	kΩ
Input capacitance		$C_{16\text{-}15}$	–	–	5	pF
Output impedance		Z_{11}	230	330	430	Ω
Detector	note 2					
Input impedance		Z_{13}	265	380	500	Ω
Output impedance		Z_{12}	7	10	14	kΩ
Output level		V_{af}	250	350	500	mV
Reference voltage						
Voltage	V_P = 8.5 V	V_8	3.8	4.0	4.2	V
Output impedance		Z_8	–	20	–	Ω
Ripple rejection		$\frac{\Delta V_P}{\Delta V_8}$	40	–	–	dB
Level output pin 6	see Fig. 5					
Output impedance		Z_6	–	1	–	kΩ
Output voltage	V_{rf} = 70 μV	V_6	0.5	0.7	1.0	mV
Output voltage	V_{rf} = 2 mV	V_6	–	15	–	mV

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input	(S + N)/N = 6 dB	V_{rf}	–	11	20	μV
	(S + N)/N = 26 dB	V_{rf}	–	110	150	μV
	(S + N)/N = 46 dB	V_{rf}	–	1100	2000	μV
	RF = 150 kHz (S + N)/N = 26 dB	V_{rf}	–	200	–	μV
Output signal						
AF output voltage	V_{rf} = 10 mV	V_{af}	250	350	500	mV
	V_{rf} = 20 μV	V_{af}	–	100	–	mV
Total distortion	V_{rf} = 1 mV; modulation = 80%	d_{tot}	–	3	5	%
Signal plus noise-to-noise ratio	RF = 10 mV to 1 V	(S+N)/N	53	57	–	dB
Ripple rejection	V_P = 8.5 V + V_r 20 Hz < fR < 20 kHz V_{rms} = 40 mV	$\frac{\Delta V_P}{\Delta V_{af}}$	20	–	–	dB
Large signal handling						
Aerial input voltage	THD = 10%; modulation = 80%	V_{rf}	2	3	–	V
AGC range of preamplifier switch			–	12	–	dB
Switching threshold	modulation = 80%	V_{rf}	–	320	–	mV
Hysteresis	modulation = 80%	V_{rf}	1.5	3.5	5.5	dB
Ripple rejection of preamplifier	20 Hz < f_R < 1.5 MHz	$\frac{\Delta V_P}{\Delta V_{20}}$	–	40	–	dB
AGC						
AGC range			–	95	–	dB
Change of V_{af}	100 μV < V_{rf} < 2 V		–	2	3	dB
AGC start		V_{rf}	30	50	80	μV
Intermodulation free dynamic range						
Long wave second order	350/250 kHz input noise level = –99 dBm	IMFDR2	72	82	–	dB
third order	input noise level = –99 dBm	IMFDR3	–	86	–	dB
Medium wave second order	650/1550 kHz input noise level = –104 dBm	IMFDR2	74	84	–	dB
third order	1.25/1.4 MHz input noise level = –104 dBm	IMFDR3	–	90	–	dB

Notes to the characteristics

1. The prestage is connected to the aerial by a 6 MHz low-pass filter that decouples unwanted aerial cable resonance frequencies. The large dynamic range of the prestage is achieved by use of a transimpedance amplifier with a feedback loop consisting of an equivalent aerial capacitance and a feedback capacitor. When large RF signals are received the feedback capacitance in the loop is increased and the gain subsequently reduced, (see Fig. 4).

   Voltage gain for small signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1}$

   Voltage gain for large signals $G_V = V_{rf} \times \frac{C_{ae}}{C_1 + C_2}$

2. To protect the demodulator and the AGC circuitry, against parasitic oscillation in the IF section, a ceramic filter is connected between the IF output and detector input.

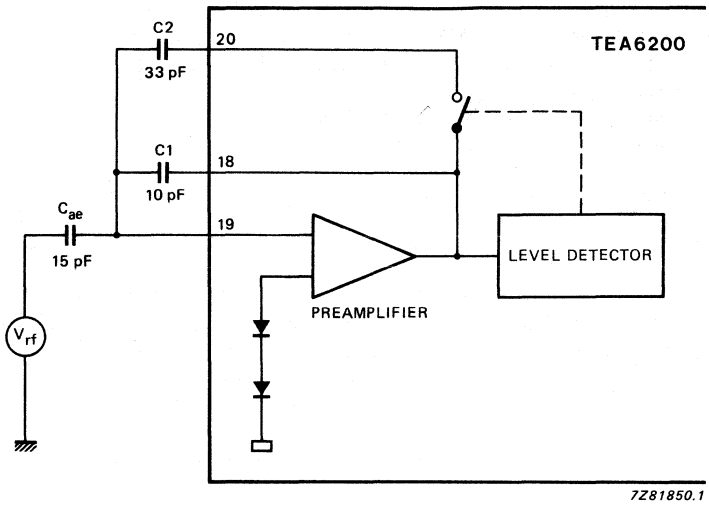


Fig. 4 Prestage circuit.

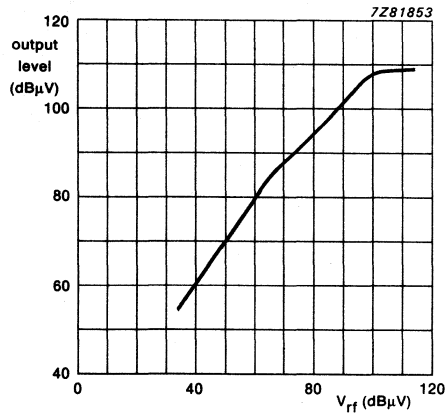


Fig. 5 IF output level.

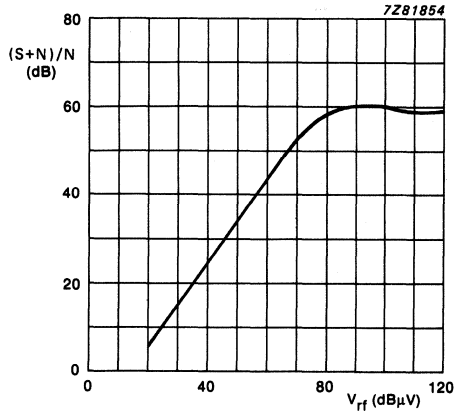


Fig. 6 Signal plus noise-to-noise ratio.

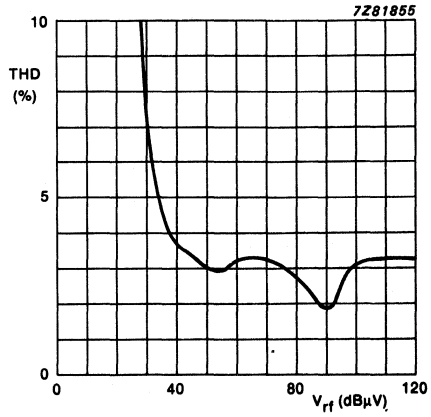


Fig. 7 Total harmonic distortion.

APPLICATION INFORMATION

Notes Fig. 8.

	Component	Circuit identity	Supplier reference
(1)	Crystal filters	XTAL	NDK 10T 7 BA
(2)	Ceramic filter	SFE	Murata E 10 7 S
(3)	Transformer	T1	Toko 7PS-1078 JK
(4)	Variable capacitance diode.	D1	BB609, BB809 or BBY40
(5)	Oscillator coil	L1	Toko 7PS-1077 X

APPLICATION INFORMATION

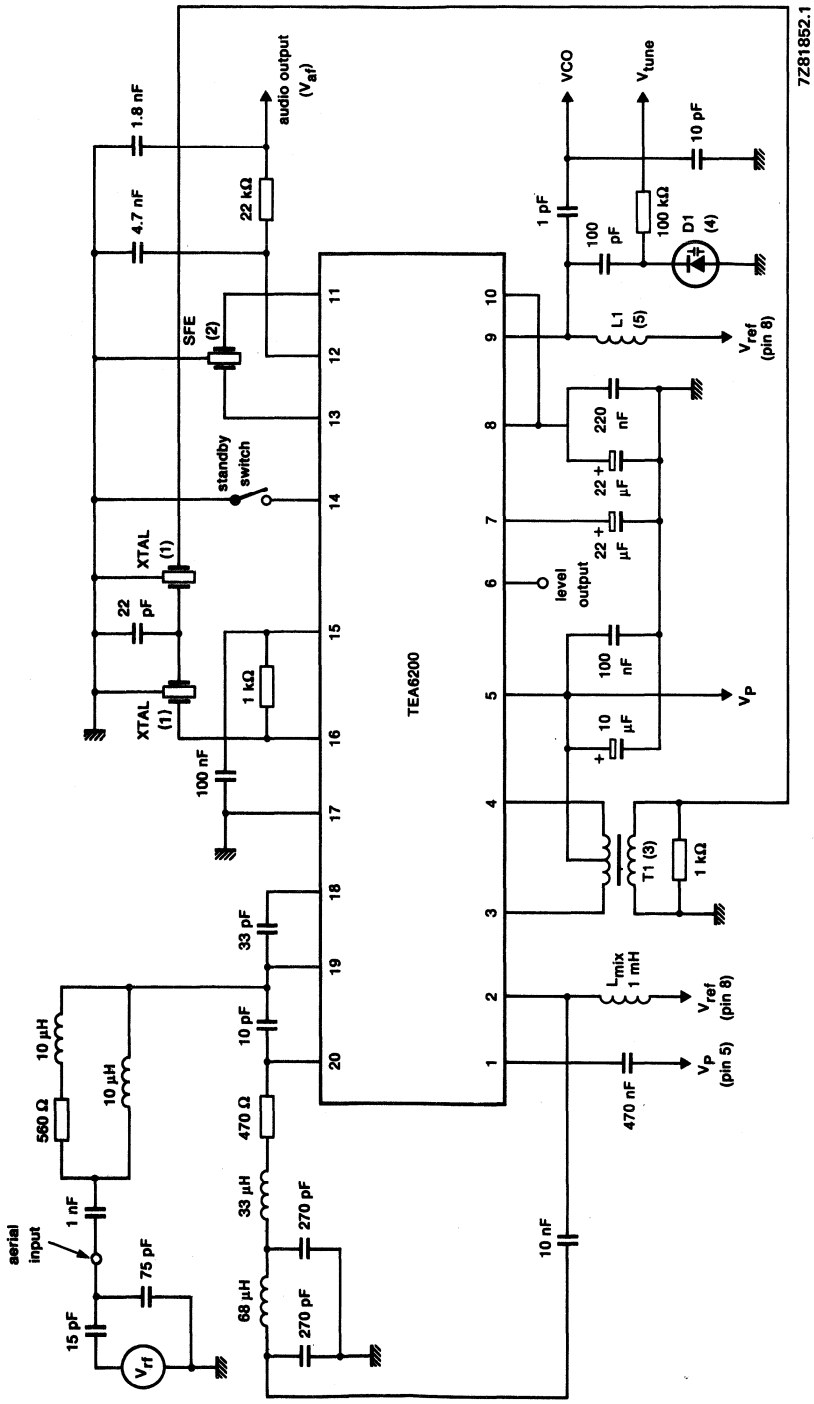


Fig. 8 Application diagram.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

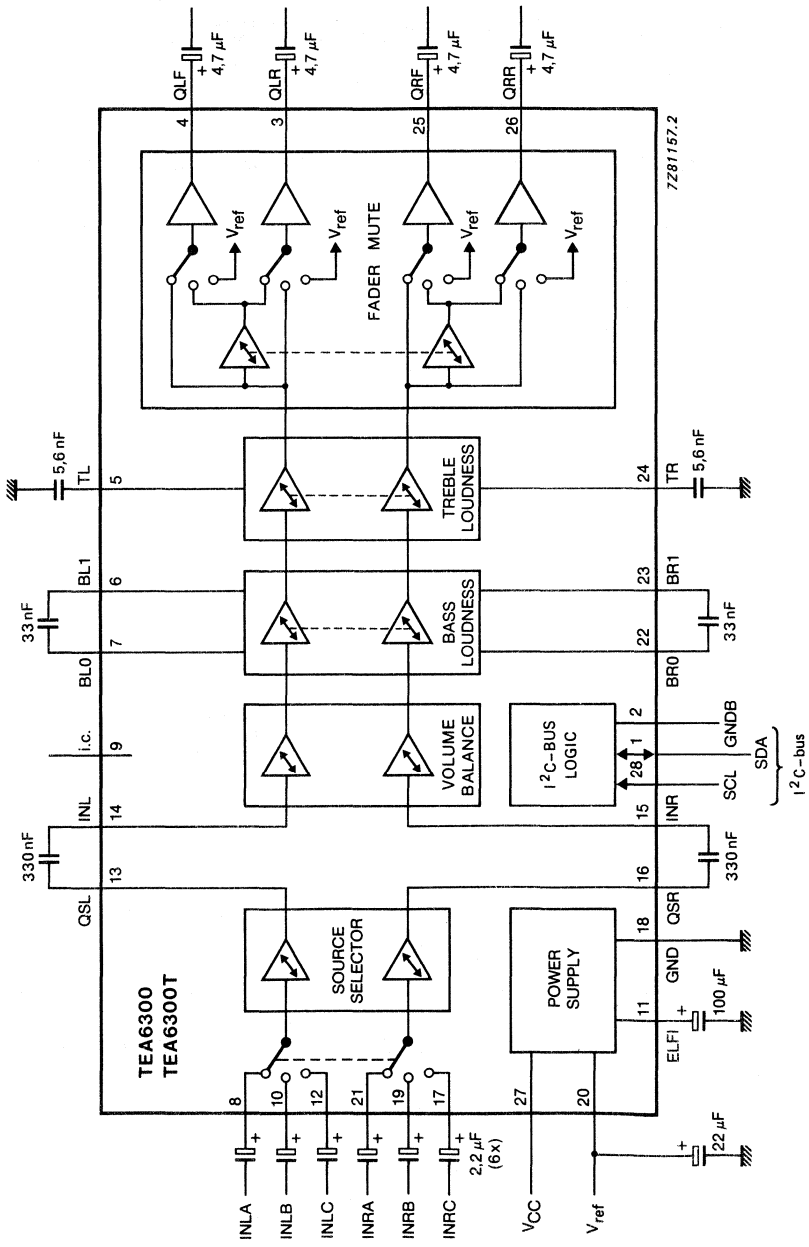


Fig. 1 Block diagram.

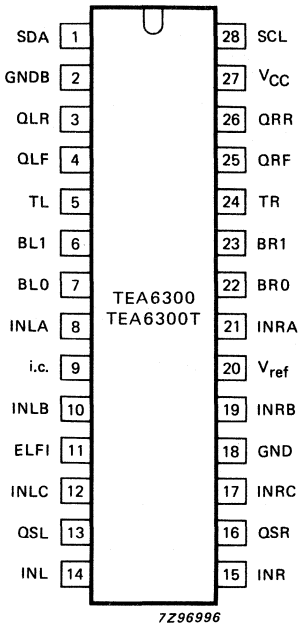


Fig. 2 Pinning diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels —RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	33	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency –1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	92	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = –10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)} < 200$ mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal plus noise-to-noise ratio bass and treble linear; notes 1 and 2 CCIR 468-2 weighted; quasi peak					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	(S + N)/N	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	(S + N)/N	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	70	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	(S + N)/N	65	78	–	dB
V_i = 50 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	70	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	(S + N)/N	–	85	–	dB
Noise output power mute position, only contribution of TEA6300; power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_V = 0 dB; bass and treble linear	α_B	–	110	–	dB
Source selector					
Input impedance	Z_i	20	30	40	kΩ
Output impedance	Z_o	–	–	100	Ω
Output load resistance	R_L	10	–	–	kΩ
Output load capacity	C_L	0	–	200	pF
Input isolation not selected source; frequency range 40 Hz to 12,5 kHz	α_S	–	80	–	dB
Voltage gain $R_L \geqslant 10$ kΩ	G_v	–	0	–	dB
Internal bias voltage ratio	$V_{b\,int}/V_{ref}$	–	1	–	
Maximum input voltage level (RMS value)					
THD < 0,5%	$V_{i(rms)}$	–	1,65	–	V
THD < 0,5%; V_{CC} = 7,5 V	$V_{i(rms)}$	–	1,5	–	V
Total harmonic distortion V_i = 500 mV; R_L = 10 kΩ	THD	–	–	0,1	%
Noise output voltage weighted CCIR 468-2, quasi peak	V_{no}	–	9	20	μV
DC offset voltage between any inputs	V_o	–	–	10	mV
Control part					
Source selector disconnected, source resistance 600 Ω					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF

parameter	symbol	min.	typ.	max.	unit
Maximum input voltage THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	72	90	–	dB
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position G_v = 0 to −66 dB		–	–	10	mV
In any bass position G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Fader control					
Continuous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	+ 1,5	V
Input current					
HIGH	I_{IH}	−10	–	+ 10	μA
LOW	I_{IL}	−10	–	+ 10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I²C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I²C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage					
start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front rear dB	dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front rear dB	dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

selected inputs	DATA SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

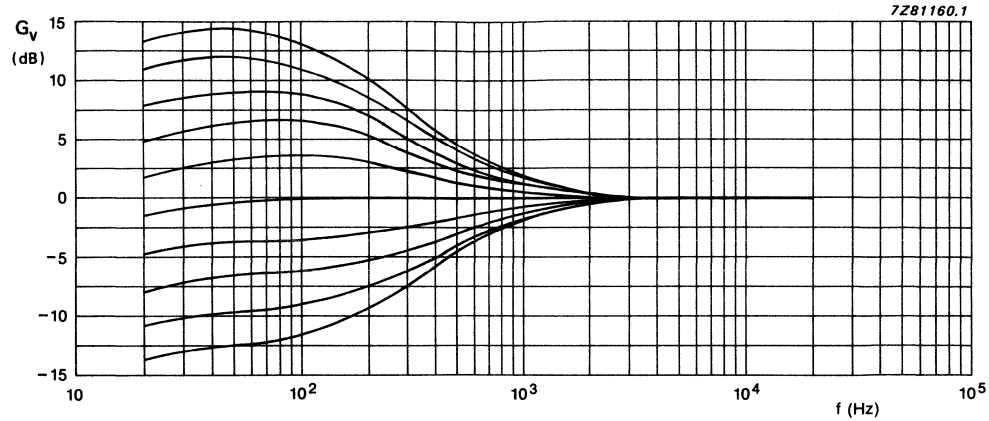


Fig. 3 Bass control without T-pass filter.

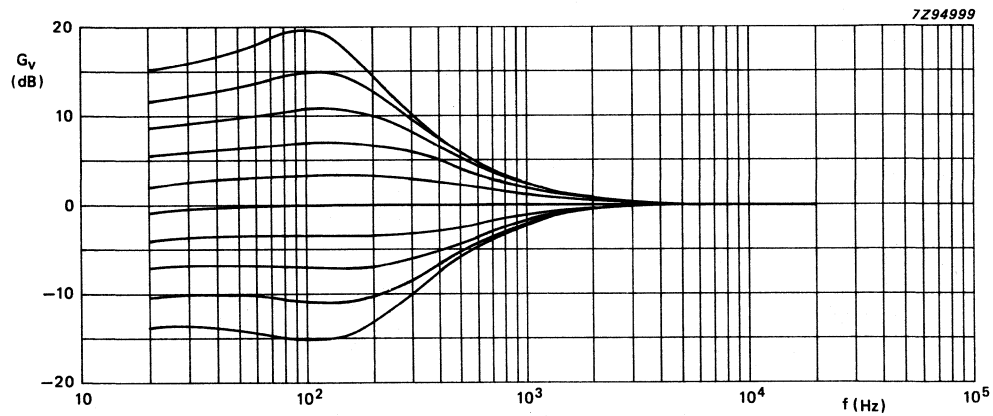
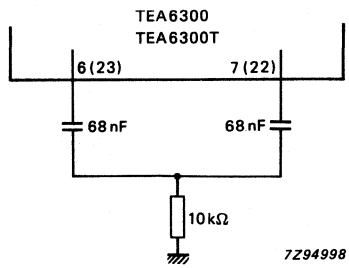


Fig. 4 Bass control with T-pass filter.



Pin numbers in parenthases refer to the bass control, right channel.

Fig. 5 T-pass filter.

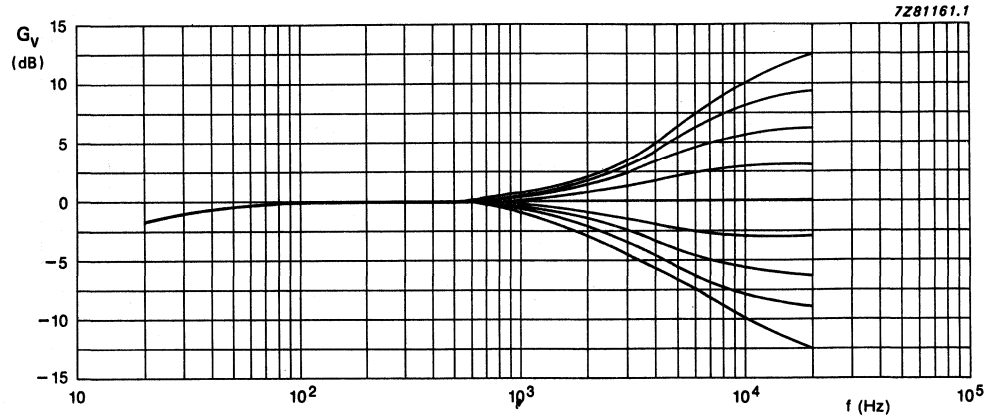


Fig. 6 Treble control.

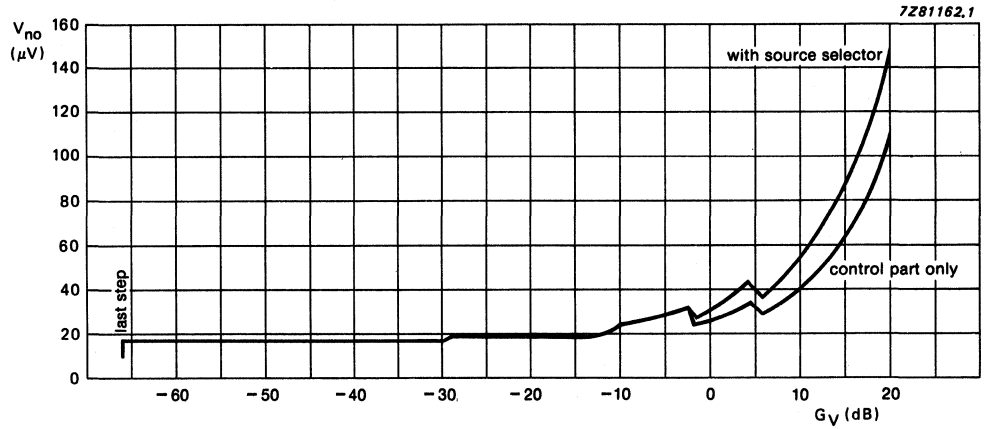


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

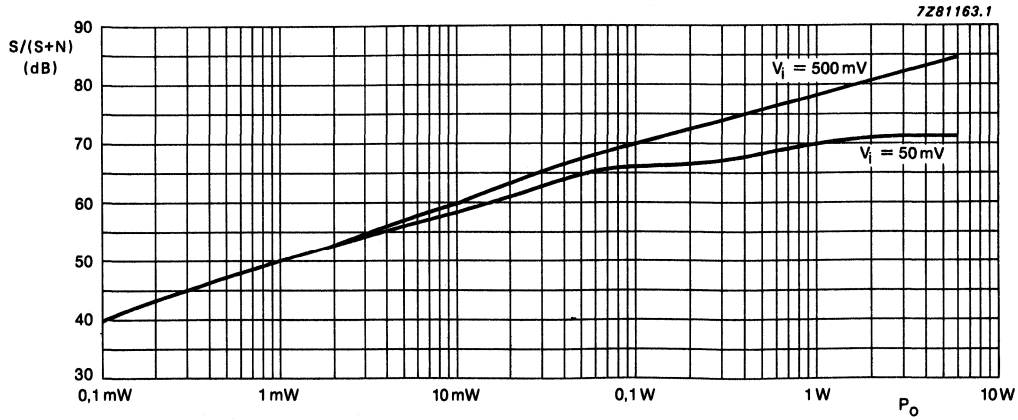


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

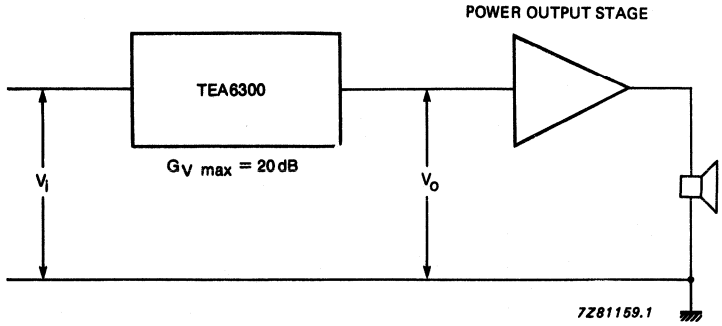


Fig. 9 Recommended level diagram; $V_{i\ min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

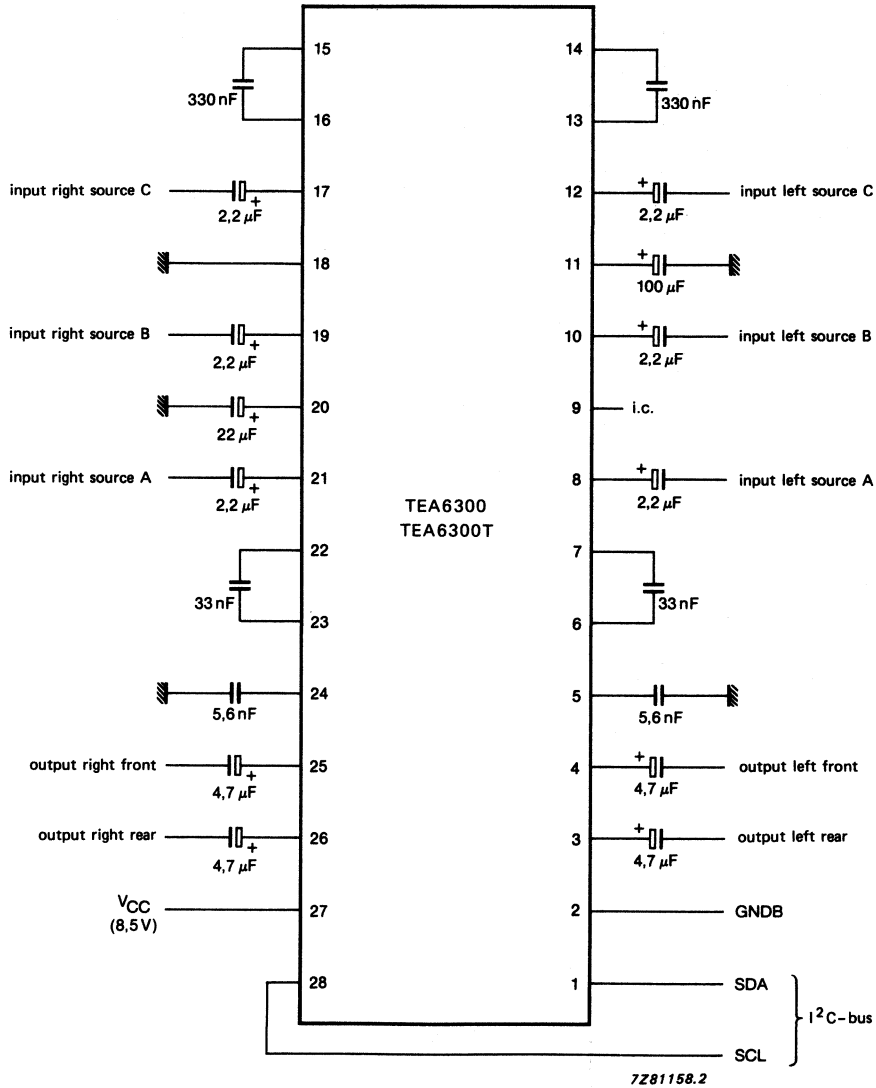


Fig. 10 Test and application circuit.

SOUND FADER CONTROL CIRCUIT

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled tone and volume control circuit for car radios.

Features

- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from +15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control form 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for Dolby* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Input sensitivity for full power at the output stage	$V_{i(rms)}$	–	50	–	mV
Input signal handling	$V_{i(rms)}$	–	1,65	–	V
Frequency response	f_r	35	–	20 000	Hz
Channel separation f = 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Signal plus noise-to-noise ratio	(S+N)/N	–	80	–	dB
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licencing Corporation, San Fransisco, California (U.S.A.).

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

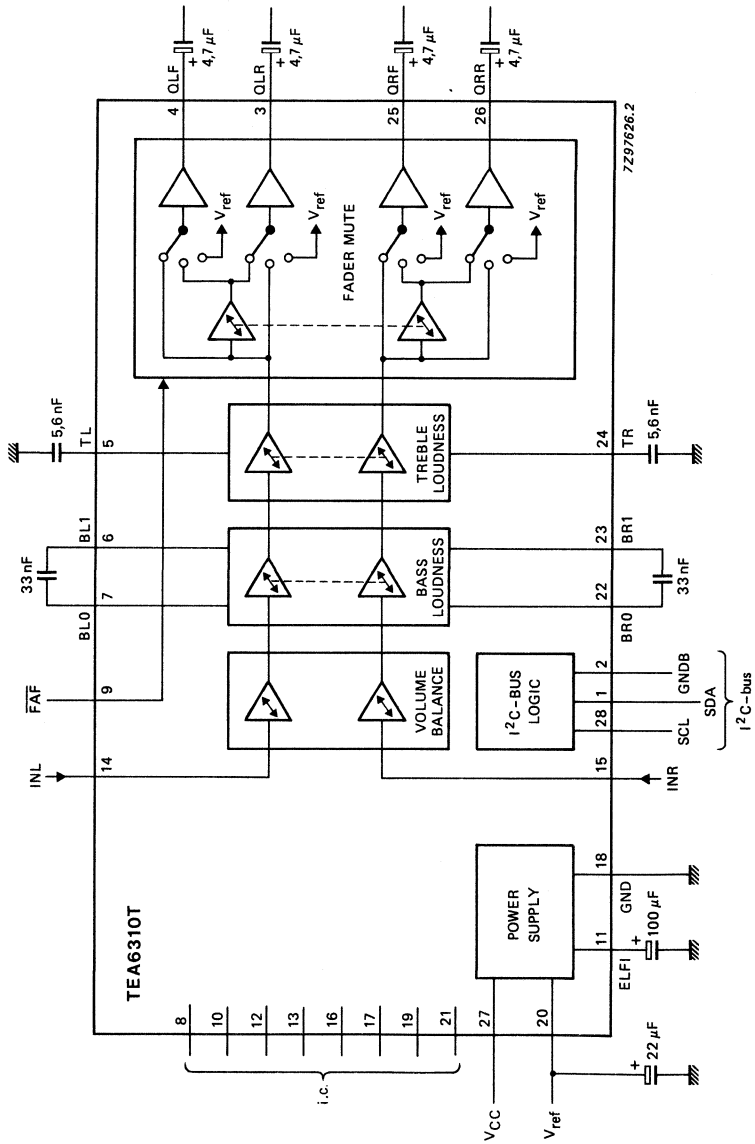


Fig. 1 Block diagram.

DEVELOPMENT DATA

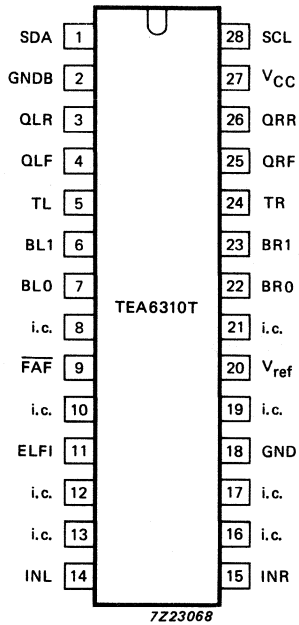


Fig. 2 Pinning diagram

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	i.c.	internally connected
9	$\overline{FAF}$	fader off control input
10	i.c.	internally connected
11	ELFI	electronic filtering for supply
12	i.c.	internally connected
13	i.c.	internally connected
14	INL	input left control part
15	INR	input right control part
16	i.c.	internally connected
17	i.c.	internally connected
18	GND	ground
19	i.c.	internally connected
20	V_{ref}	reference voltage (1/2 V_{CC})
21	i.c.	internally connected
22	BR0	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2C-bus)

FUNCTIONAL DESCRIPTION

The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6310T has four outputs a low level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. The Fader function can be disabled by an input signal at $\overline{FAF}$ (pin 9).
An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6310T is required.

The on-chip power-on-reset sets the TEA6310T to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 27-18)	V_{CC}	–	16	V
Maximum power dissipation	P_{tot}	–	1	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	7,0	8,5	13,2	V
Supply current	I_{CC}	–	26	–	mA
Supply current at 8,5 V	I_{CC}	–	–	30	mA
Supply current at 13,2 V	I_{CC}	–	–	44	mA
DC voltage inputs, outputs and reference	V_{DC}	0,45	0,5	0,55	V_{CC}
Internal reference voltage (pin 20) V_{ref} = 0,5 V_{CC}	V_{REF}	–	4,25	–	V
Maximum voltage gain bass and treble linear, fader off	G_v	19	20	21	dB
Output voltage level for P_{max} at the output stage	$V_{o(rms)}$	–	500	–	mV
for start of clipping	$V_{o(rms)}$	–	1000	–	mV
Input sensitivity at V_o = 500 mV	$V_{i(rms)}$	–	50	–	mV
Frequency response bass and treble linear; roll-off frequency −1 dB	f_r	35	–	20 000	Hz
Channel separation G_v = 0 dB; bass and treble linear; frequency range 250 Hz to 10 kHz	α_{CS}	70	96	–	dB
Total harmonic distortion frequency range 20 Hz to 12,5 kHz					
V_i = 50 mV; G_v = 20 dB	THD	–	0,1	0,3	%
V_i = 500 mV; G_v = 0 dB	THD	–	0,05	0,2	%
V_i = 1,6 V; G_v = −10 dB	THD	–	0,2	0,5	%
Ripple rejection $V_{r(rms)}$ <200 mV; G_v = 0 dB; bass and treble linear;					
at f = 100 Hz	RR_{100}	–	70	–	dB
at f = 40 Hz to 12,5 kHz	RR_{range}	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio; bass and treble linear; notes 1 and 2; CCIR 468-2 weighted; quasi peak;					
V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	S/(S + N)	–	65	–	dB
V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	S/(S + N)	–	67	–	dB
V_i = 50 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	72	–	dB
V_i = 500 mV; V_o = 200 mV; P_o = 1 W	S/(S + N)	65	78	–	dB
V_i = 50 mV, V_o = 500 mV; P_o = 6 W	S/(S + N)	–	72	–	dB
V_i = 500 mV; V_o = 500 mV; P_o = 6 W	S/(S + N)	–	86	–	dB
Noise output power mute position, only contribution of TEA310T, power amplifier for 25 W	P_{no}	–	–	10	nW
Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$) between bus inputs and signal outputs G_v = 0 dB; bass and treble linear;	α_B	–	110	–	dB
Control part					
Input impedance	Z_i	35	50	65	kΩ
Output impedance	Z_o	–	100	150	Ω
Output load resistance	R_L	5	–	–	kΩ
Output load capacity	C_L	0	–	2500	pF
Maximum input voltage; THD < 0,5%; G_v = −10 dB; bass and treble linear	$V_{i(rms)}$	–	2,0	–	V
Noise output voltage; weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off;					
G_v = 20 dB	V_{no}	–	110	220	μV
G_v = 0 dB	V_{no}	–	25	50	μV
G_v = −66 dB	V_{no}	–	19	38	μV
mute position	V_{no}	–	11	22	μV
Volume control					
Continuous control range	G_c	–	86	–	dB
Step resolution		–	2	–	dB
Attenuator set error; (G_v = + 20 to −50 dB)	ΔG_a	–	–	2	dB
Attenuator set error; (G_v = + 20 to −66 dB)	ΔG_a	–	–	3	dB
Gain tracking error; balance in mid position, bass and treble linear	ΔG_t	–	–	2	dB
Mute attenuation	α_m	76	90	–	dB

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
DC step offset					
Between any adjoining step and any step to mute					
G_v = 0 to −66 dB		–	0,2	10	mV
G_v = 20 to 0 dB		–	2	15	mV
In any treble and fader position					
G_v = 0 to −66 dB		–	–	10	mV
In any bass position					
G_v = 0 to −66 dB		–	–	20	mV
Bass control					
Bass control range;					
f = 40 Hz; maximum boost	G_b	14	15	16	dB
f = 40 Hz; maximum attenuation	G_b	11	12	13	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Treble control					
Treble control range					
f = 15 kHz; maximum boost	G_t	11	12	13	dB
f = 15 kHz; maximum attenuation	G_t	11	12	13	dB
f > 15 kHz; maximum boost	G_t	–	–	15	dB
Step resolution		–	3	–	dB
Step error		–	–	0,5	dB
Fader control					
Continous attenuation fader control range	G_f	–	30	–	dB
Step resolution		–	2	–	dB
Attenuator set error		–	–	1,5	dB
Mute attenuation	α_m	74	84	–	dB
Fader enable/disable control (pin 9)					
Fader enabled					
Input voltage HIGH	$V_{9\text{-}18}$	3	–	12	V
Fader disabled					
Input voltage LOW	$V_{9\text{-}18}$	−0,3	–	1,5	V
Input current					
HIGH	I_9	−10	–	+10	μA
LOW	I_9	−10	–	+10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Digital part					
Bus terminals					
Input voltage					
HIGH	V_{IH}	3	–	12	V
LOW	V_{IL}	−0,3	–	1,5	V
Input current					
HIGH	I_{IH}	−10	–	+10	μA
LOW	I_{IL}	−10	–	+10	μA
Output voltage LOW I_L = 3 mA	V_{OL}	–	–	0,4	V
AC characteristics					
in accordance with the I^2C-bus specification					
Power-on-Reset					
When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position					
Increasing supply voltage					
start of reset	V_{CC}	–	–	2,5	V
end of reset	V_{CC}	5,2	6,0	6,8	V
Decreasing supply voltage start of reset	V_{CC}	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 10000 0000
A = acknowledge, generated by the slave
SUBADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

function	subaddress	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	00000000	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	00000001	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	00000010	X	X	X	X	BA3	BA2	BA1	BA0
treble	00000011	X	X	X	X	TR3	TR2	TR1	TR0
fader	00000100	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	00000101	GMU	X	X	X	X	X	X	X

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

DEVELOPMENT DATA

Table 2 Bass setting

G_V dB	DATA			
	BA3	BA2	BA1	BA0
+ 15	1	1	1	1
+ 15	1	1	1	0
+ 15	1	1	0	1
+ 15	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V dB	DATA			
	TR3	TR2	TR1	TR0
+ 12	1	1	1	1
+ 12	1	1	1	0
+ 12	1	1	0	1
+ 12	1	1	0	0
+ 12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

DEVELOPMENT DATA

Table 4 Volume setting LEFT

G_v dB	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_v dB	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Mute control

MUTE control	DATA GMU	remarks
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

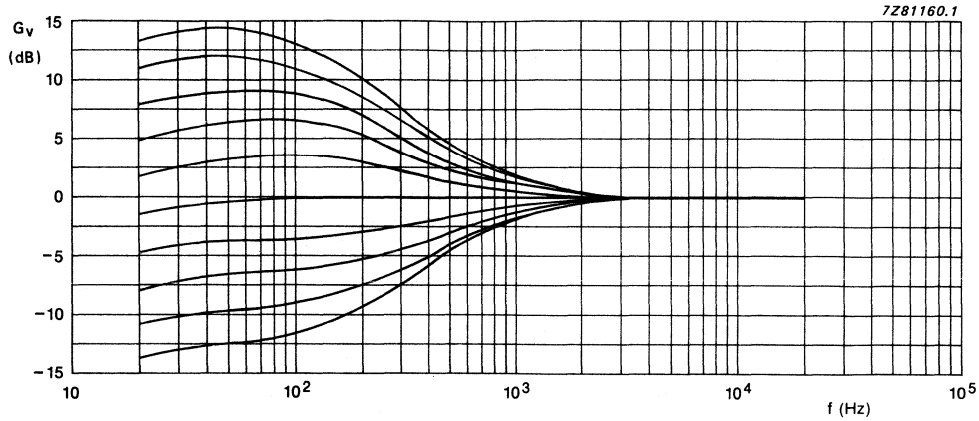


Fig. 3 Bass control without T-pass filter.

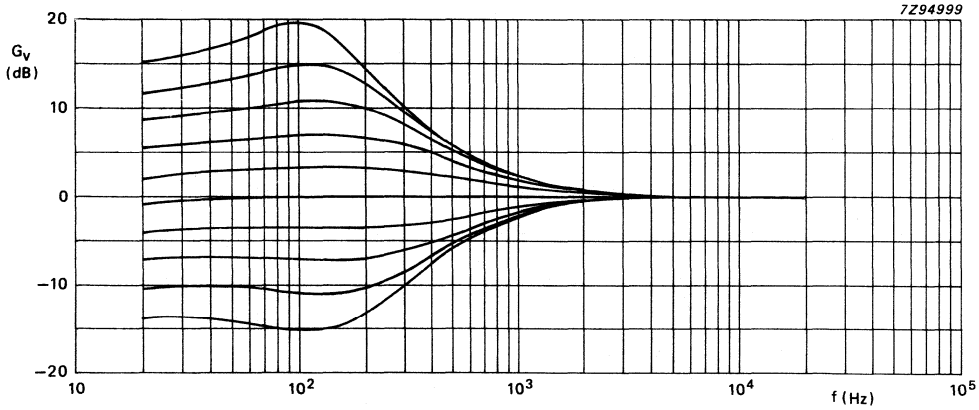
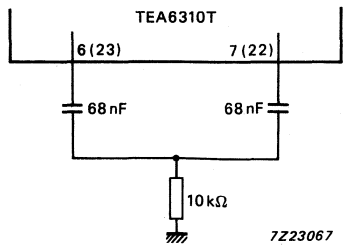


Fig. 4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig. 5 T-pass filer.

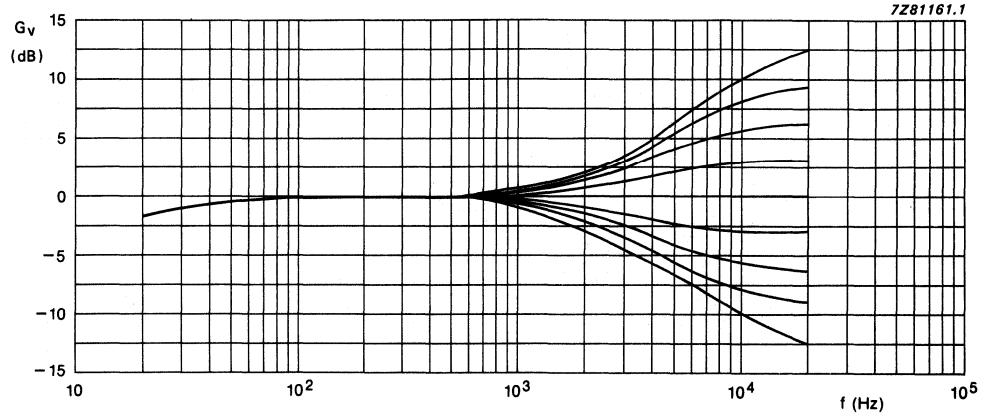


Fig. 6 Treble control.

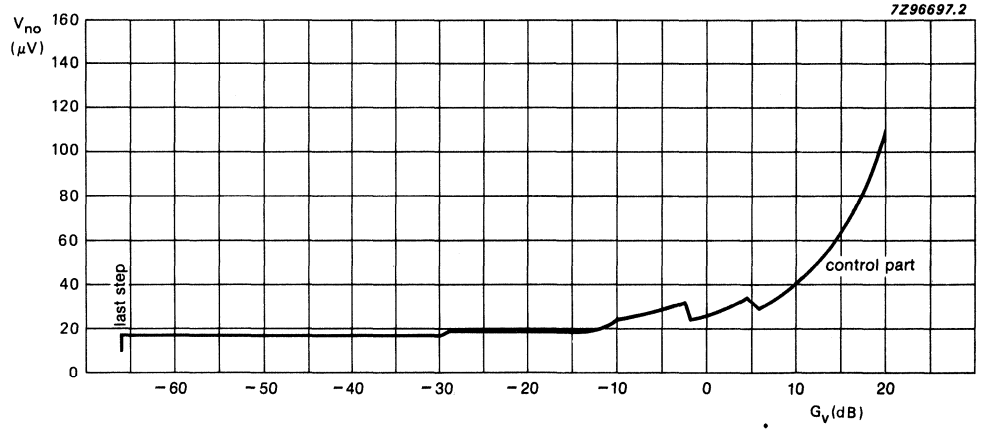


Fig. 7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

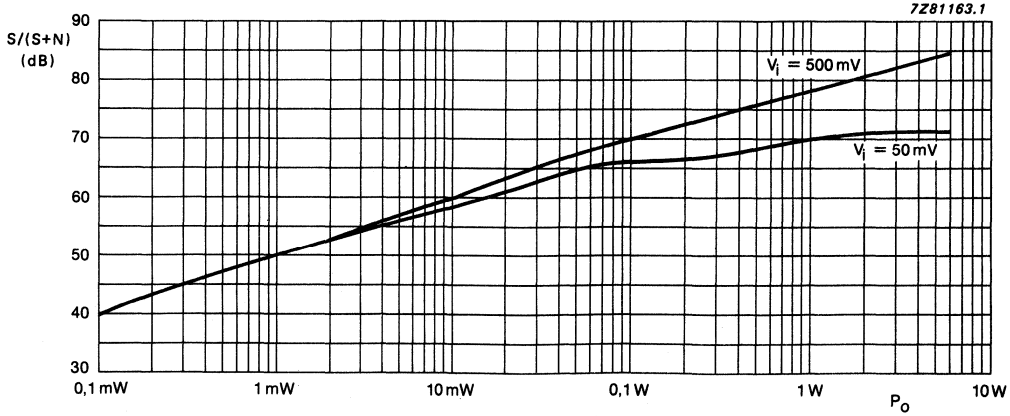


Fig. 8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig. 9).

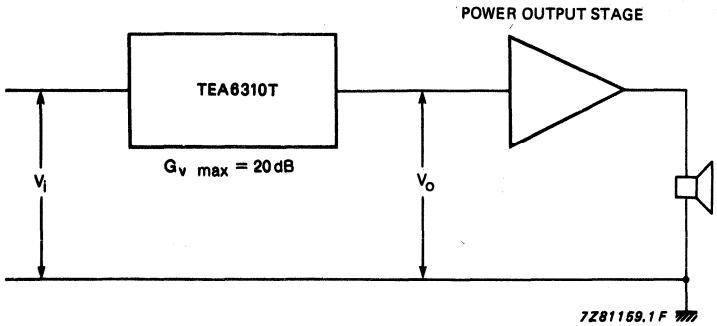


Fig. 9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

DEVELOPMENT DATA

APPLICATION INFORMATION

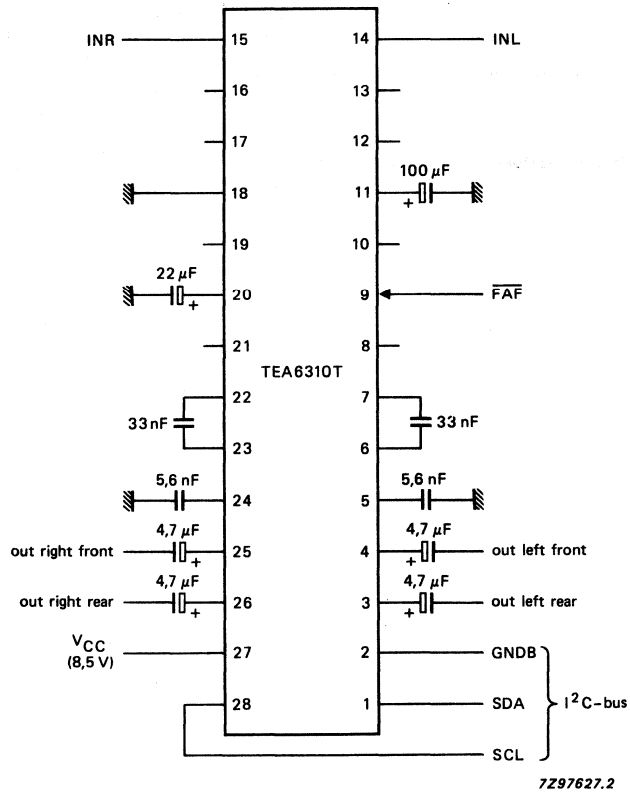
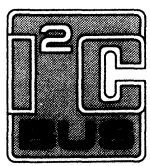


Fig. 10 Test and application circuit.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

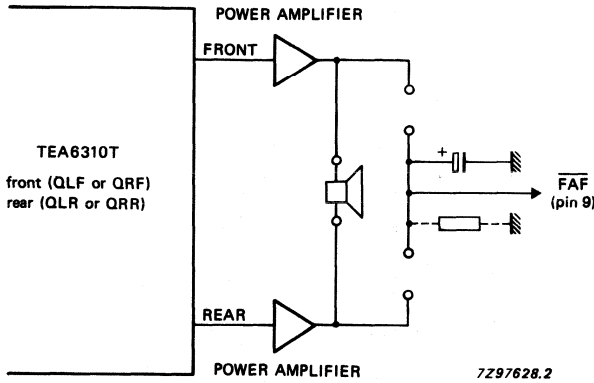


Fig. 11 Automatic FADER control; P_o = 24 W, $V_{g\text{-}18}$ = 0 V (FADER disabled).

DEVELOPMENT DATA

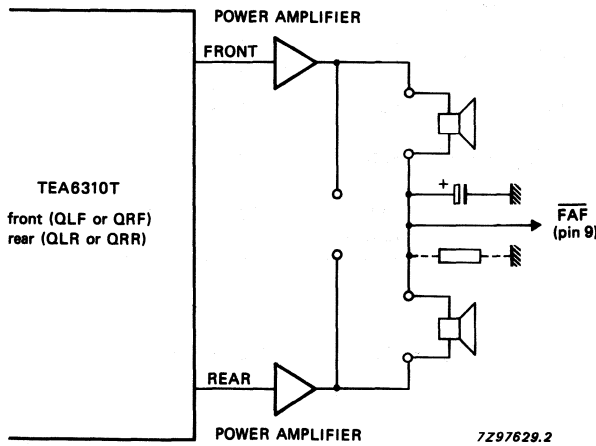


Fig. 12 Automatic FADER control; P_o = 2 x 6 W, $V_{g\text{-}18}$ = 7 V (FADER enabled).

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	June 1991

TEA6330T

Sound fader control circuit for carradios

FEATURES

- Stereo/hi-fi processor for carradios performed with volume, balance, bass and treble controls
- Sound fader control (front/rear) down to –30 dB in steps of 2 dB
- Fast muting via bus or via setting the muting pin
- Suitable for external audio equalizers, can be looped-in controlled by the I²C-bus
- Power-on reset on chip sets the device into general mute position
- AC and DC short circuit protected concerning neighbouring pins
- I²C-bus control for all functions.

GENERAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for carradios, in addition with fader function and the possibility of an external equalizer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current	-	26	-	mA
V_i	maximum AF input signal (RMS value)	2	-	-	V
V_o	maximum AF output signal (RMS value)	2	-	-	V
ΔG_v	volume control range, separated	–66	-	+20	dB
	fader control range, separated	0	-	–30	dB
	bass control range	–12	-	+15	dB
	treble control range	–12	-	+12	dB
THD	total harmonic distortion	-	-	0.2	%
S/N(W)	weighted signal-to-noise ratio	-	67	-	dB
α_{CR}	crosstalk attenuation	-	90	-	dB
B	frequency response (–1 dB)	-	35 to 20000	-	Hz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6330T	20	SO	plastic	SOT163A

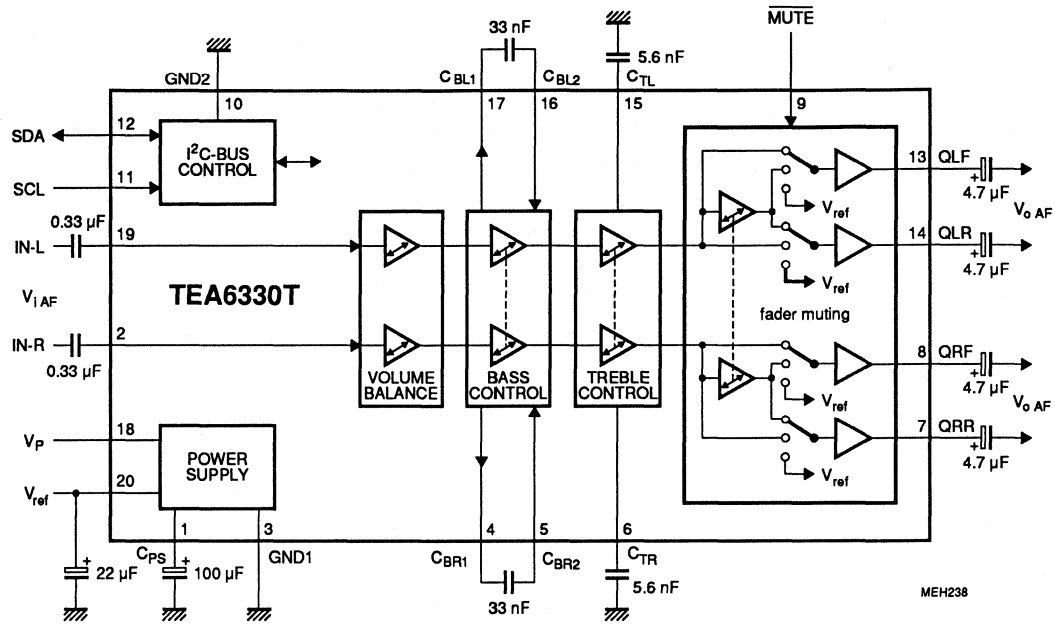


Fig.1 Block and test circuit.

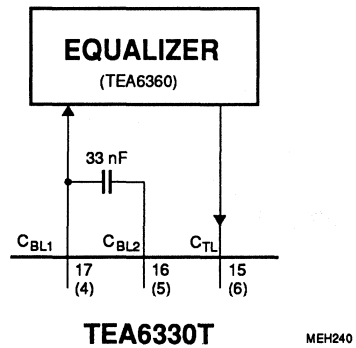


Fig.2 Connection of equalizer (Table 7). In application with equalizer circuit TEA6360 coupling capacitors are not necessary. Connectors for RIGHT in brackets.

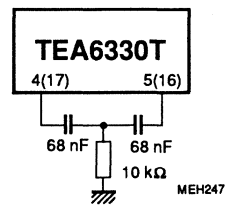


Fig.3 T-filter for enhanced bass control (Fig.5). Connectors for RIGHT in brackets.

Sound fader control circuit for carradios

TEA6330T

PINNING

SYMBOL	PIN	DESCRIPTION
C_{PS}	1	filtering capacitor for power supply
IN-R	2	audio input signal RIGHT
GND1	3	analog ground (0 V)
C_{BR1}	4	capacitor for bass control RIGHT and signal to equalizer
C_{BR2}	5	capacitor for bass control RIGHT
C_{TR}	6	capacitor for treble control RIGHT, input signal for equalizer RIGHT
QRR	7	right audio output signal of rear channel
QRF	8	right audio output signal of front channel
MUTE	9	input to set mute externally
GND2	10	digital ground (0 V) for bus control
SCL	11	clock signal of I²C-bus
SDA	12	data signal of I²C-bus
QLF	13	left audio output signal of front channel
QLR	14	left audio output signal of rear channel
C_{TL}	15	capacitor for treble control LEFT, input signal for equalizer LEFT
C_{BL2}	16	capacitor for bass control LEFT
C_{BL1}	17	capacitor for bass control LEFT and signal to equalizer
V_P	18	+8.5 V supply voltage
IN-L	19	audio input signal LEFT
V_{ref}	20	reference voltage output (V_P/2)

PIN CONFIGURATION

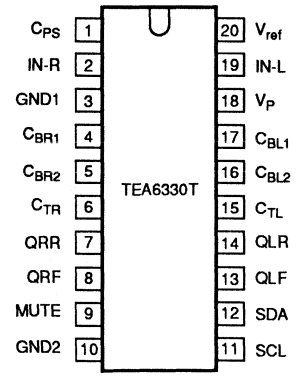


Fig.4 Pin configuration.

FUNCTION DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for carradios including fader function and the possibility of an external equalizer. The sound signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantages of this principle are the combination of low noise, low distortion and a high dynamic range. The separated volume controls of the left and the right channel make the balance control possible. The value and the characteristic of the balance is controlled via the I²C-bus.

The contour function is performed by setting an extra bass control and optional treble, depending on the actual volume position. Its switching points and its range are also controllable via the I²C-bus.
An interface is assigned behind the volume control to loop-in an equalizer (Fig.2). In this case the treble control is switched off, and the bass control can be used to set the contour.

Low level control fader is included independent of the volume controls, because the TEA6330T has four driver outputs (for front and rear).

An extra mute position for the front, the rear or for all channels is built in. The last function may be used for muting during preset selection.
No external interface is required between the microcomputer and this circuit, for all switching and controlling functions are controllable via the two-wire I²C-bus.

The separate mute-pin allows to switch the fader into mute position without using the I²C-bus.
The on chip power-on reset sets the TEA6330T into the general mute mode.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	0	10	V
P_{tot}	total power dissipation	0	700	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins	-	±200	V
	electrostatic handling** for all pins	-	±2000	V

CHARACTERISTICS

V_P = 8.5 V; load resistors at audio outputs 10 kΩ, f_i = 1 kHz (R_S = 600 Ω), bass and treble in linear position, fader in off position and T_{amb} = 25 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		7	8.5	10	V
I_P	supply current		-	26	-	mA
V_{ref}	reference voltage (pin 20)		0.45 V_P	0.5 V_P	0.55 V_P	V
V_O	DC voltage at output (pins 7, 8, 13, 14)		-	0.5 V_P	-	V
Measurements over all						
V_i	maximum AF input level for THD = 2 % at pins 2 and 19 (RMS value)	G_v = –66 to –6 dB and V_P = 8.1 V	2	-	-	V
V_o	maximum AF output level for THD = 2 % at pins 7, 8, 13, 14 (RMS value)	G_v = –4 to +20 dB and V_P = 8.1 V	1.1	-	-	V
G_v	maximum gain by volume setting		19	20	21	dB
B	frequency response	–1 dB roll-off frequency	-	35 to 20000	-	Hz
α_{CR}	crosstalk attenuation	f = 250 to 10000 Hz G_v = 0 dB	70	90	-	dB
THD	total harmonic distortion	f = 20 to 12500 Hz				
	$V_{i\,(rms)}$ = 50 mV	G_v = +20 dB	-	0.1	0.3	%
	$V_{i\,(rms)}$ = 500 mV	G_v = 0 dB	-	0.05	0.2	%
	$V_{i\,(rms)}$ = 1.6 V	G_v = –10 dB	-	0.2	0.5	%
RR	ripple rejection for V_R < 200 mV rms	G_v = 0 dB				
		f = 100 Hz	-	70	-	dB
		f = 40 to 3000 Hz	-	60	-	dB
		f = 3 to 12.5 kHz	-	50	-	dB

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_N	noise power at output of a 25 W power stage with 26 dB gain (only contribution of TEA6330T)	mute position (V_9 = 0)	-	-	10	nW
α_{BUS}	crosstalk attenuation between SDA, SCL and signal output (20 log V_{BUS} (p-p)/ V_o rms)	G_V = 0 dB	-	110	-	dB
S/N(W)	weighted signal-to-noise ratio for	CCIR 468-2 quasi peak				
	V_i = 50 mV rms	P_o = 50 mW	-	65	-	dB
	V_i = 500 mV rms	P_o = 50 mW	-	67	-	dB
	V_i = 50 mV rms	P_o = 1 W	65	72	-	dB
	V_i = 500 mV rms	P_o = 1 W	65	78	-	dB
	V_i = 50 mV rms	P_o = 6 W; Fig.9	-	72	-	dB
	V_i = 500 mV rms	P_o = 6 W; Fig.9	-	86	-	dB
Audio frequency outputs QLF, QRF, QLR and QRR						
V_o	maximum output signal (RMS value)		1.1	-	-	V
R_o	output resistance (pins 7, 8, 13 and 14)		-	100	150	Ω
R_L	admissible output load resistor		7.5	-	-	kΩ
C_L	admissible output load capacitor		-	-	2.5	nF
$V_{N(W)}$	weighted noise voltage at output	CCIR 468-2 ; Fig.8				
	for maximim gain	G_V = +20 dB	-	110	220	μV
	for 0 dB gain	G_V = 0 dB	-	25	50	μV
	for minimum gain	G_V = –66 dB	-	19	38	μV
	for mute position	(V_9 = 0)	-	11	22	μV
Volume control		R_G = 600 Ω				
R_I	input resistance (pins 2 and 19)		35	50	65	kΩ
G_V	volume control range	Table 2	–66	-	+20	dB
ΔG_V	step width		-	2	-	dB
	gain set error	G_V = –50 to +20 dB	-	-	2	dB
		G_V = –66 to –50 dB	-	-	3	dB
	gain tracking error	balance in mid position	-	-	2	dB
α_{mute}	mute attenuation at volume mute	set mute-bits	76	90	-	dB
Bass control						
G_V	controllable bass range	Table 3				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum boost	f = 100 Hz	12	13	14	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
	maximum attenuation	f = 100 Hz	10	11	12	dB
ΔG_V	step width	f = 40 Hz	2.5	3	3.5	dB

Sound fader control circuit for carradios

TEA6330T

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble control						
G_V	controllable treble range	Table 4; Fig.7				
	maximum boost	f = 10 kHz	9	10	11	dB
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	-	-	15	dB
	maximum attenuation	f = 10 kHz	9	10	11	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_V	step width	f = 15 kHz	2.5	3	3.5	dB
Fader control						
G_V	fader control range	Table 5	-	0 to −30	-	dB
	step width		1.5	2	2.5	dB
α_{MUTE}	mute attenuation	GMB-bit = 1; Table 6	74	84	-	dB
ΔV_o	DC offset output voltage (pins 7, 8, 13, 14)					
	between any adjoining step and any step to mute	G_V = −66 to 0 dB	-	0.2	10	mV
		G_V = 0 to +20 dB	-	2	15	mV
	in any treble and fader position	G_V = −66 to 0 dB	-	-	10	mV
	in any bass position	G_V = −66 to 0 dB	-	-	10	mV
External mute (pin 9)						
V_9	input voltage for MUTE-ON (LOW)	fader is switched into general mute position	0		1.5	V
	input voltage for MUTE-OFF (HIGH)	Tables 2 and 5	3		V_P	V
	input voltage for MUTE-OFF	pin 9 open-circuit	-	5	-	V
I_9	input current		-	-	±10	μA
I²C-bus, SCL and SDA (pins 11 and 12)						
$V_{11, 12}$	input voltage HIGH-level		3	-	V_P	V
	input voltage LOW-level		0	-	1.5	V
$I_{11, 12}$	input current		-	-	±10	μA
V_{ACK}	output voltage at acknowledge (pin 12)	I_{12} = −3 mA	-	-	0.4	V
Power-on reset, when reset is active the GMU-bit (general mute) is set and the bus receiver is in reset position						
V_P	supply voltage for start of reset	increasing voltage	-	-	2.5	V
	supply voltage for end of reset	increasing voltage	5.2	6.0	6.8	V
	supply voltage for start of reset	decreasing voltage	4.2	5.0	5.8	V

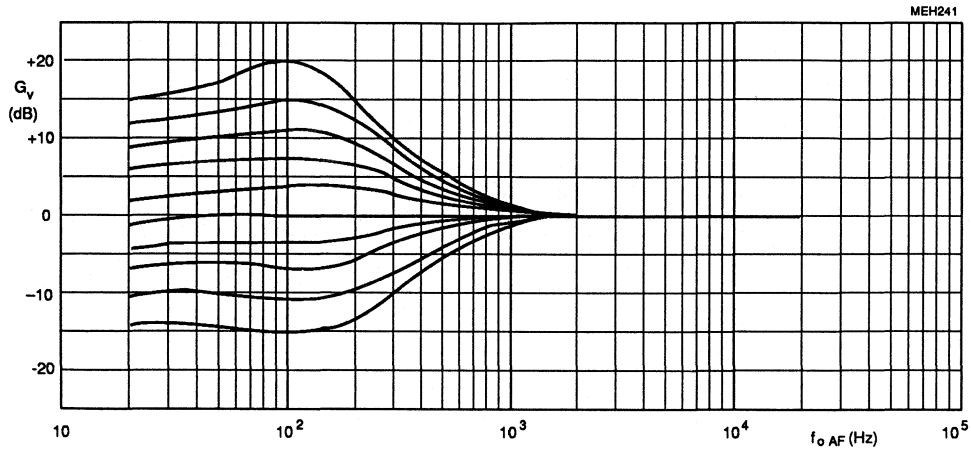


Fig.5 Bass control with enhanced control range (T-filter coupling, Fig.1).

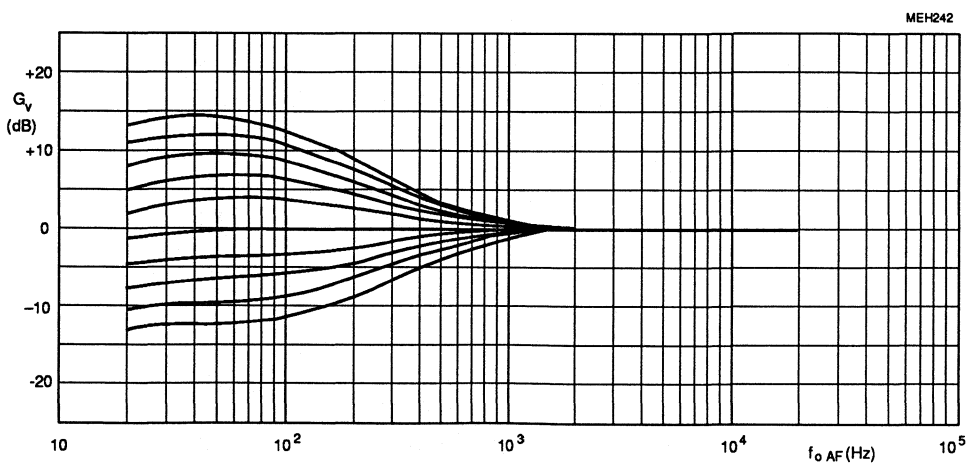


Fig.6 Bass control with normal control range (Fig.1).

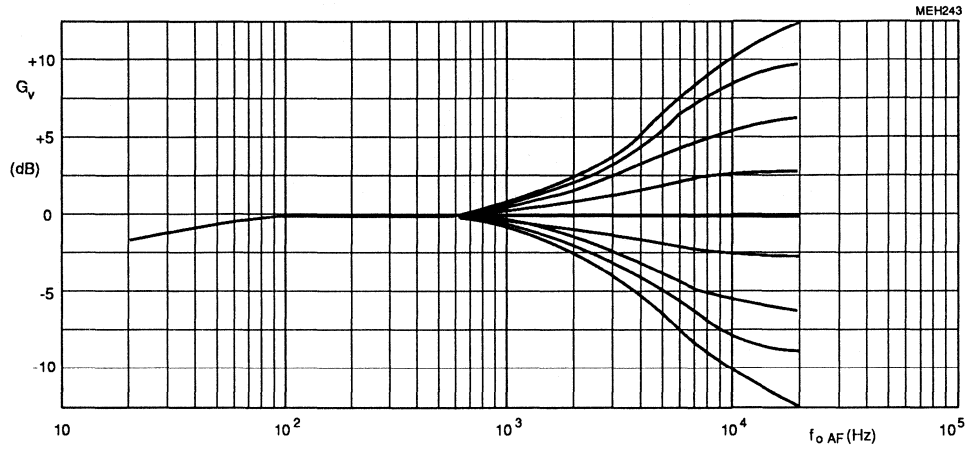


Fig.7 Treble control.

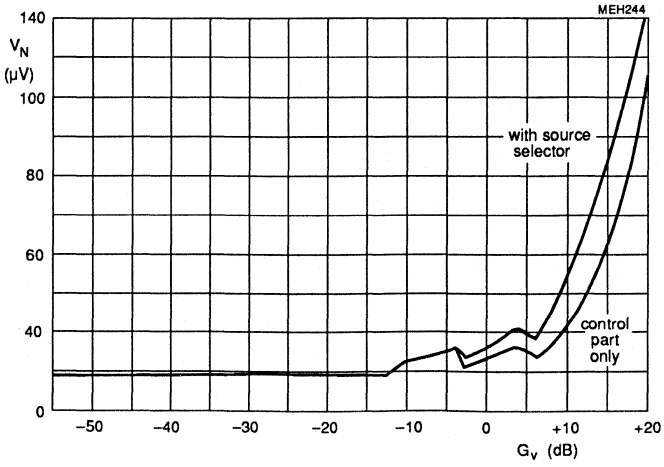


Fig.8 Noise voltage on outputs (CCIR 468-2 weighted, quasi-peak).

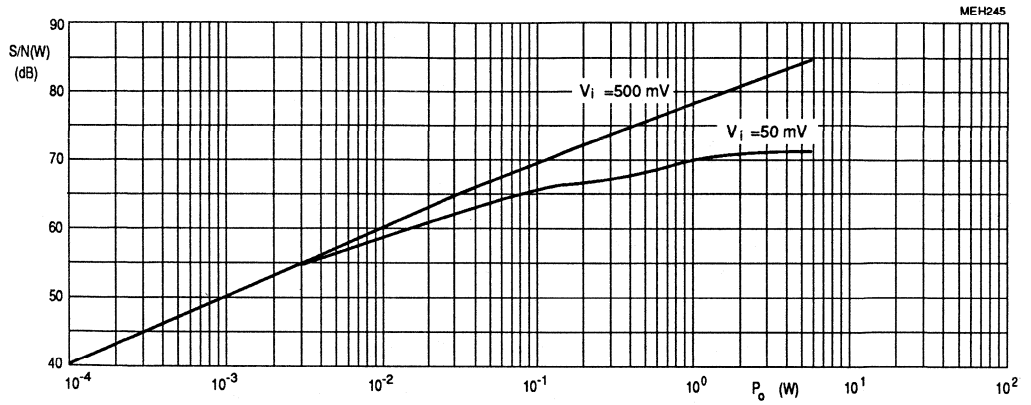


Fig.9 Signal-to-noise ratio (CCIR 468-2 weighted, quasi-peak) for TEA6330T with a 6 W power amplifier (20 dB gain, Fig.10). Measurements without noise contribution of the power amplifier.

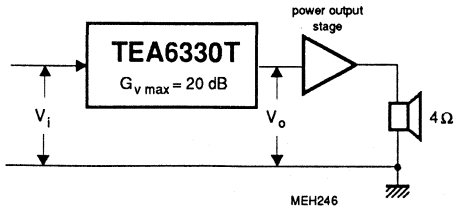


Fig.10 Signal-to-noise ratio measurement (Fig.9) with V_i = 50 mV rms, V_o = 500 mV rms for P_{max} = 6 W.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 000X**
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, Table 1
DATA = data byte, Table 1
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission

function	subaddress byte								data byte D7	D6	D5	D4	D3	D2	D1	D0
volume left	0	0	0	0	0	0	0	0	0	0	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0	0	0	0	0	0	0	1	0	0	VR5	VR4	VR3	VR2	VR1	VR0
bass	0	0	0	0	0	0	1	0	0	0	0	0	BA3	BA2	BA1	BA0
treble	0	0	0	0	0	0	1	1	0	0	0	0	TR3	TR2	TR1	TR0
fader	0	0	0	0	0	1	0	0	0	0	MFN	FCH	FA3	FA2	FA1	FA0
audio switch	0	0	0	0	0	1	0	1	GMU	EQN	0	0	0	0	0	0

Function of the bits:

VL0 to VL5 volume control of left channel (balance control)
VR0 to VR5 volume control of right channel (balance control)
BA0 to BA3 bass control of both channels
TR0 to TR3 treble control of both channels
FA0 to FA3 fader control front to rear

FCH select fader channels front or rear
MFN mute control of the selected channels front or rear
GMU mute control, general mute
EQN equalizer switchover (0 = equalizer-on)

Table 2(a) Volume setting LEFT

G_v dB	DATA VL5	VL4	VL3	VL2	VL1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
−2	1	1	0	1	0	0
−4	1	1	0	0	1	1
−6	1	1	0	0	1	0
−8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
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mute left	0	0	0	0	0	0

Table 2(b) Volume setting RIGHT

G_v dB	DATA VR5	VR4	VR3	VR2	VR1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
−2	1	1	0	1	0	0
−4	1	1	0	0	1	1
−6	1	1	0	0	1	0
−8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
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mute right	0	0	0	0	0	0

Table 3(a) Bass setting with equalizer passive (EQN = 1)

G_v dB	DATA D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 3(b) Bass setting with equalizer active (EQN = 0)

G_v dB	DATA D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 4(a) Treble setting with equalizer passive (EQN = 1)

G_v dB	DATA D3	D2	D1	D0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 4(b) Treble setting with equalizer active (EQN = 0)

G_v dB	DATA D3	D2	D1	D0
0	1	1	1	1
0	1	1	1	0
0	1	1	0	1
0	1	1	0	0
0	1	0	1	1
0	1	0	1	0
0	1	0	0	1
0	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 5(a) Fader function front

setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
–2	0	1	1	1	1	1	0
–4	0	1	1	1	1	0	1
–6	0	1	1	1	1	0	0
–8	0	1	1	1	0	1	1
–10	0	1	1	1	0	1	0
–12	0	1	1	1	0	0	1
–14	0	1	1	1	0	0	0
–16	0	1	1	0	1	1	1
–18	0	1	1	0	1	1	0
–20	0	1	1	0	1	0	1
–22	0	1	1	0	1	0	0
–24	0	1	1	0	0	1	1
–26	0	1	1	0	0	1	0
–28	0	1	1	0	0	0	1
–30	0	1	1	0	0	0	0
		mute front					
–84	0	0	1	1	1	1	0
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–84	0	0	1	0	0	0	0

Table 5(b) Fader function rear

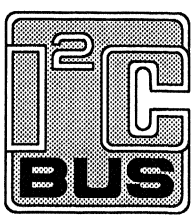
setting front dB	setting rear dB	DATA MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	–2	1	0	1	1	1	0
0	–4	1	0	1	1	0	1
0	–6	1	0	1	1	0	0
0	–8	1	0	1	0	1	1
0	–10	1	0	1	0	1	0
0	–12	1	0	1	0	0	1
0	–14	1	0	1	0	0	0
0	–16	1	0	0	1	1	1
0	–18	1	0	0	1	1	0
0	–20	1	0	0	1	0	1
0	–22	1	0	0	1	0	0
0	–24	1	0	0	0	1	1
0	–26	1	0	0	0	1	0
0	–28	1	0	0	0	0	1
0	–30	1	0	0	0	0	0
		mute rear					
0	–84	0	0	1	1	1	0
	---			---			---
	---			---			---
	---			---			---
0	–84	0	0	0	0	0	0

Table 6 Mute control

MUTE control	DATA GMU-bit	remarks
active	1	outputs QLF, QLR, QRF and QRR are muted
passive	0	no general mute

Table 7 Equalizer

equalizer control	DATA EQN-bit	remarks
active	0	signal outputs for equalizer are pins 4 and 17, inputs are pins 6 and 15; Tables 3(b) and 4(b)
passive	1	no general mute; Tables 3(a) and 4(a)



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1991

TEA6360
5-band stereo equalizer circuit

FEATURES

- Monolithic integrated 5-band stereo equalizer circuit
- Five filters for each channel
- Centre frequency, bandwidth and maximum boost/cut defined by external components
- Choise for variable or constant Q-factor via I²C software
- Defeat mode
- All stages are DC-coupled
- I²C-bus control for all functions
- Two different modul addresses programmable

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 14)	7	8.5	13.2	V
I_P	supply current	-	24.5	-	mA
$V_{1,32}$	input voltage range	-	2.1 to V_{P-1}	-	V
V_o	maximum output signal level (RMS value, pins 13 and 20)	- 1.1		-	V
G_v	total signal gain, all filters linear	–0.5	-	0	dB
B	-1 dB frequency response (linear)	0 to 20	-	-	kHz
T_{amb}	operating ambient temperature	–40	-	85	°C

GENERAL DESCRIPTION

The 5-band stereo equalizer is an I²C-bus controlled tone processor for application in car radio sets, TV sets and music centres. It offers the possibility of sound control as well as equalization of sound pressure behaviour of different rooms or loudspeakers, especially in cars.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6360	32	shrink DIL	plastic	SOT232
TEA6360/T	32	mini-pack	plastic	SOT287

5-band stereo equalizer circuit

TEA6360

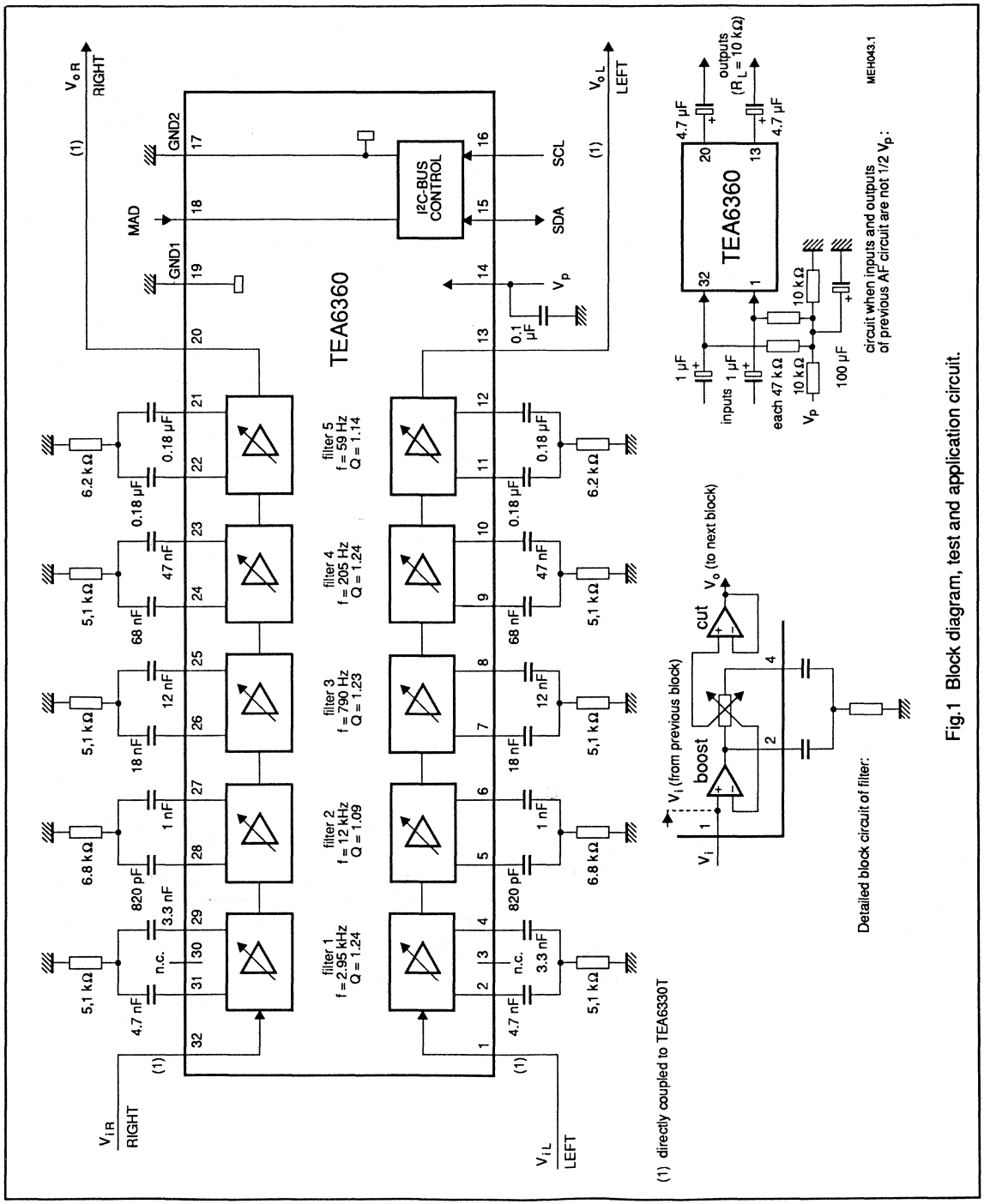


Fig.1 Block diagram, test and application circuit.

5-band stereo equalizer circuit TEA6360

PINNING

SYMBOL	PIN	DESCRIPTION
V_{iL}	1	audio frequency input LEFT
F1LA	2	connection A for filter 1 LEFT (f = 2.95 kHz)
n.c.	3	not connected
F1LB	4	connection B for filter 1 LEFT(f = 2.95 kHz)
F2LA	5	connection A for filter 2 LEFT (f = 12 kHz)
F2LB	6	connection B for filter 2 LEFT (f = 12 kHz)
F3LA	7	connection A for filter 3 LEFT (f = 790 Hz)
F3LB	8	connection B for filter 3 LEFT (f = 790 Hz)
F4LA	9	connection A for filter 4 LEFT (f = 205 Hz)
F4LB	10	connection B for filter 4 LEFT (f = 205 Hz)
F5LA	11	connection A for filter 5 LEFT (f = 59 Hz)
F5LB	12	connection B for filter 5 LEFT (f = 59 Hz)
V_{oL}	13	audio frequency output LEFT
V_P	14	supply voltage (+8.5 V)
SDA	15	I^2C-bus data line
SCL	16	I^2C-bus clock line
GND2	17	ground 2 (I^2C-bus ground)
MAD	18	modul address
GND1	19	ground 1 (analog ground)
V_{oR}	20	audio frequency output RIGHT
F5RB	21	connection B for filter 5 RIGHT (f = 59 Hz)
F5RA	22	connection A for filter 5 RIGHT (f = 59 Hz)
F4RB	23	connection B for filter 4 RIGHT (f = 205 Hz)
F4RA	24	connection A for filter 4 RIGHT (f = 205 Hz)
F3RB	25	connection B for filter 3 RIGHT (f = 790 Hz)
F3RA	26	connection A for filter 3 RIGHT (f = 790 Hz)
F2RB	27	connection B for filter 2 RIGHT (f = 12 kHz)
F2RA	28	connection A for filter 2 RIGHT (f = 12 kHz)
F1RB	29	connection B for filter 1 RIGHT (f = 2.95 kHz)
n.c.	30	not connected
F1RA	31	connection A for filter 1 RIGHT (f = 2.95 kHz)
V_{iR}	32	audio frequency input RIGHT

PIN CONFIGURATION

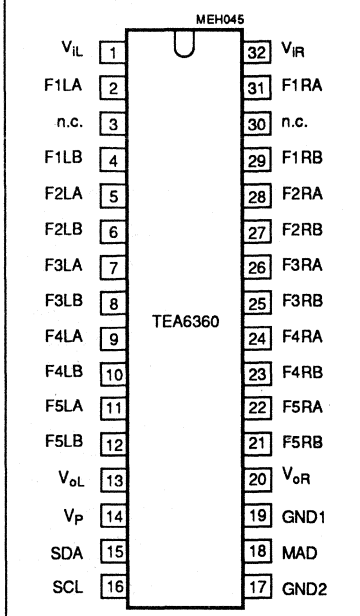


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TEA6360 is performed with two stereo channels (RIGHT and LEFT), each one consists of five equal filter amplifiers (Fig.1).

The centre frequencies for the different filters as well as the bandwidth and the control ranges for boost and cut depend on the external components. Each filter can have different external components but for one definite pair of filters the centre frequency as well as the control range for boost and cut are the same. That means, they have symmetrical curves for boost and cut.

The control range (maximum value in dB) is divided into five steps and one extra step for the linear position.

At maximum gain of 12 dB the typical step resolution is 2.4 dB. The internal resistor chain of each filter amplifier is optimized for 12 dB maximum gain. Therefore the typical gain factors for 15 dB application are as follows:

step 1 = 2.7 dB
step 2 = 5.5 dB
step 3 = 8.4 dB
step 4 = 11.6 dB
step 5 = 15.0 dB

The control of the different filters is obtained by selecting the appropriate subaddress byte (Tab.1). The position of the filter in the left channel and that in the right channel is always the same (stereo). The position of the boost part and the cut part is independently controllable (Tables 2 and 3).

The quality factor of the filter has its maximum in the maximum position (steps 5), if boost (cut on step 0) or cut (boost on step 0) is used. The quality factor decreases also with the step number (variable quality factor). In this mode the control pattern are according to Table 4.

A different control is necessary to achieve a constant quality factor over the whole control range. For boost with a constant quality factor over the boost range position +5 is selected and boost control is then performed using cut. This control technique is applied to the cut range with position –5 selected and the boost is varied (Table 5).

The cut part has to follow the boost part in each filter for economic reasons. So the signal is first amplified and then attenuated. This has to be taken into account for the internal level diagram in case of constant quality factor. This may result in a mode between constant Q and non-constant Q mode; for example for the position +2 it is not necessary to amplify by step +5 and then attenuate by –3 step. The combination of step +4 and step –2 to reach position +2 is a good result (quasi constant quality factor, Table 6).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 19, 28 and 43 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)	0	13.2	V
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–40	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins		±500	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_P = 8.5 V; f_i = 1 kHz (R_S = 600 Ω), R_L = 10 kΩ, T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 14)		7	8.5	13.2	V
I_P	supply current (pin 14)	V_P = 8.5 V	-	25.5	-	mA
		V_P = 12 V	-	26.0	-	mA
Analog part						
R_i	input resistor (pins 1 and 32)		1	-	-	MΩ
$V_{1,32}$	input voltage range at any stage		2.1 to V_P–1	-	-	V
$V_{13,20}$	output voltage range at any stage		1.0 to V_P–1	-	-	V
V_o	output signal level (RMS value, pins 13 and 20)	control range 0 to +5, variable Q-factor or quasi constant Q-factor	1.1	-	-	V
R_o	output resistor (pins 13 and 20)		-	100	-	Ω
R_L	admissable load resistance at outputs (pins 13 and 20)		2	-	-	kΩ
C_L	admissable load capacitance at outputs (pins 13 and 20)		-	-	2.5	nF
G_v	total signal gain ($G = V_o / V_i$)	all filters linear	–0.5	-	0	dB
B	frequency response	all filters linear, roll off frequency for –1 dB				
	minimum value	(DC-coupled)	0	-	-	Hz
	maximum value		20	-	-	kHz
α_{Cr}	crosstalk attenuation between channels	f = 250 to 10000 Hz				
	all filters linear		60	75	-	dB
	all filters maximum boost		55	-	-	dB
	all filters maximum cut		55	-	-	dB
THD	distortion (pins 13 and 20)	f = 20 to 12500 Hz V_P = 8.5 to 12 V				
	$V_{o\ (rms)}$ = 1.1 V	all filters linear	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 0.1 V	all filters linear	-	0.05	0.2	%
	$V_{o\ (rms)}$ = 1.1 V	all filters max. boost	-	0.5	1.0	%
	$V_{o\ (rms)}$ = 0.1 V	all filters max. boost	-	0.1	0.3	%
	$V_{o\ (rms)}$ = 0.1 V	all filters maximum cut	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 1 V	all filters max. boost f = 1 kHz	-	-	0.35	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_N	weighted output noise voltage (RMS value)	CCIR 468-3, maximum gain/filter of 12 dB				
	defeat mode		-	8	16	μV
	all filters linear		-	23	46	μV
	all filters maximum boost		-	70	140	μV
	all filters maximum cut		-	23	46	μV
α_{Cr}	crosstalk between bus inputs and signal outputs, 20 log (V_{bus} (p-p) / V_o rms)	all filters linear	-	120	-	dB
RR	ripple rejection at V_{ripple} rms < 200 mV	all filters linear				
	for f = 100 Hz		-	70	-	dB
	for f = 40 to 12500 Hz		-	60	-	dB
Internal filters of analog part						
Q	Q-factor dependent on maximum gain					
	maximum gain 10 dB		0.1	-	1.2	
	maximum gain 12 dB		0.1	-	1.4	
	maximum gain 15 dB		0.1	-	1.8	
R_{tot}	total resistor of different filter sections		29.6	37.0	44.4	kΩ
ΔR_{tot}	tolerance between any filter section		-	-	±4	%
Internal controls of analog part via I²C-bus						
Step	number of steps for boost or for cut		-	5	-	
	position for linear		-	1	-	
	step resolution	maximum gain 12 dB	-	2.4	-	dB
	step set error		-	0.5	-	dB
ΔV_o	DC offset between any step or neighbouring step or defeat		-	-	±10	mV
I²C-bus control SDA and SCL (pins 15 and 16)						
V_{IH}	input level HIGH		3	-	V_P	V
V_{IL}	input level LOW		0	-	1.5	V
I_I	input current		-	-	±10	μA
V_{ACK}	acknowledge voltage on SDA	I_{15} = 3 mA at LOW	-	-	0.4	V
Module address bit (pin 18)						
V_{IH}	input level HIGH for address 1000 0110		3	-	V_P	V
V_{IL}	input level LOW for address 1000 0100		0	-	1.5	V
I_I	input current		-	-	±10	μA
Power on reset: When reset is active the DEF-bit (defeat) is set and the I²C-bus receiver is in reset position.						
RESET	start of reset	increasing V_P	-	-	2.5	V
		decreasing V_P	4.2	5.0	5.8	V
	end of reset	increasing V_P	5.2	6.0	6.8	V

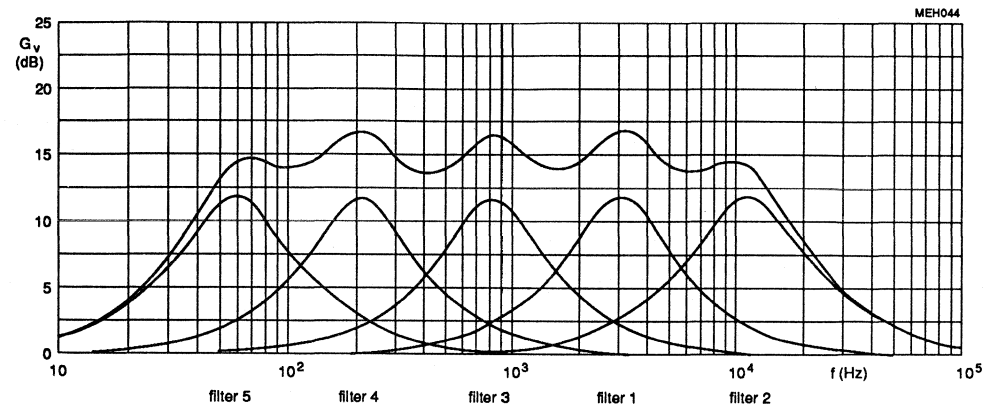


Fig.3 Frequency response for maximum boost of +12 dB according to Fig.1. For maximum cut the curves are symmetrical to negative gain values.

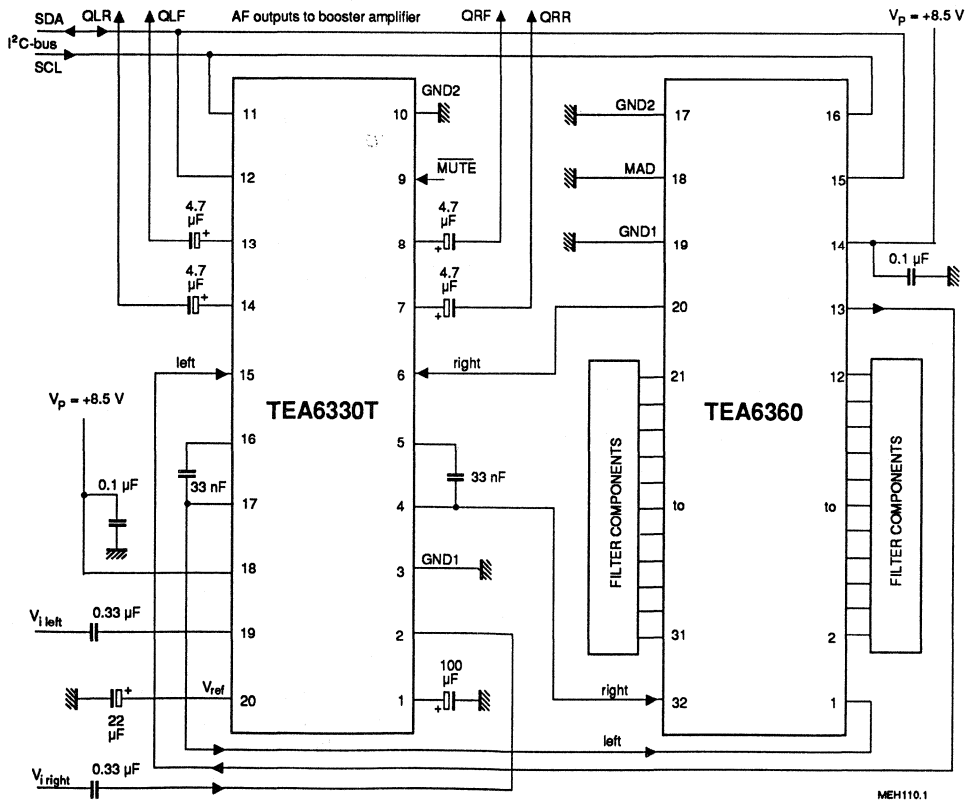


Fig.4 Application for car radio (V_P <8.5 V).

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 0100** when pin 18 is set LOW
or **1000 0110** when pin 18 is set HIGH or open-circuit
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission.

function	subaddress byte								data byte D7	D6	D5	D4	D3	D2	D1	D0
filter 1 /defeat	0	0	0	0	0	0	0	0	DEF	1B2	1B1	1B0	0	1C2	1C1	1C0
filter 2	0	0	0	0	0	0	0	1	0	2B2	2B1	2B0	0	2C2	2C1	2C0
filter 3	0	0	0	0	0	0	1	0	0	3B2	3B1	3B0	0	3C2	3C1	3C0
filter 4	0	0	0	0	0	0	1	1	0	4B2	4B1	4B0	0	4C2	4C1	4C0
filter 5	0	0	0	0	0	1	0	0	0	5B2	5B1	5B0	0	5C2	5C1	5C0

Function of the bits of Table 1:

1B0 to 1B2 boost control for filter 1
1B0 to 1B2 cut control for filter 1
2B0 to 2B2 boost control for filter 2
2B0 to 2B2 cut control for filter 2
3B0 to 3B2 boost control for filter 3
3B0 to 3B2 cut control for filter 3
4B0 to 4B2 boost control for filter 4
4B0 to 4B2 cut control for filter 4
5B0 to 5B2 boost control for filter 5
5B0 to 5B2 cut control for filter 5

DEF
DEF = 0 (defeat bit): All filters operating.
DEF = 1 : Linear frequency response, input is directly connected to the output of the output amplifier. The filter settings are stored but the internal amplification is controlled to 0 dB, independent on bits nB2 to nB0.

Table 2 Boost control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no boost)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum boost)	1	0	1
step 5	(maximum boost)	1	1	0
step 5	(maximum boost)	1	1	1

Table 3 Cut control for filter n

DATA				
position		nB2	nB1	nB0
step 0	(no cut)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum cut)	1	0	1
step 5	(maximum cut)	1	1	0
step 5	(maximum cut)	1	1	1

Table 4 Filter control with variable quality factor

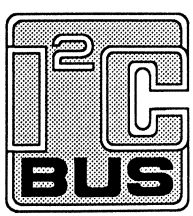
position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	0	0	0	0	0	(+4) + (−0) = +4
+3	0	0	1	1	0	0	0	0	(+3) + (−0) = +3
+2	0	0	1	0	0	0	0	0	(+2) + (−0) = +2
+1	0	0	0	1	0	0	0	0	(+1) + (−0) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	0	0	0	0	0	1	(+0) + (−1) = −1
−2	0	0	0	0	0	0	1	0	(+0) + (−2) = −2
−3	0	0	0	0	0	0	1	1	(+0) + (−3) = −3
−4	0	0	0	0	0	1	0	0	(+0) + (−4) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 5 Filter control with constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	1	0	0	1	1	(+5) + (−3) = +2
+1	0	1	0	1	0	1	0	0	(+5) + (−4) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	1	0	0	0	1	0	1	(+4) + (−5) = −1
−2	0	0	1	1	0	1	0	1	(+3) + (−5) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 6 Filter control with quasi-constant quality factor

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nC1	D0 nC0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	0	0	0	1	0	(+4) + (−2) = +2
+1	0	0	1	1	0	0	1	0	(+3) + (−2) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	1	0	0	0	1	1	(+2) + (−3) = −1
−2	0	0	1	0	0	1	0	0	(+2) + (−4) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5



RADIO TUNING PLL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I²C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3-4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16-4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

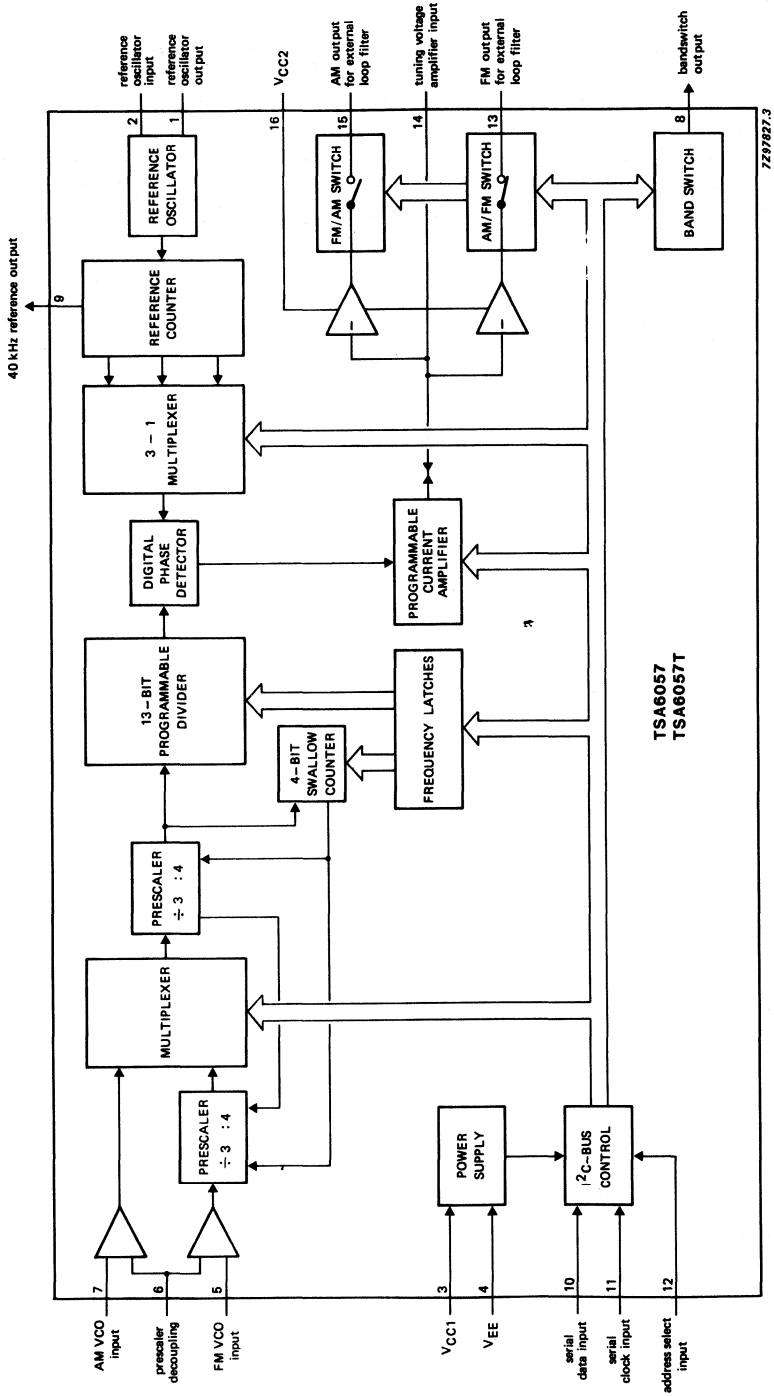


Fig.1 Block diagram.

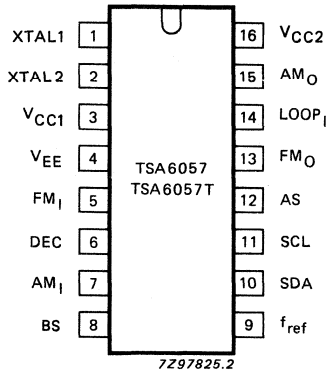


Fig.2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output
2	XTAL2	reference oscillator input
3	V_{CC1}	positive supply voltage
4	V_{EE}	ground
5	FM_I	FM VCO input
6	DEC	prescaler decoupling
7	AM_I	AM VCO input
8	BS	bandswitch output
9	f_{ref}	40 kHz reference output
10	SDA	serial data input (I²C-bus)
11	SCL	serial clock input (I²C-bus)
12	AS	address select input (I²C-bus)
13	FM_O	FM output for external loop filter
14	$LOOP_I$	tuning voltage amplifier input
15	AM_O	AM output for external loop filter
16	V_{CC2}	positive supply voltage

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I²C-bus interface with data latches and control logic. The I²C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I²C-bus specification is available on request.
- A software-controlled bandswitch output.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I²C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I²C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM_I (pin 7) or FM_I (pin 5). If the system is in lock the following is valid:

FM/$\overline{AM}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM_I
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM_I

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

(d) The bit $\overline{FM}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{FM}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . 0. It is also used for test purposes.

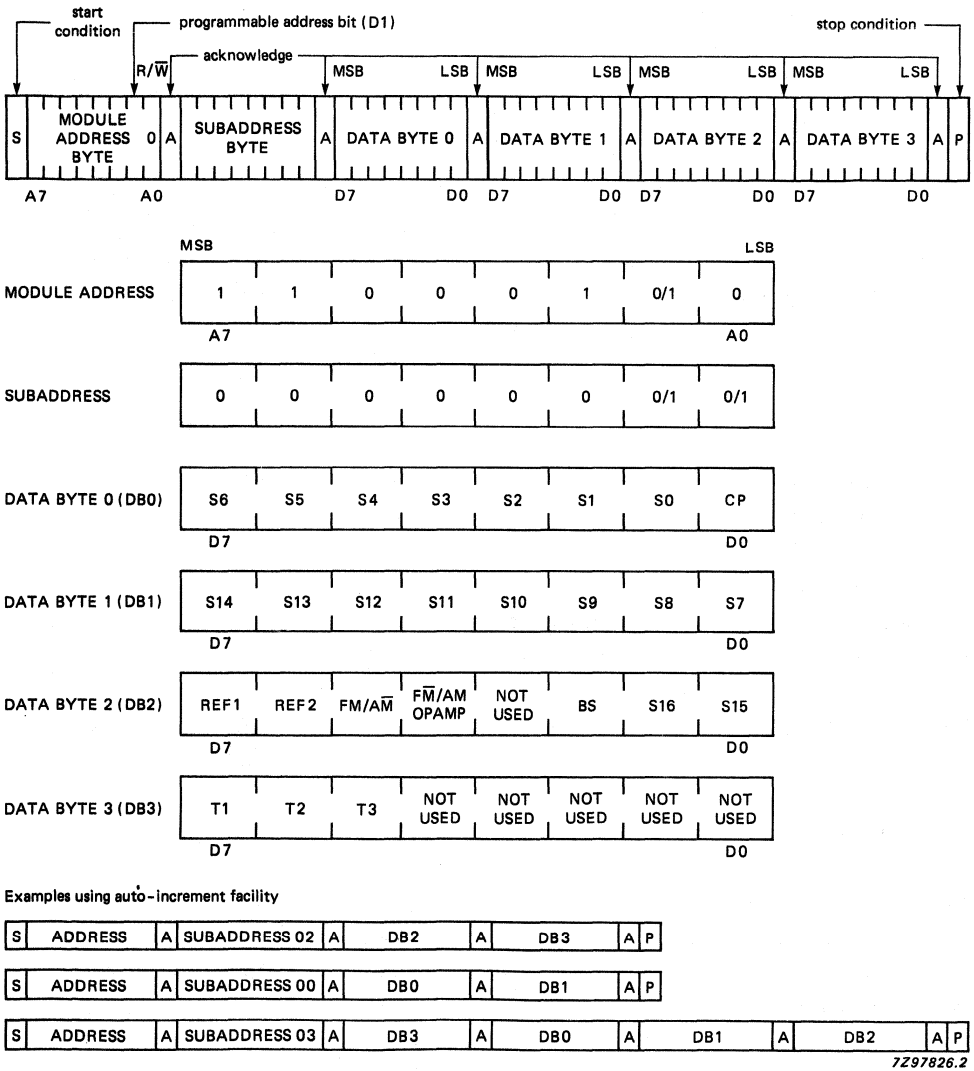


Fig.3 Bit organization.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3-4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16-4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I²C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	I_{OL} = 3.0 mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	V_{iFM} = 0 V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	μA
bit CP = logic 1		I_{chp}	400	500	600	μA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	μA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 μA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

DEVELOPMENT DATA

SENSITIVITY MEASUREMENT

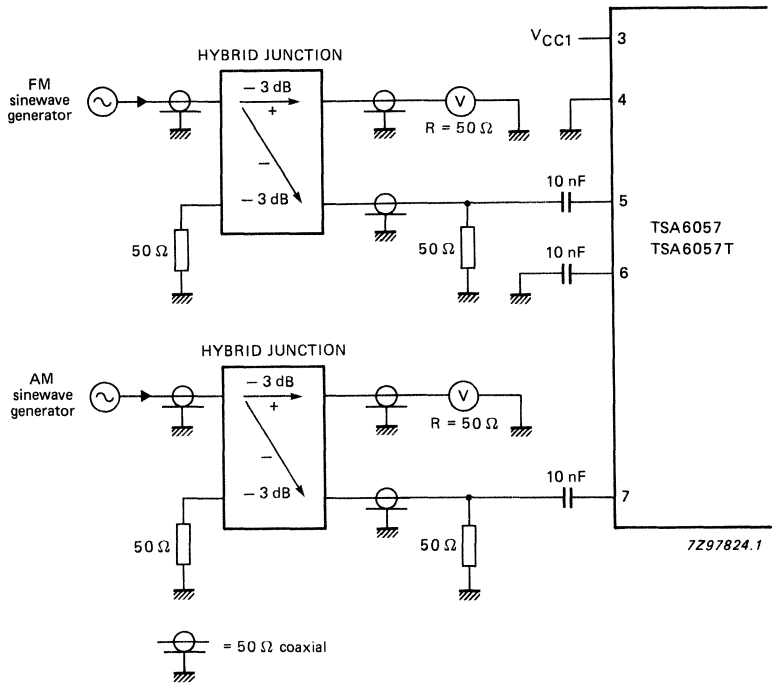


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

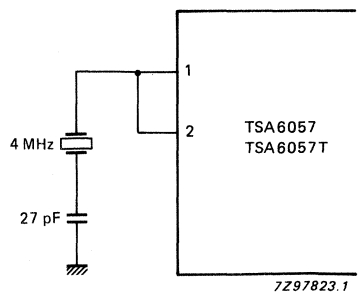


Fig.5 Crystal connection (4 MHz).

DEVELOPMENT DATA

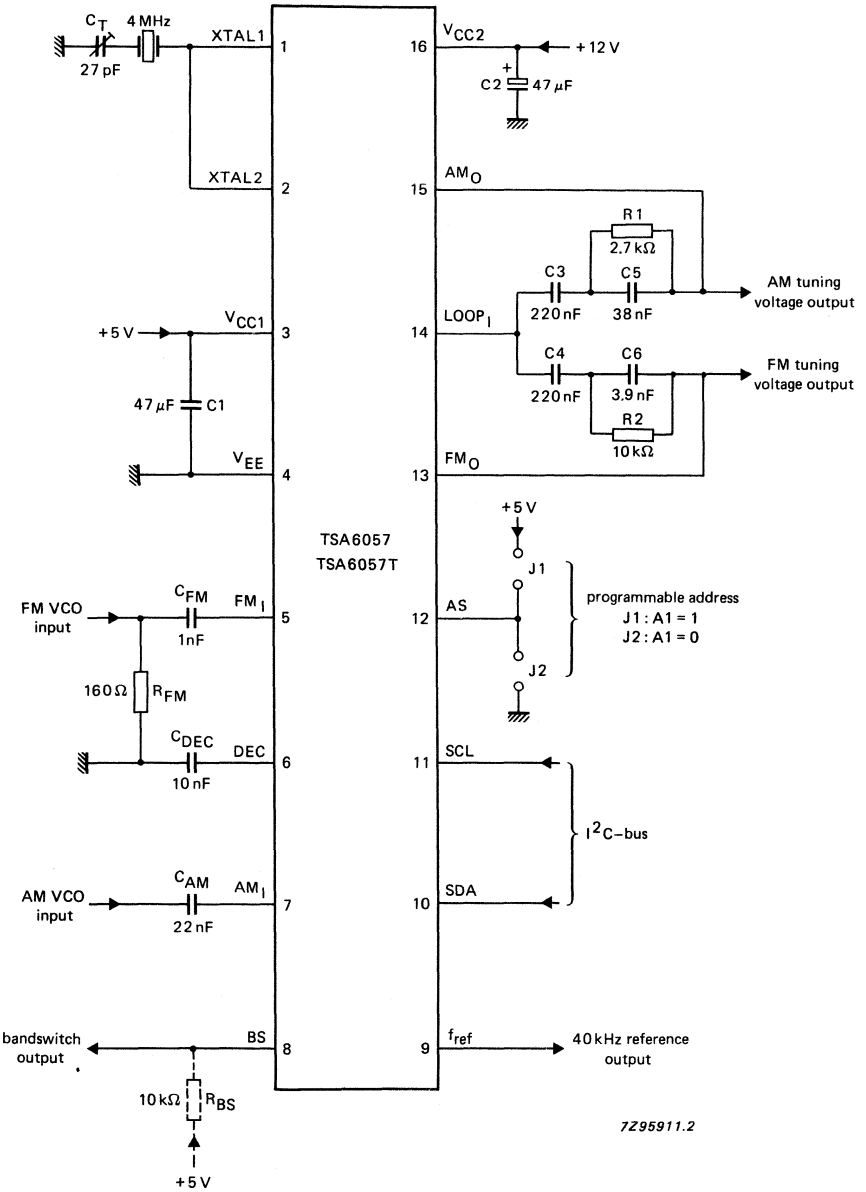


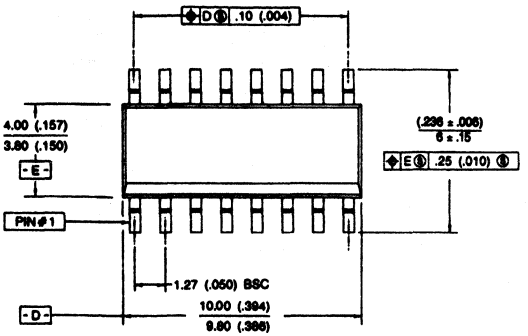
Fig.6 Application diagram

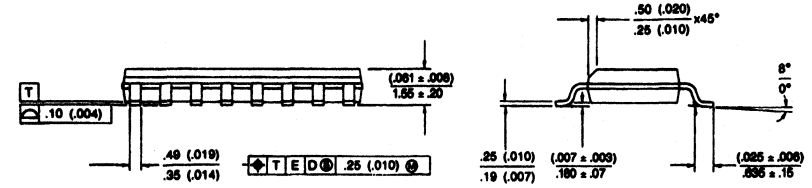
PACKAGE INFORMATION

Package outlines

Soldering

16-PIN PLASTIC SO (D PACKAGE)





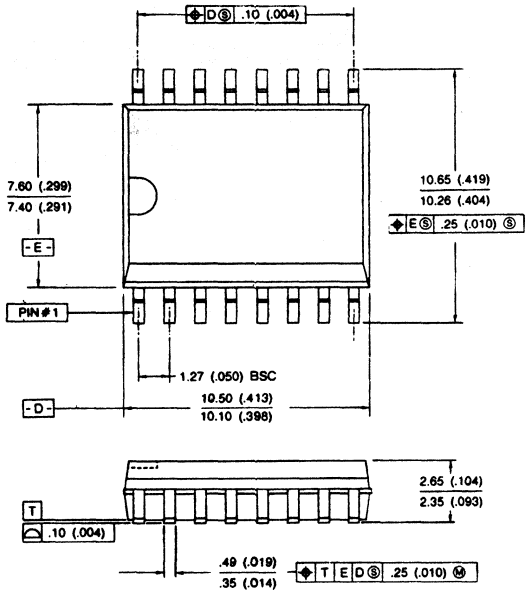
853-0005 88069

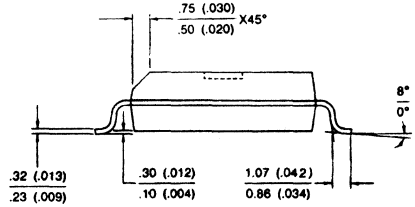
PO00252S

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body, and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SOL (D PACKAGE)





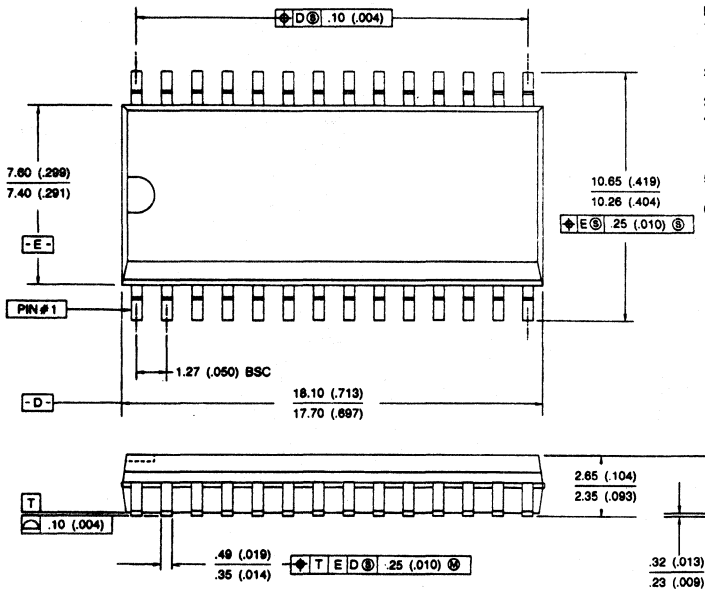
853-0171 81218

PO00241S

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

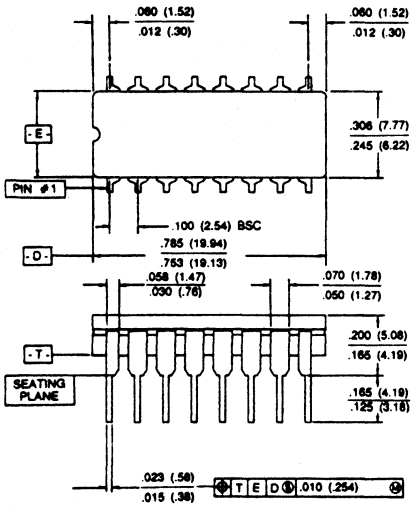
28-PIN PLASTIC SOL (D PACKAGE)

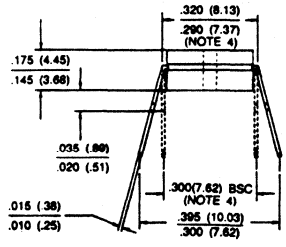


NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN CERDIP (F PACKAGE)



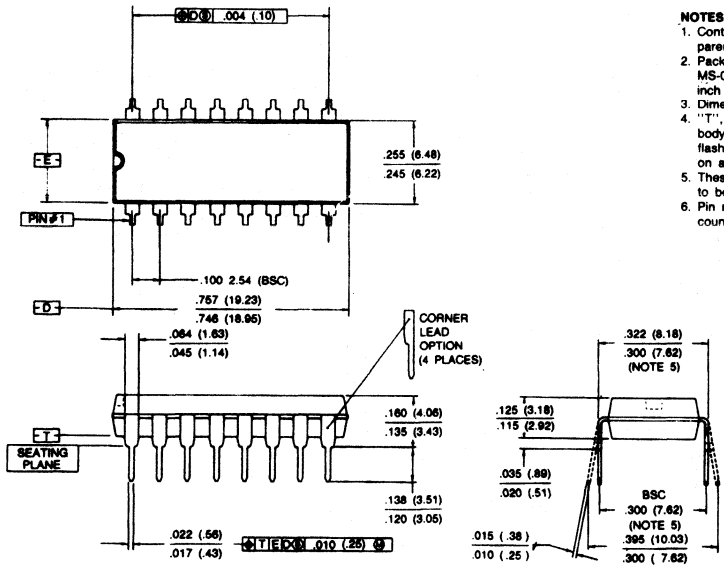


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0582 81594

FO004605

16-PIN PLASTIC DIP (N PACKAGE)



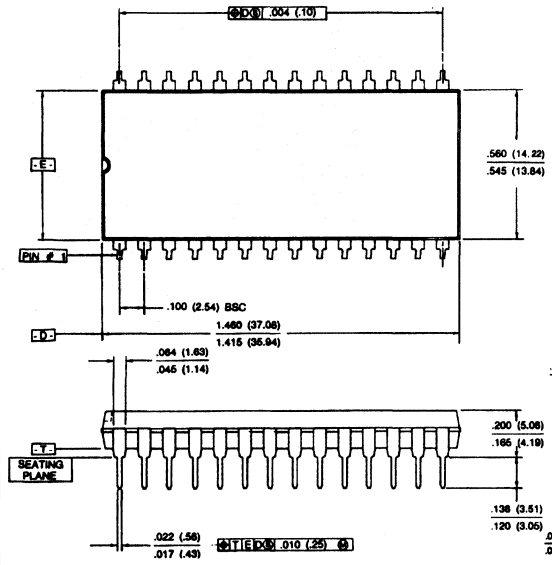
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

28-PIN PLASTIC DIP (N PACKAGE)



NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

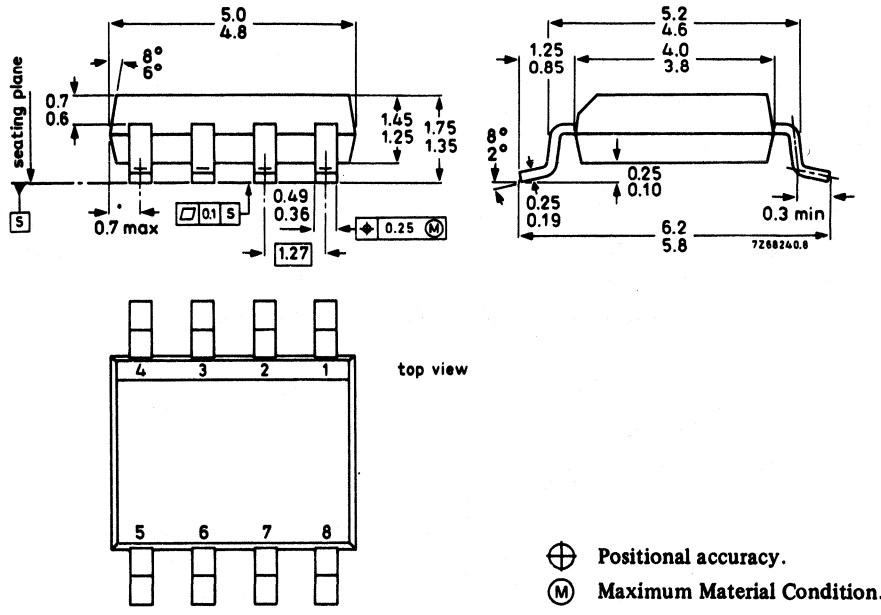
853-0413 84099

PO00372S

Package outlines for prefixes:

PCA, PCB, PCD, PCF,
SAA, SAF, TDA,
TEA and TSA

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

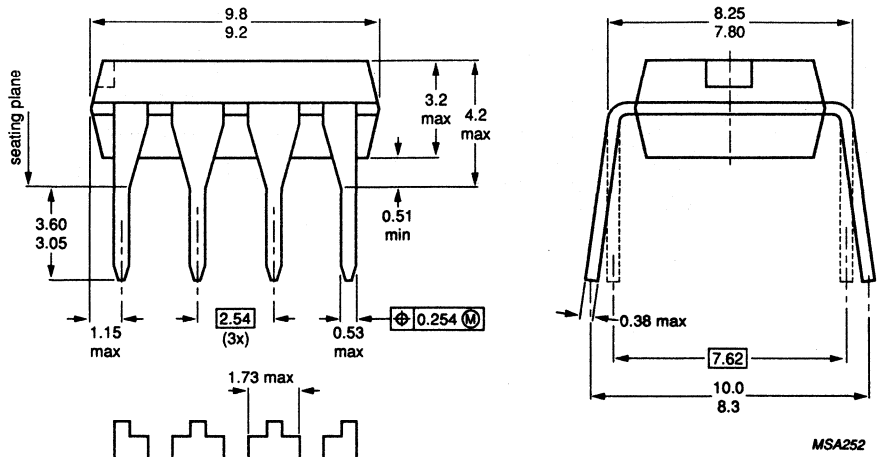


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

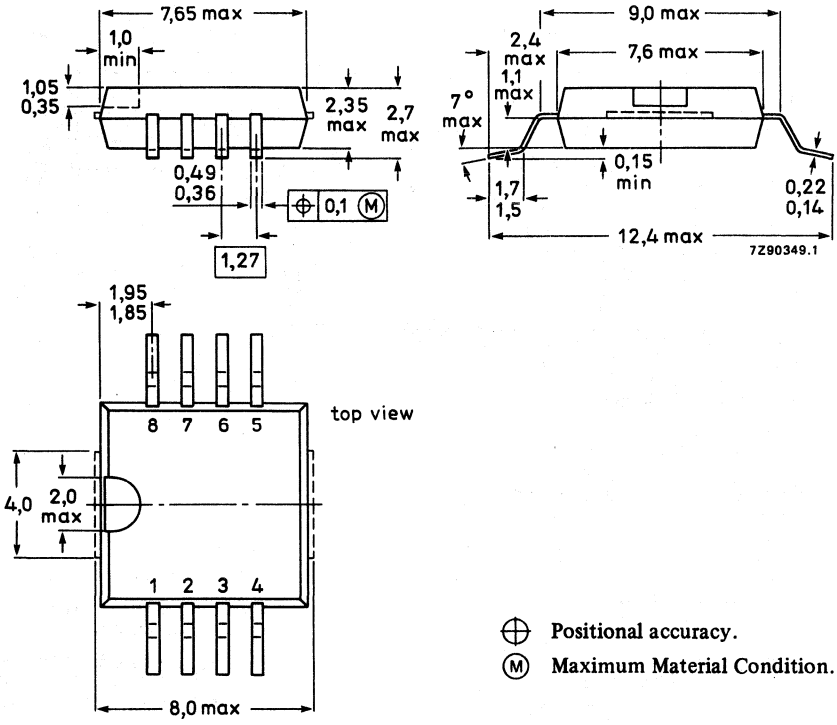
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)

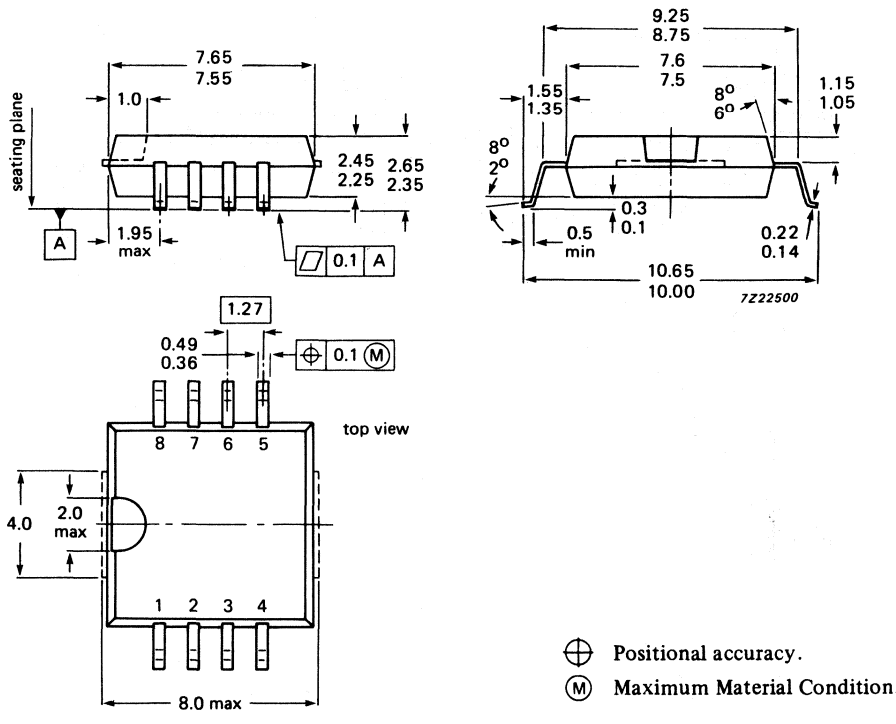


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)

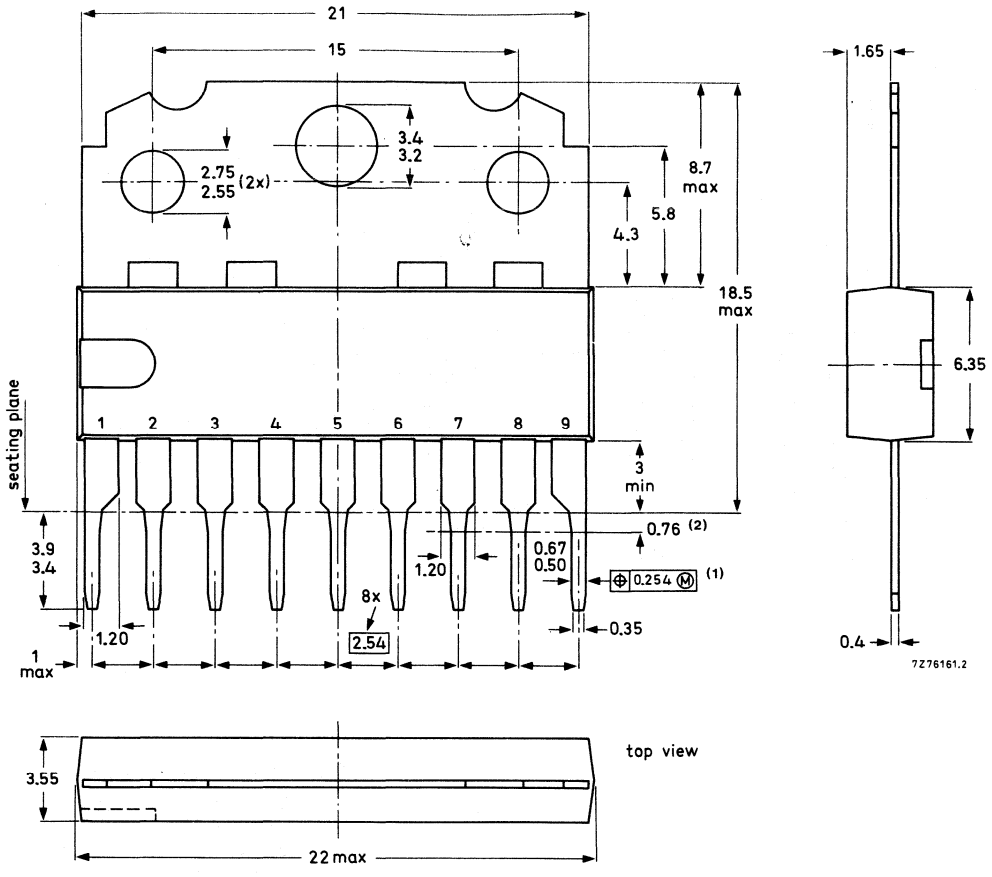


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

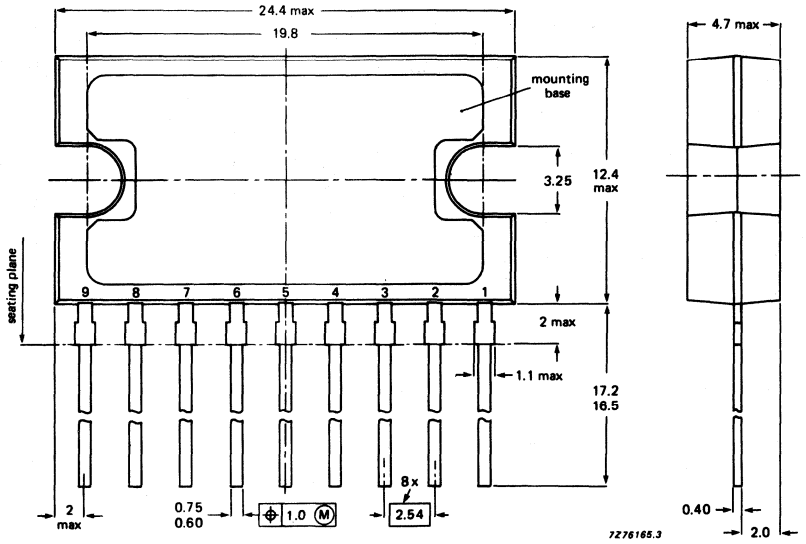
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT131)



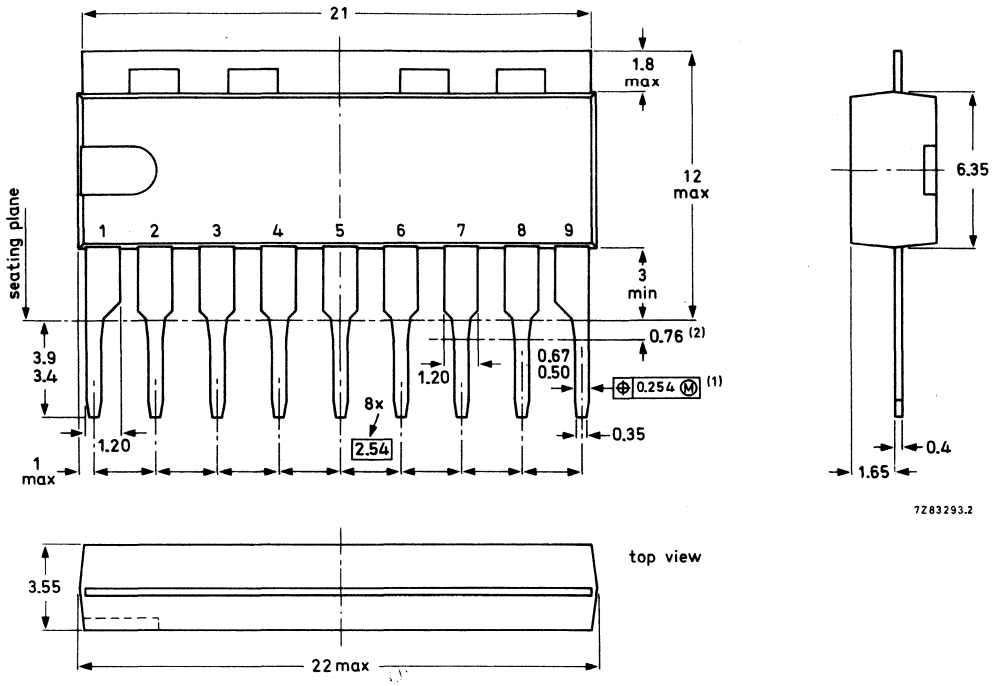
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT142)



⊕ Positional accuracy.

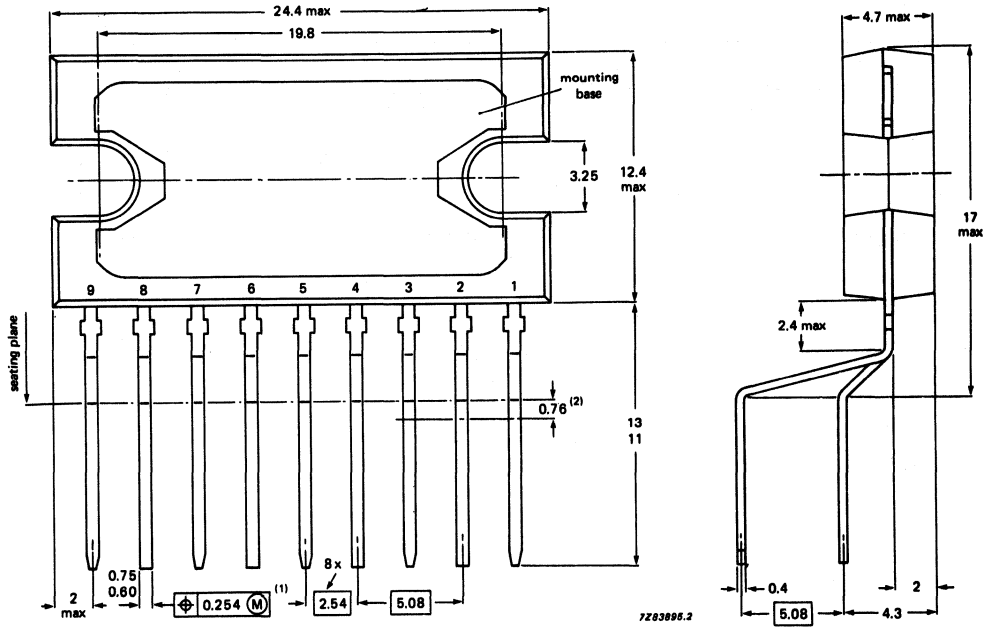
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT157)



⊕ Positional accuracy.

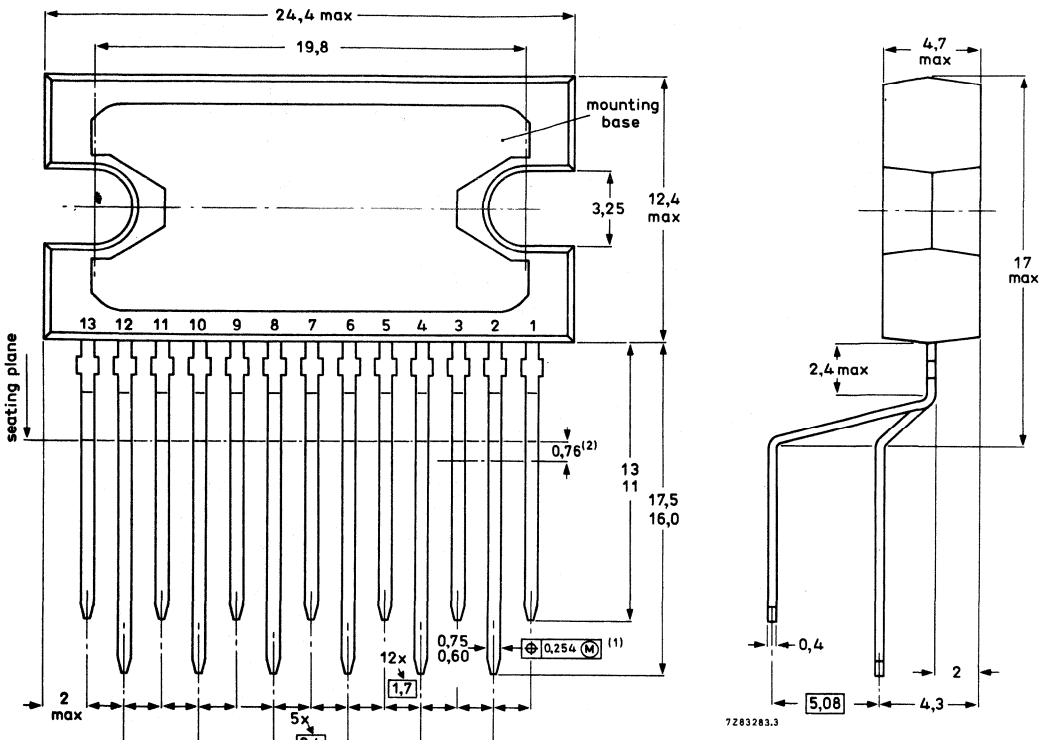
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT141RCE)



⊕ Positional accuracy.

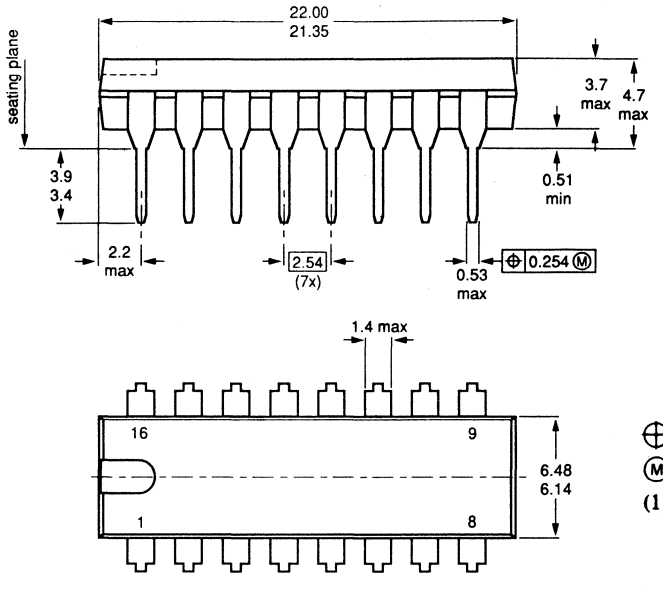
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



⊕ Positional accuracy.

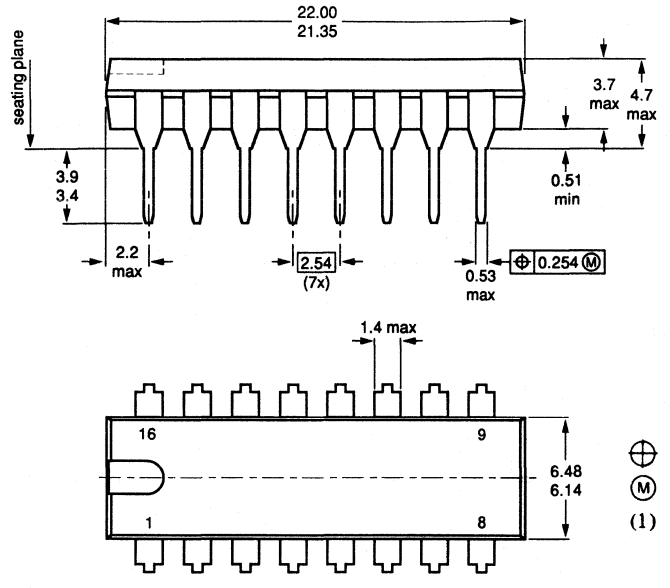
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)



⊕ Positional accuracy.

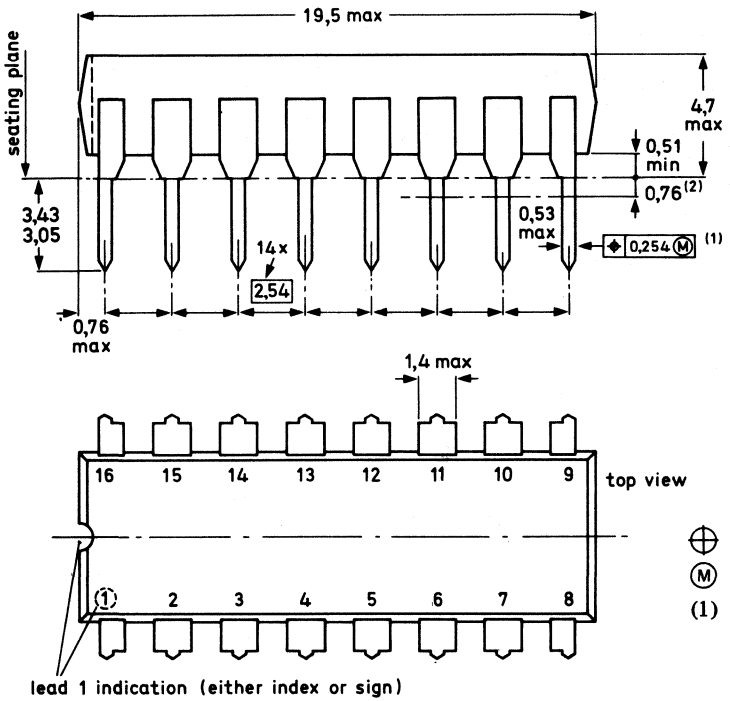
Ⓜ Maximum Material Condition.

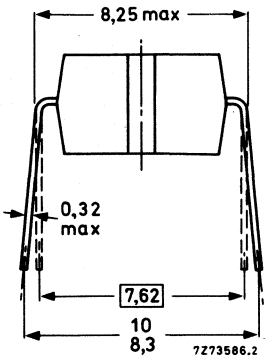
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38CP)





⊕ Positional accuracy.

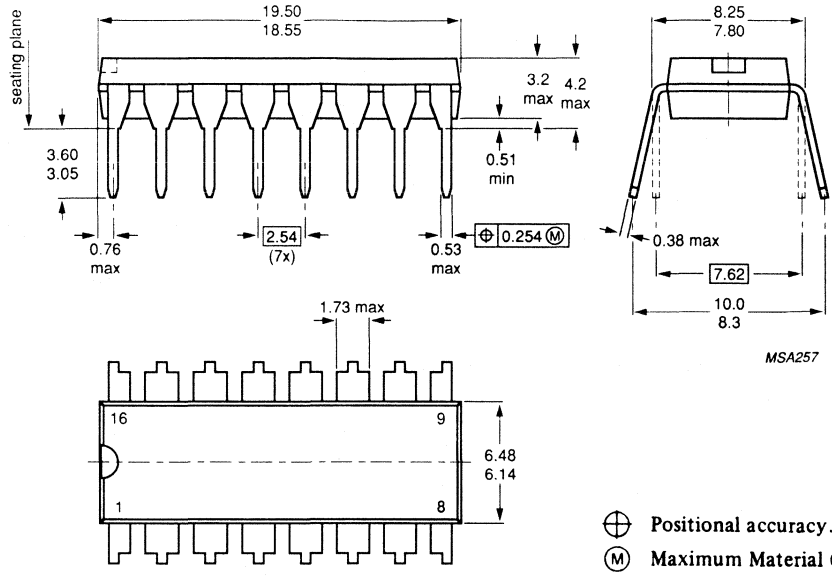
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38D)



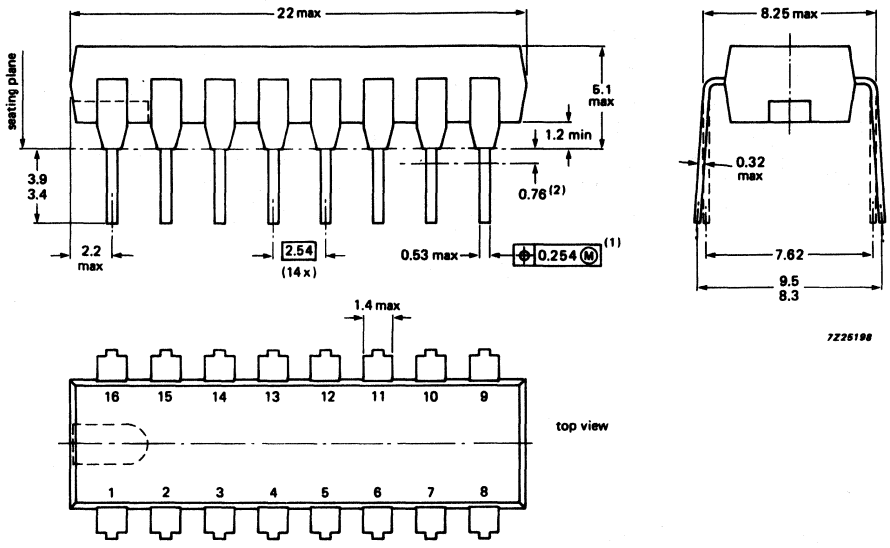
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (OPPOSITE BENT LEADS) (SOT38WBE)

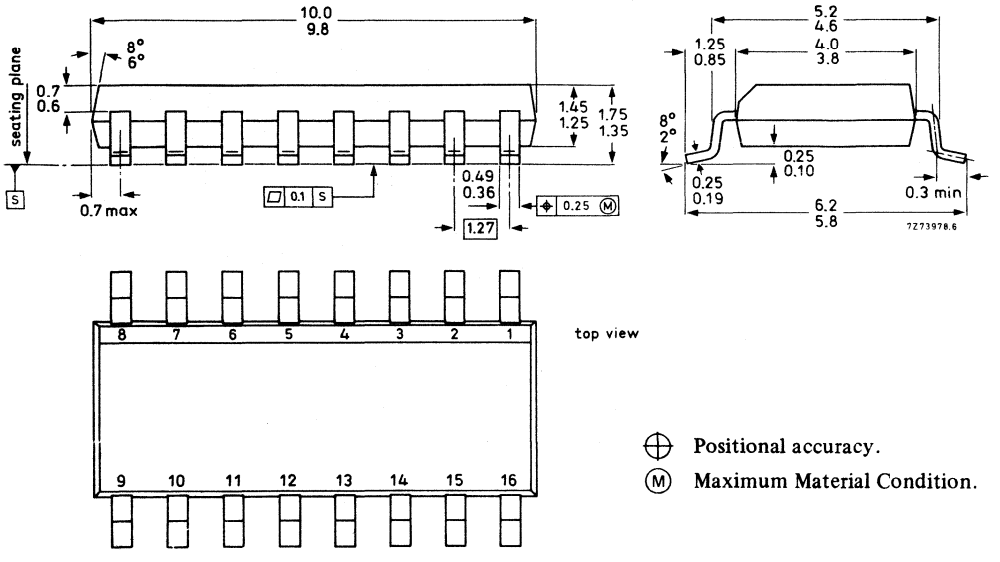


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

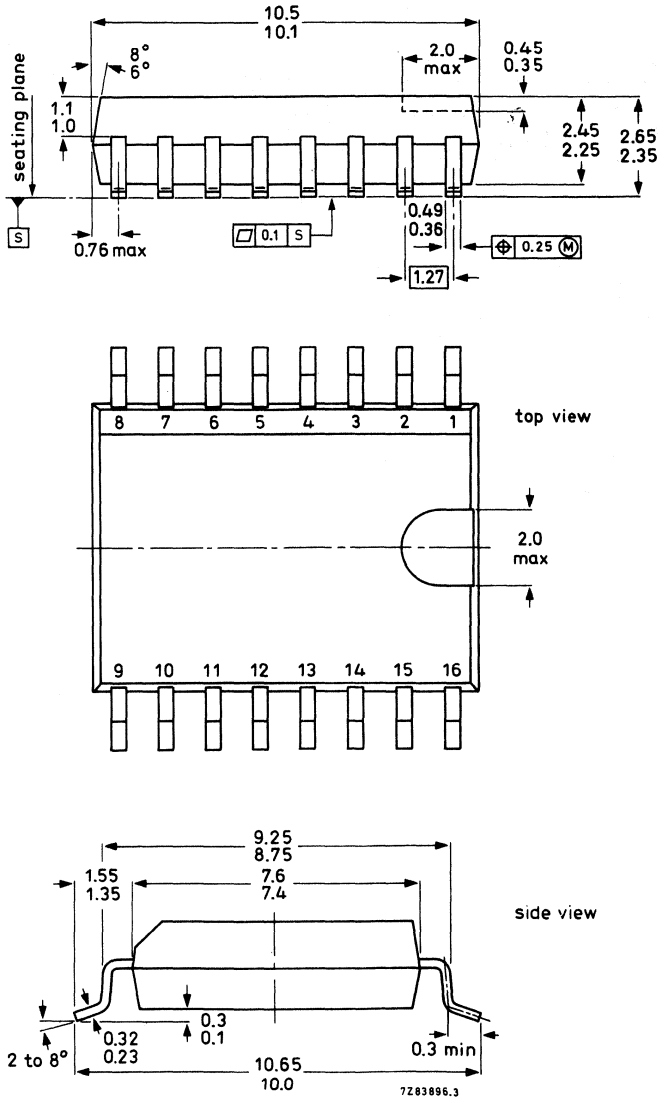


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

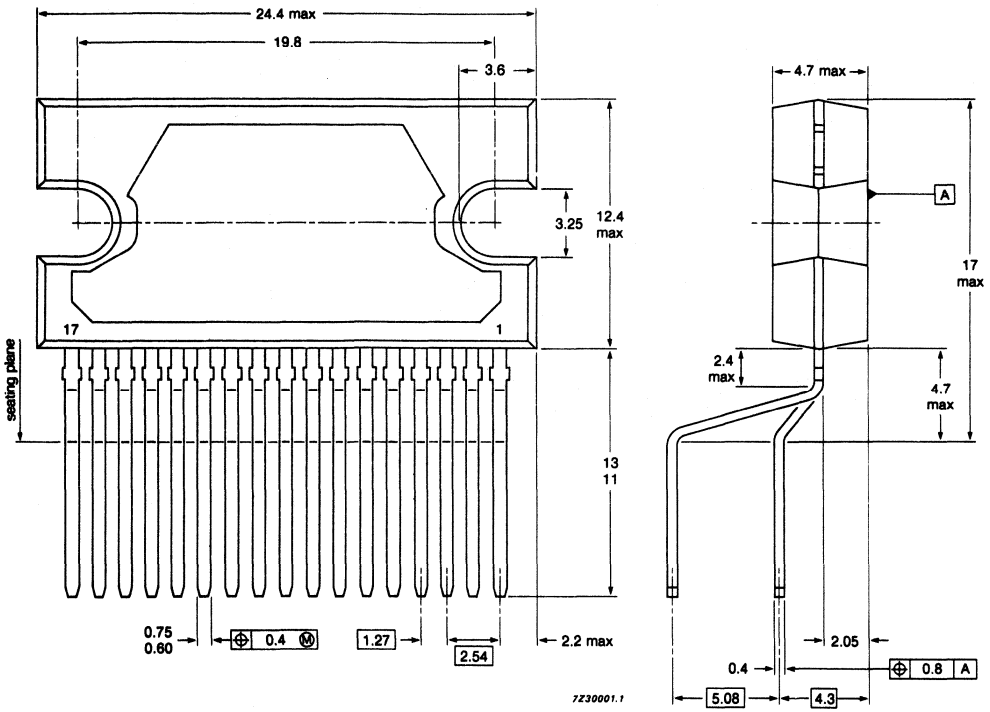


⊕ Positional accuracy.

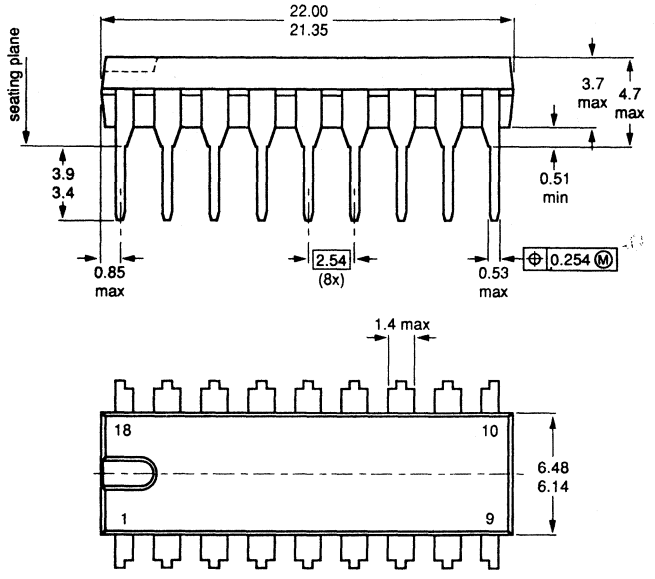
Ⓜ Maximum Material Condition.

Dimensions in mm

17-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT243RAA, RGA)



18-LEAD DUAL IN-LINE; PLASTIC (SOT102)



⊕ Positional accuracy.

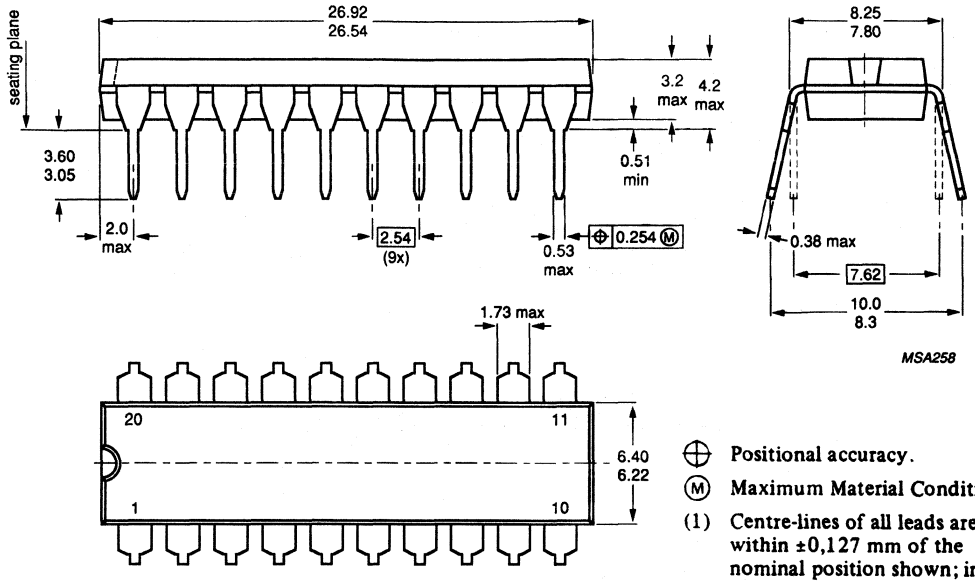
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

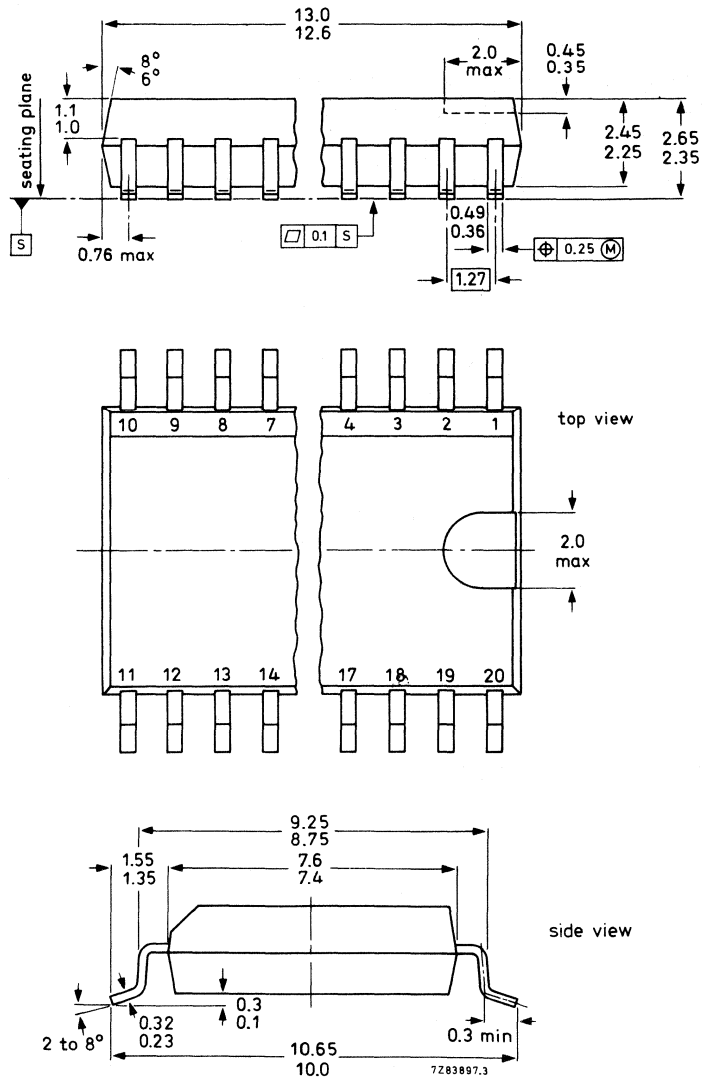
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

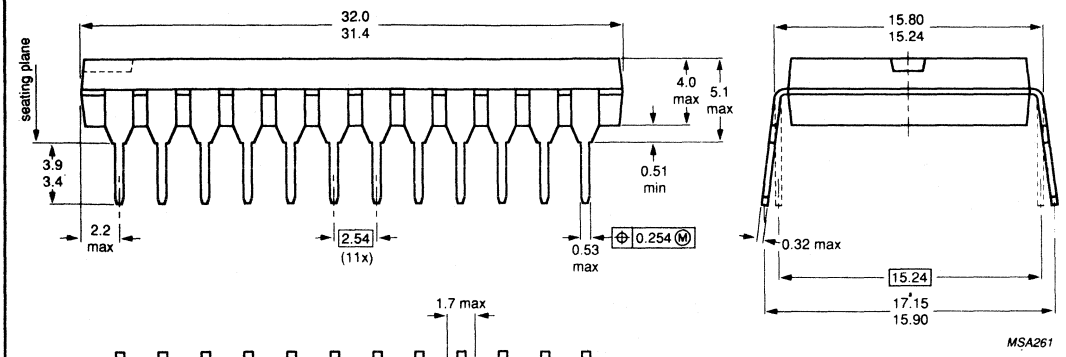


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

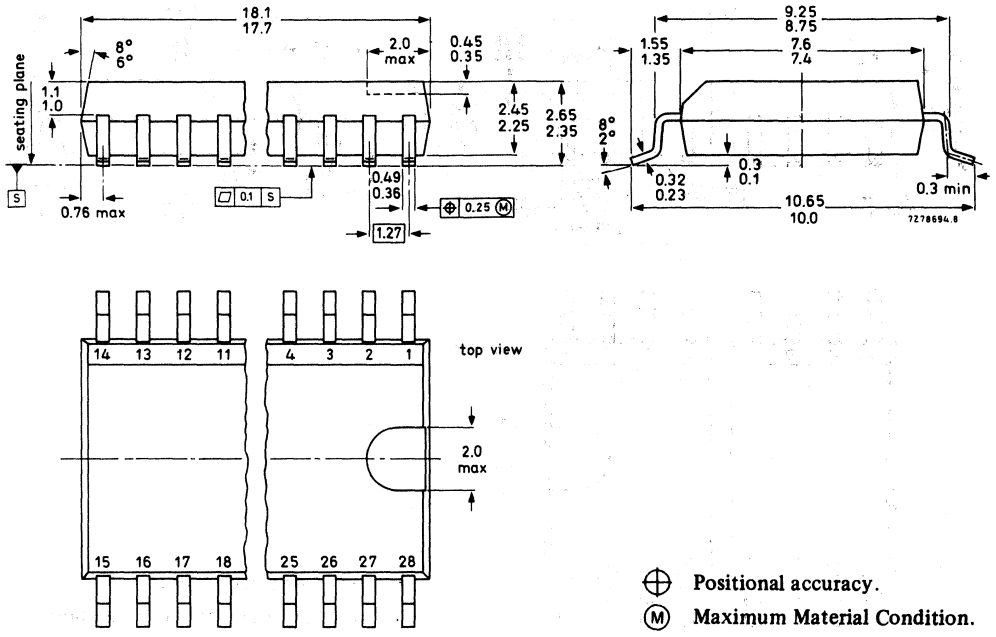
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

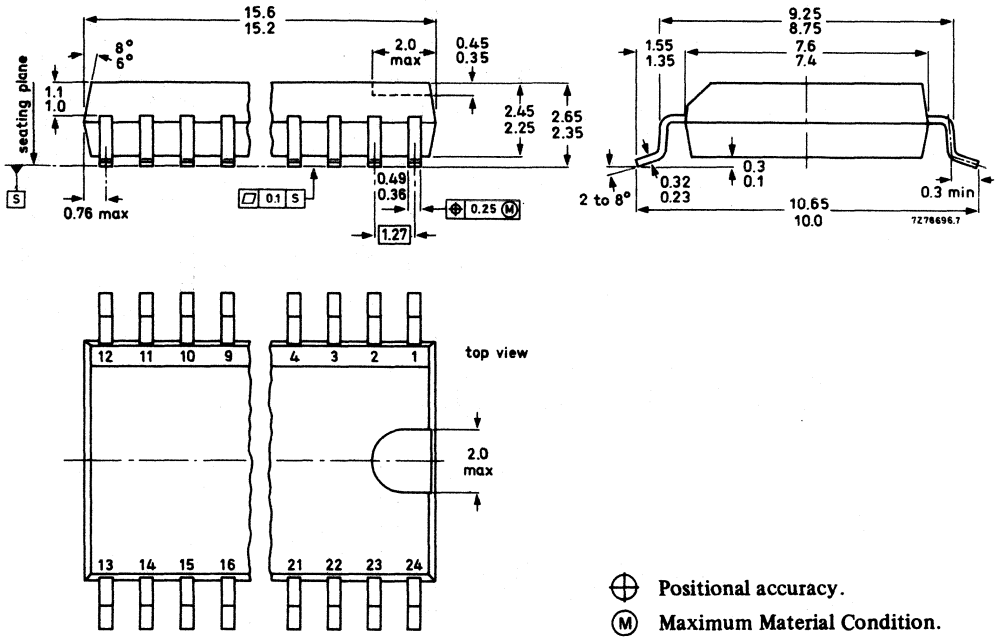


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)

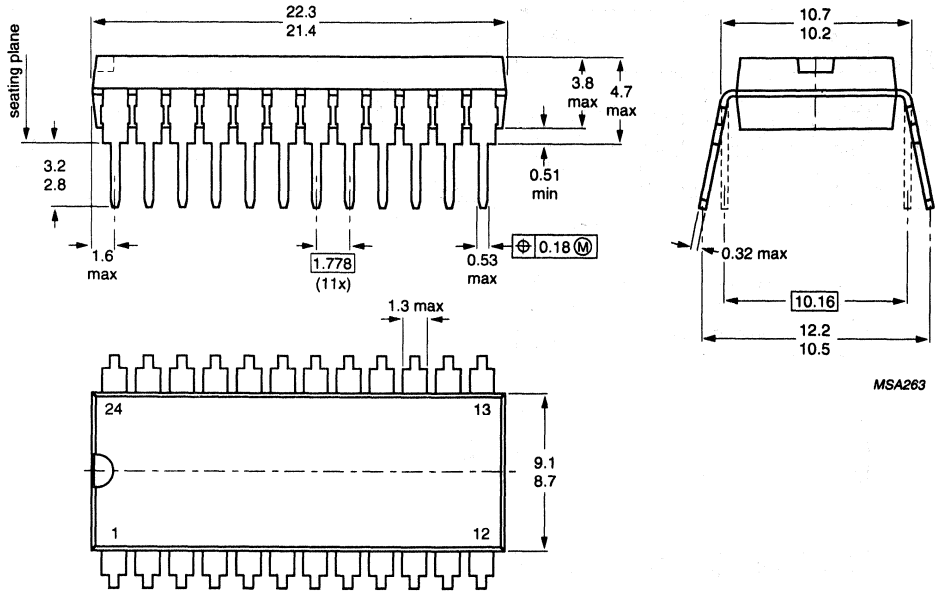


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

24-LEAD SHRING DUAL IN-LINE; PLASTIC (SOT234)

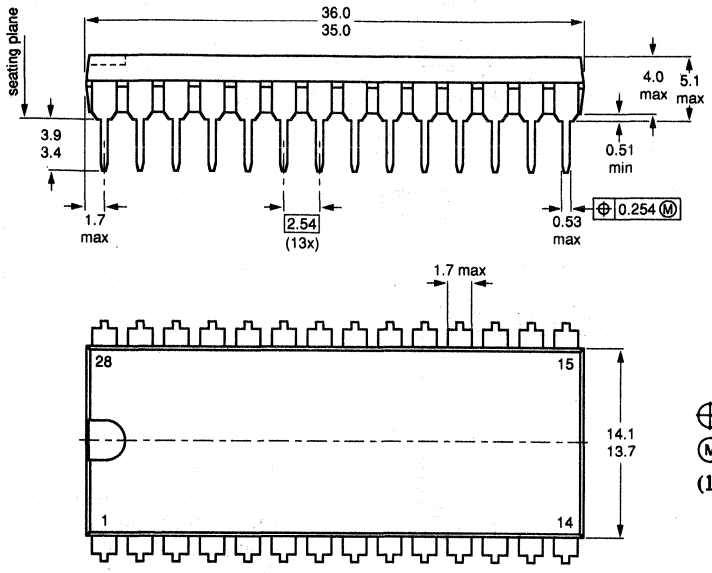


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

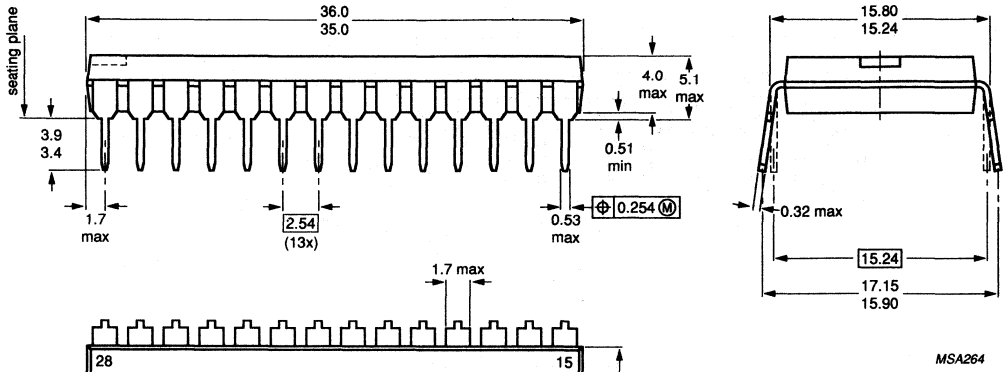
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

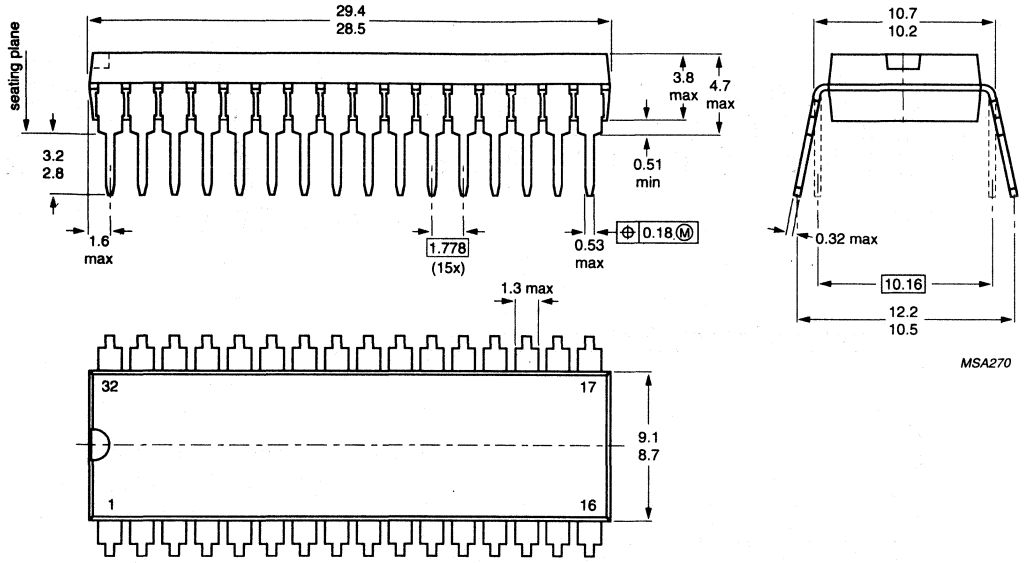
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

32-LEAD SHRINK DUAL IN-LINE; PLASTIC (SOT232)

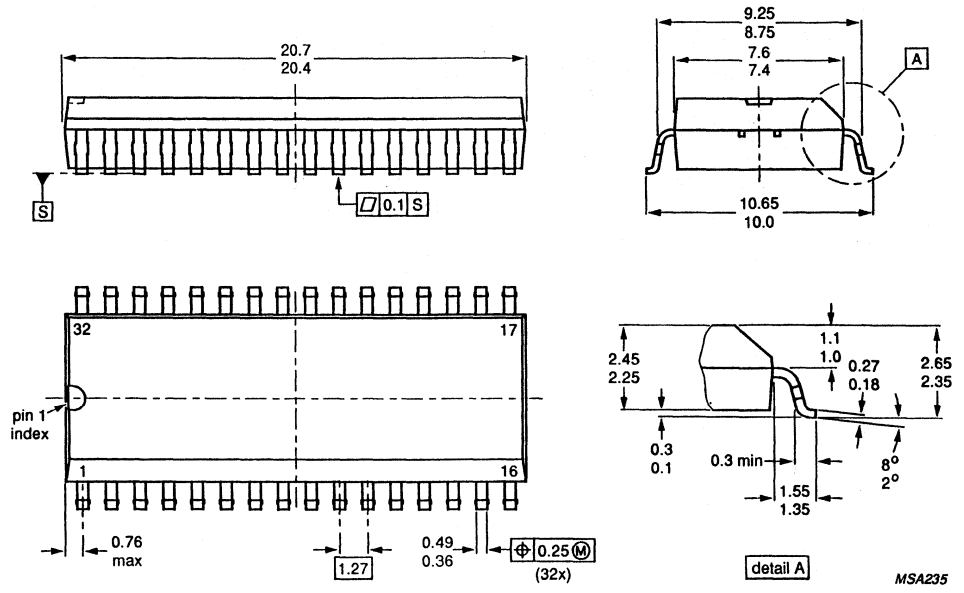


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

32-LEAD MINI-PACK; PLASTIC (SO32L; SOT287)

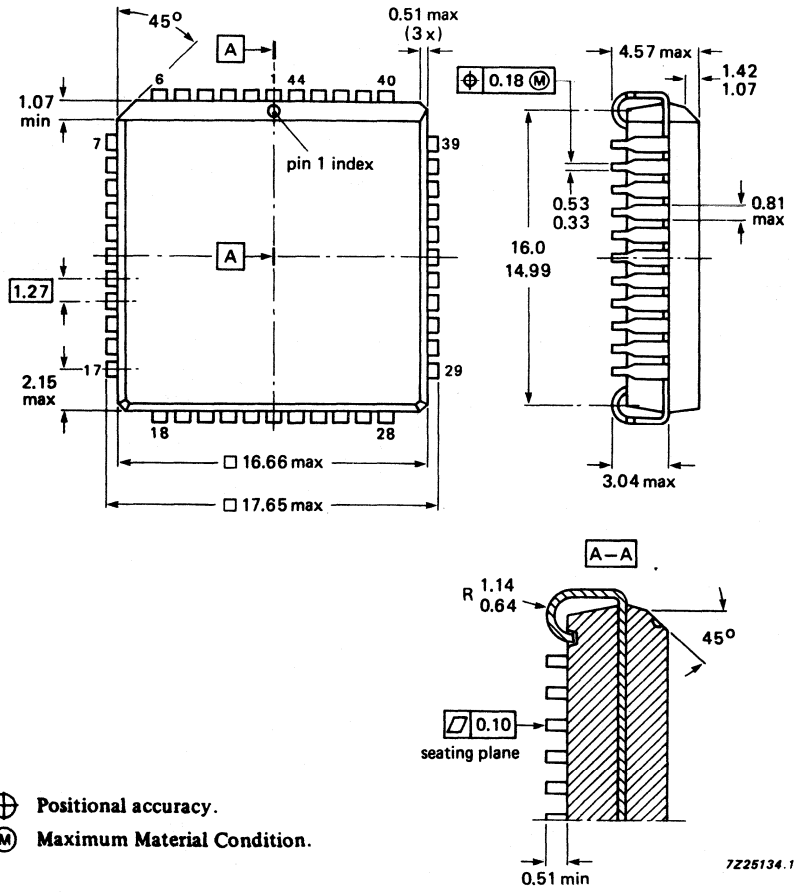


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT187AGA, CG)

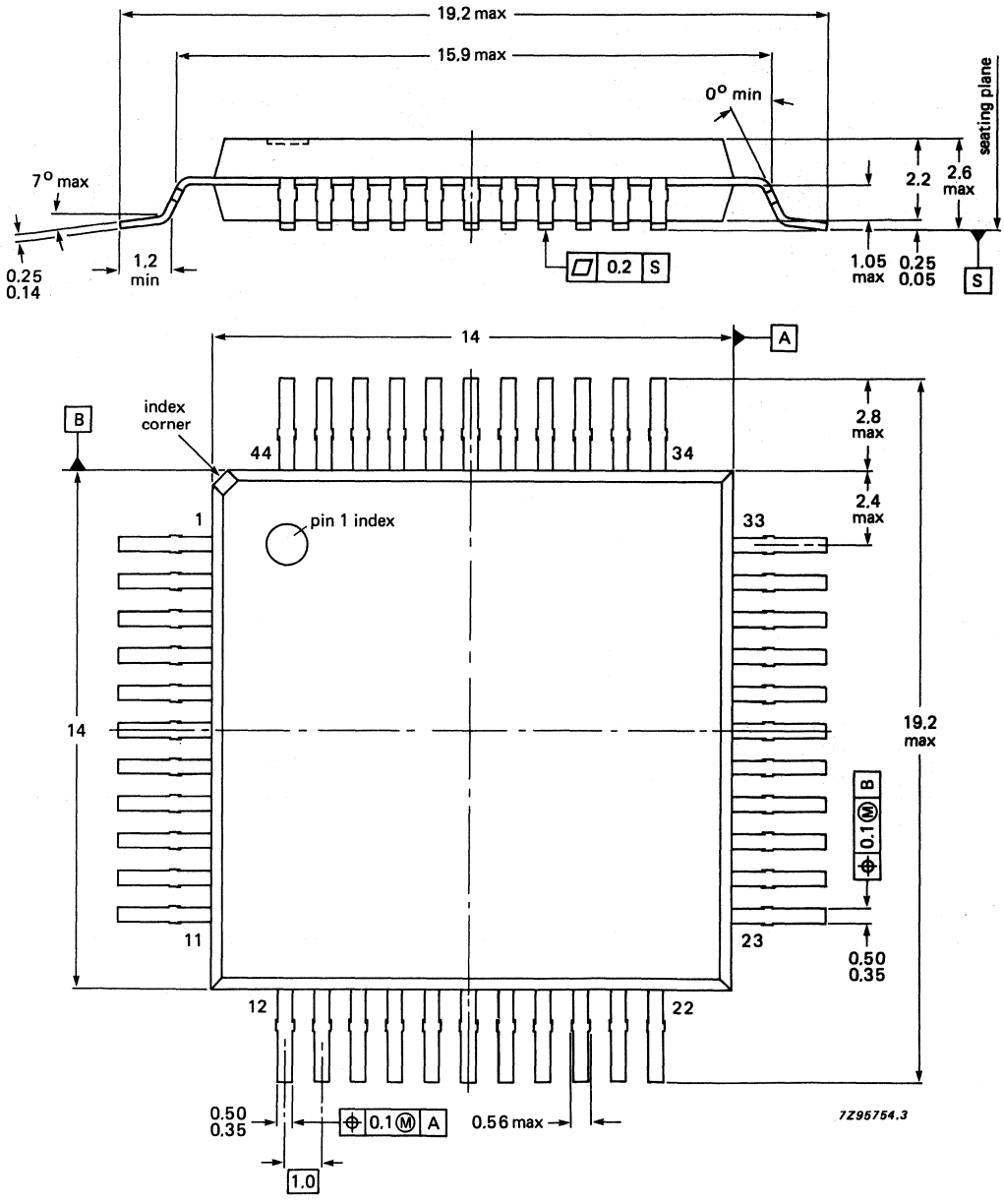


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205AG)

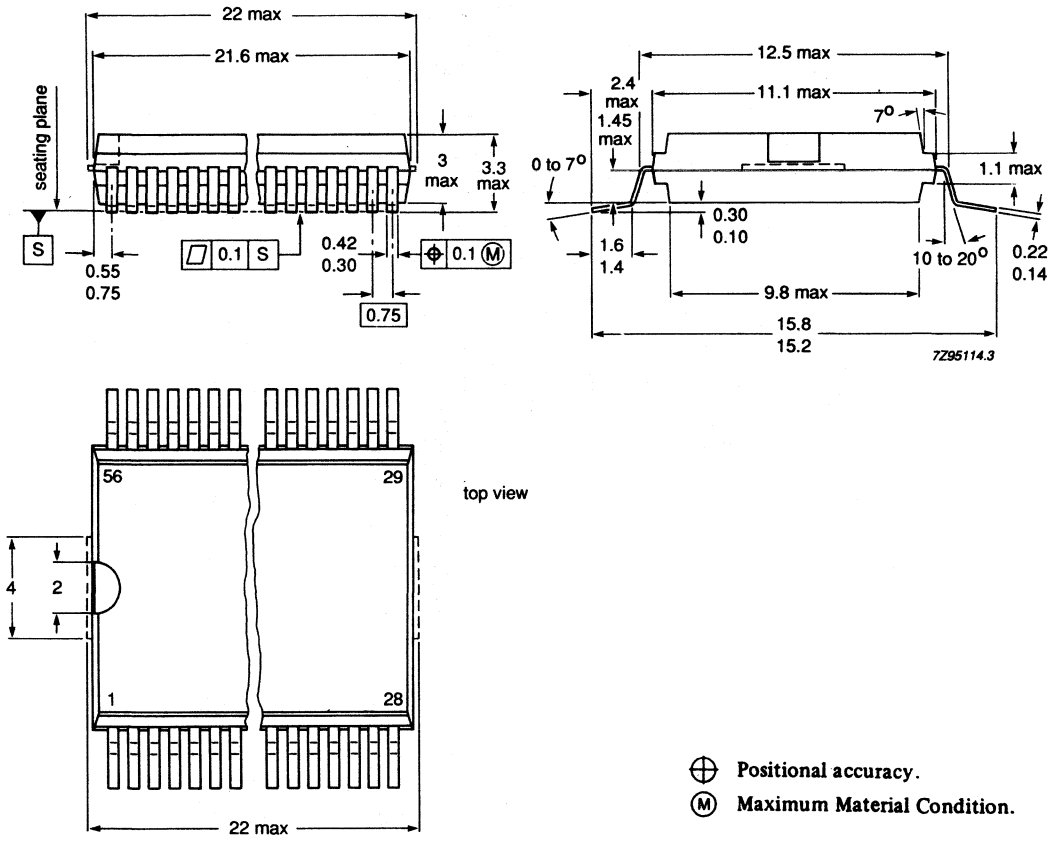


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

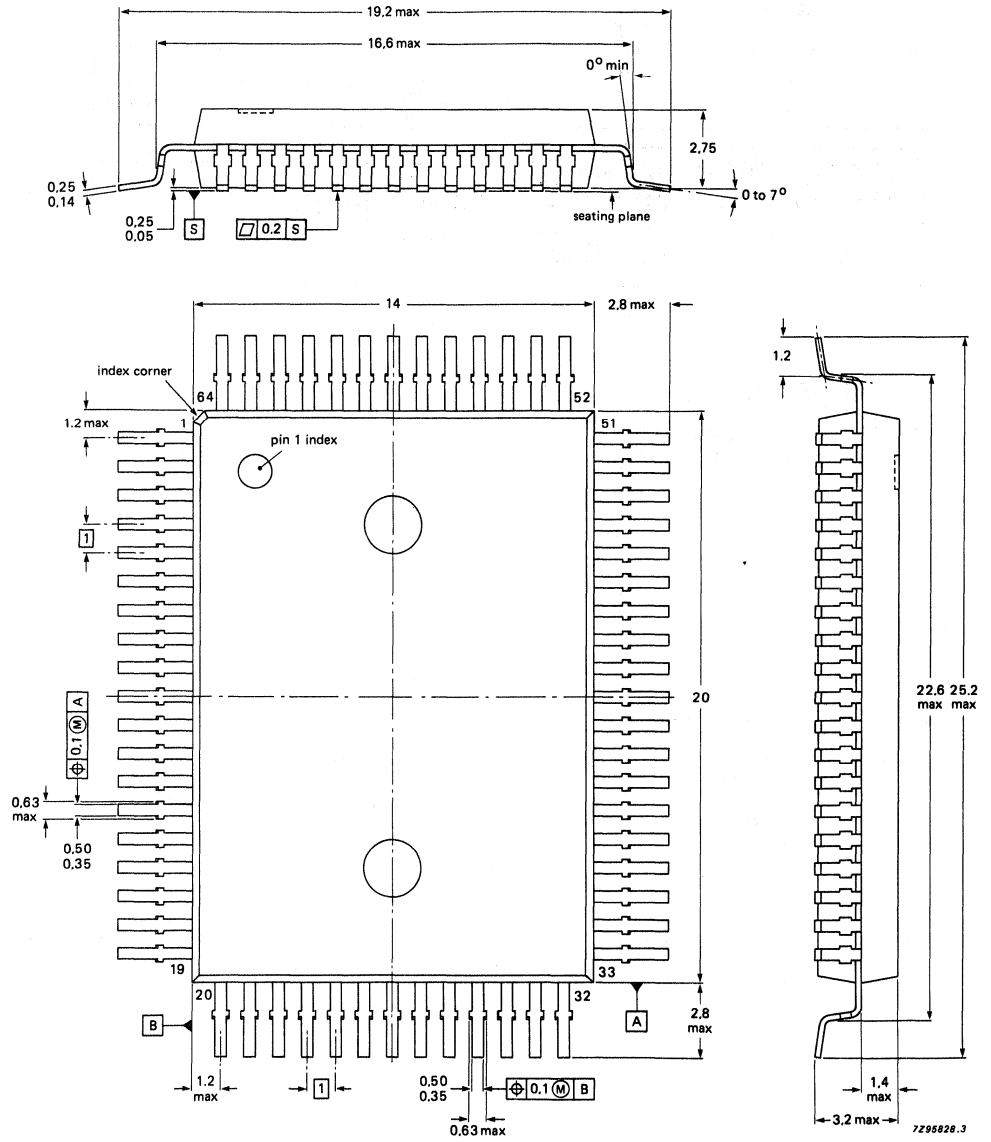
Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VS056; SOT190)



Dimensions in mm

64-LEAD QUAD FLAT-PACK; PLASTIC (SOT208)

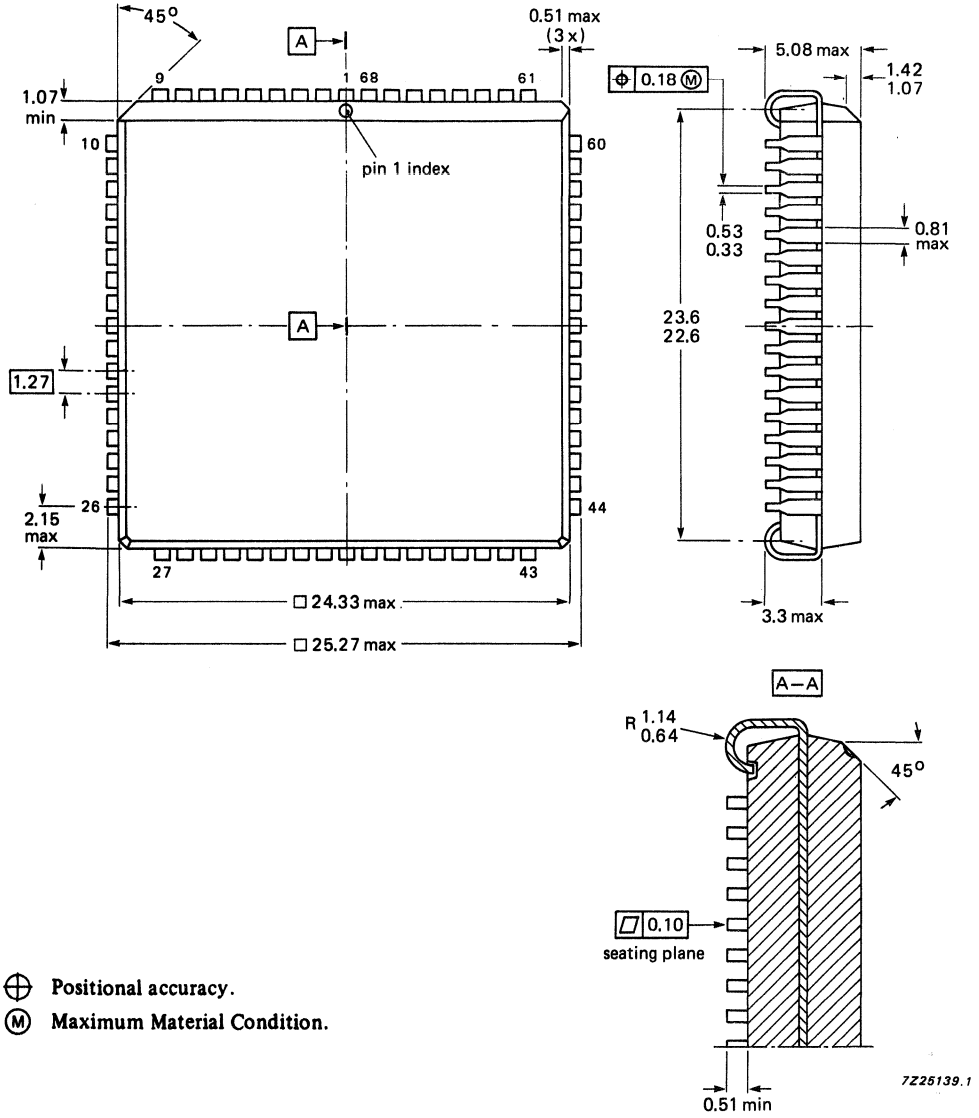


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT188AGA, CG)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

SOLDERING

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

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Data handbook system

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